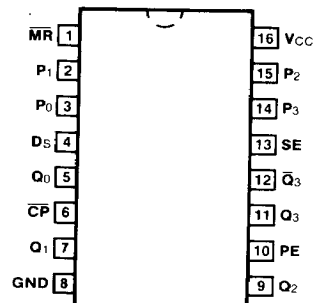


✓ 54/74179 010682

## 4-BIT SHIFT REGISTER

### CONNECTION DIAGRAM PINOUT A

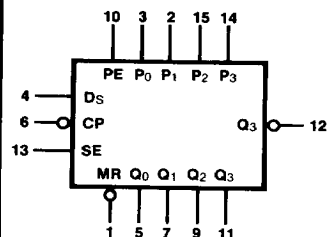


**DESCRIPTION** — The '179 features synchronous parallel or serial entry, asynchronous reset and parallel outputs, with the complement output of the fourth stage also available. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. A LOW signal on the Master Reset input overrides all other inputs and forces the Q outputs to the LOW state.

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74179PC		9B
Ceramic DIP (D)	A	74179DC	54179DM	6B
Flatpak (F)	A	74179FC	54179FM	4L

### LOGIC SYMBOL



V<sub>CC</sub> = Pin 16  
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
P <sub>0</sub> — P <sub>3</sub>	Parallel Data Inputs	1.0/1.0
D <sub>S</sub>	Serial Data Input	1.0/1.0
SE	Shift Enable Input	1.0/1.0
CP	Clock Pulse Input (Active Falling Edge)	1.0/1.0
MR	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q <sub>0</sub> — Q <sub>3</sub>	Flip-flop Outputs	20/10
Q <sub>3</sub>	Fourth Stage Complement Output	20/10

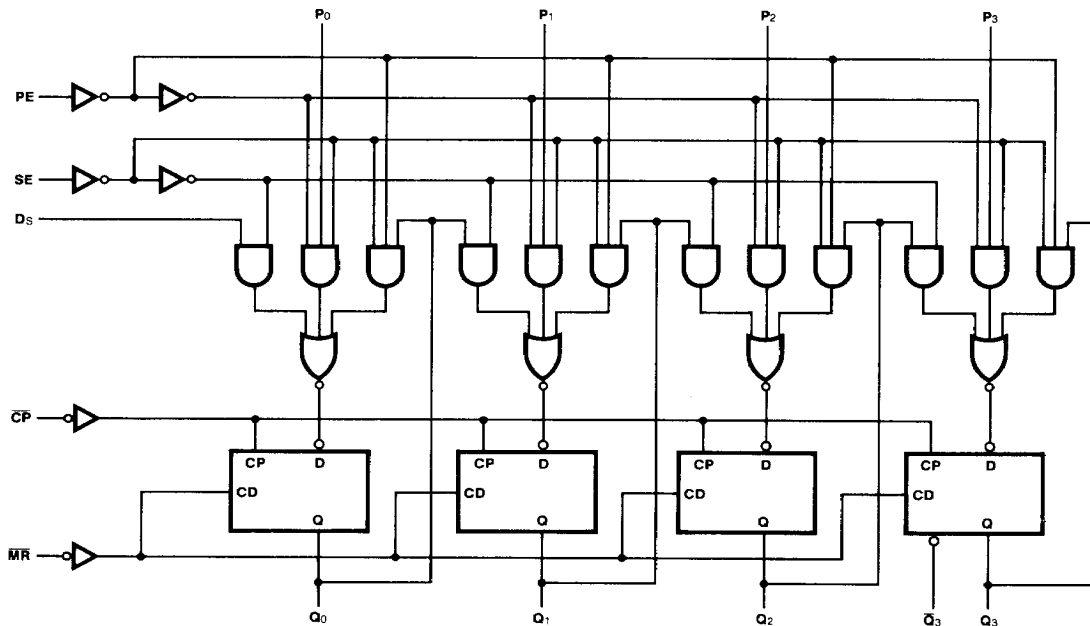
**FUNCTIONAL DESCRIPTION** — The '179 contains four D-type edge-triggered flip-flops and sufficient inter-stage logic to perform parallel load, shift right or hold operations. All state changes except reset are initiated by a HIGH-to-LOW transition of the clock. A LOW signal on  $\overline{MR}$  overrides all other inputs and forces the Q outputs LOW and  $\overline{Q}_3$  HIGH. With  $\overline{MR}$  HIGH, a HIGH signal on SE prevents parallel loading and permits a right shift each time the clock makes a HIGH-to-LOW transition. When  $\overline{MR}$  and SE are LOW, the signal applied to PE determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE,  $D_S$  and  $P_n$  inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

**MODE SELECT TABLE**

INPUTS				RESPONSE
$\overline{MR}$	SE	PE	$\overline{CP}$	
L	X	X	X	Asynchronous Reset; $Q_n \rightarrow \text{LOW}$ ; $\overline{Q}_3 \rightarrow \text{HIGH}$
H	H	X	$\downarrow$	Right Shift. $D_S \rightarrow Q_0$ ; $Q_0 \rightarrow Q_1$ , etc.
H	L	H	$\downarrow$	Parallel load. $P_n \rightarrow Q_n$
H	L	L	X	Hold

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER		54/74		UNITS	CONDITIONS
			Min	Max		
I <sub>CC</sub>	Power Supply Current	XM	70		mA	V <sub>CC</sub> = Max, P <sub>n</sub> = Gnd D <sub>s</sub> , $\overline{PE}$ , SE, $\overline{MR}$ = 4.5 V $\overline{CP}$ = $\overline{L}$
		XC	75			

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω			
		Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-9
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{CP}$ to Q <sub>n</sub>	26 35		ns	Figs. 3-1, 3-9
t <sub>PLH</sub>	Propagation Delay MR to Q <sub>3</sub>	23		ns	Figs. 3-1, 3-17
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>n</sub>	36		ns	

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS	
		Min	Max			
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>s</sub> or P <sub>n</sub> to $\overline{CP}$	30 30		ns	Fig. 3-7	
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>s</sub> or P <sub>n</sub> to $\overline{CP}$	5.0 5.0		ns		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW PE or SE to $\overline{CP}$	35 35		ns		
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW PE or SE to $\overline{CP}$	5.0 5.0		ns		
t <sub>w</sub> (H)	$\overline{CP}$ Pulse Width HIGH	20		ns		Fig. 3-9
t <sub>w</sub> (L)	$\overline{MR}$ Pulse Width LOW	20		ns		Fig. 3-17
t <sub>rec</sub>	Recovery Time $\overline{MR}$ to $\overline{CP}$	15		ns	Fig. 3-17	