Advance Information

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Bt858

12–18 MHz RGB/YCrCb-to-NTSC/PAL

Distinguishing Features

- NTSC or PAL Composite Video Output
- Separate Y/C Video (S-Video) Outputs
- Interlaced 60 Hz, 525-Line Digital RGB or YCrCb Input (NTSC Output)
- Interlaced 50 Hz, 625-Line Digital RGB or YCrCb Input (PAL Output)
- 4-Field NTSC or 8-Field PAL Generation
- Studio-Quality Outputs
- On-Chip Color Bar Generation
- Graphics/Video Mixing (Pixel Basis)
- Three 256 x 8 Input Lookup Table RAMs
- 15 x 24 Overlay Registers
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 160-pin PQFP Package
- Typical Power Dissipation: 1.25 W
- Pseudo Color/YCrCb Color Keying Capability

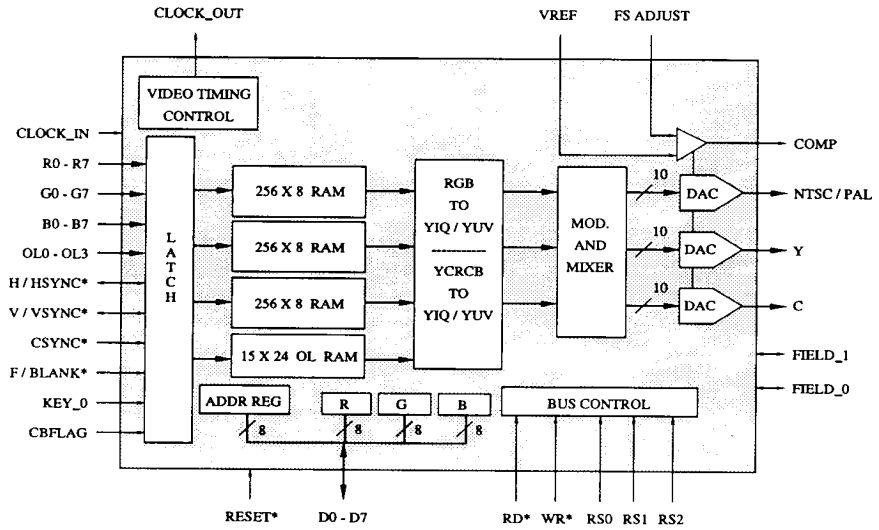
Applications

- Desktop Video
- Video Editing
- Video Presentations

Related Products

- Bt855

Functional Block Diagram



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Product Description

The Bt858 is designed specifically for graphics and imaging systems requiring the generation of studio-quality 4-field, 525-line (M) NTSC or 8-field, 625-line (B, D, G, H, I, N) PAL composite or Y/C (S-video) video signals at pixel clock rates of 12–18 MHz. Standards conversion applications may also be generated by 4.43 NTSC. The number of pixels per scan line is programmable, so applications other than 12.27 MHz square pixel NTSC, 13.5 MHz CCIR601, and 14.75 MHz square pixel PAL are easily supported.

Video timing control may be input with horizontal and vertical sync, composite sync, or the CCIR601 H, V, and F control signals. Alternately, the Bt858 may generate the horizontal and vertical sync signals.

The interlaced RGB or YCrCb data is converted to either YIQ (NTSC operation) or YUV (PAL operation). The color difference signals are digitally low-pass filtered to 1.3 MHz and modulated. The rise and fall times of sync, burst envelope, and video blanking are internally controlled to be within composite video specifications.

Analog luminance (Y) and chroma (C) information is available on the Y and C analog outputs for interface to S-video equipment. Composite analog video is output simultaneously onto the NTSC/PAL analog output.

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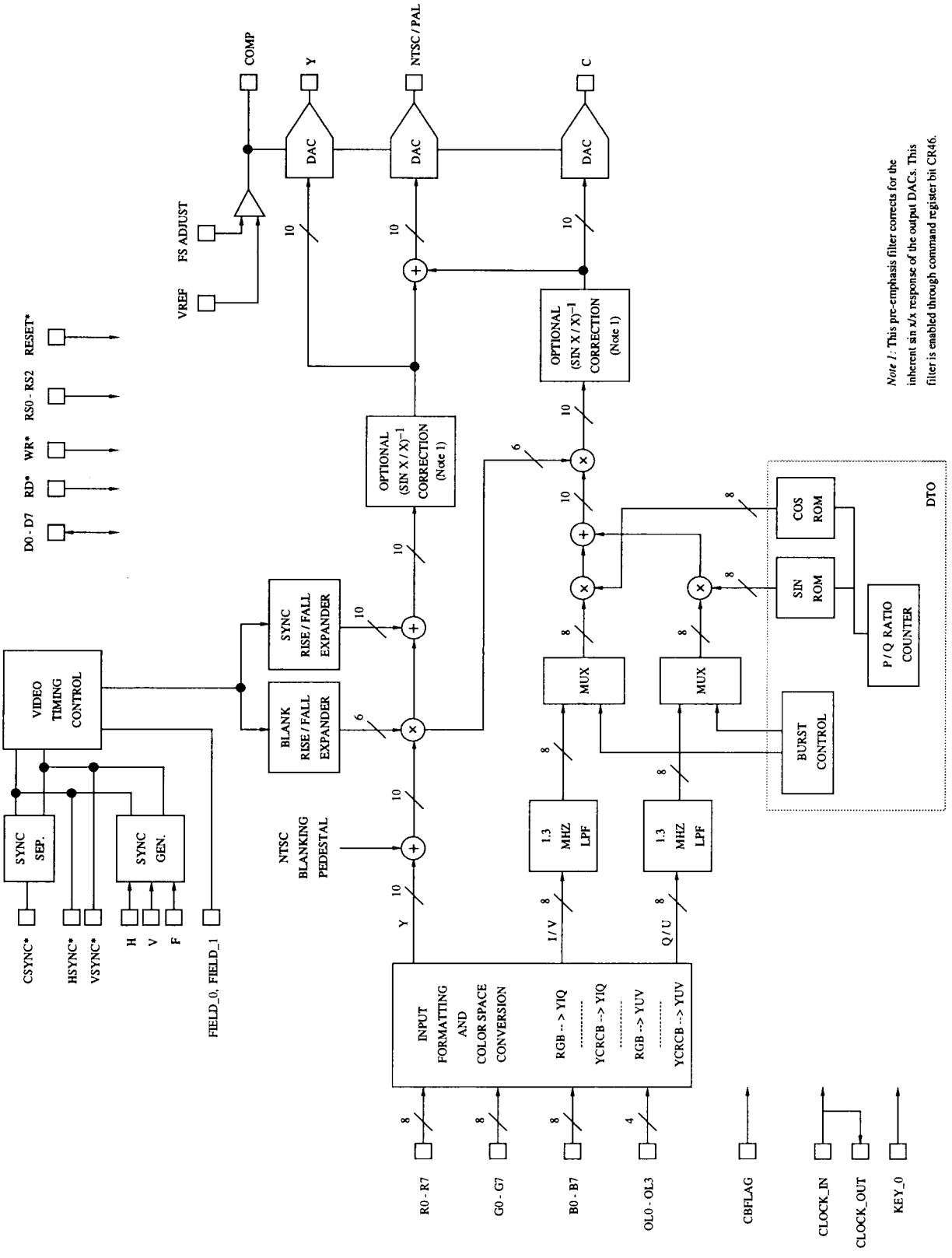


Figure 1. Detailed Block Diagram.

Circuit Description—MPU Interface

MPU Interface

As illustrated in the detailed block diagram (Figure 1), the Bt858 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, or control registers, as shown in Table 1. The 8-bit address register addresses the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode, control register read/write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	control registers

Table 1. Control Input Truth Table.

Circuit Description—MPU Interface (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Control Register Data

To write control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a write cycle, using RS0–RS2 to select the control registers. After the write cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may write by writing another byte of data. A block of data in consecutive control registers may be written by writing the start address and performing continuous write cycles until the entire block has been written.

Reading Control Register Data

To read control register data, the MPU loads the address register (control register read/write mode) with the address of the control register to be read. The MPU performs a read cycle, using RS0–RS2 to select the control registers. After the read cycle, the address register (ADDR0–ADDR7) increments to the next location, which the MPU may read by reading another byte of data. A block of data in consecutive control registers may be read by writing the start address and performing continuous read cycles until the entire block has been read.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

When the MPU is accessing the control registers, the address register does not reset to $00 following a read or write cycle to address $FF. Data read from reserved locations returns invalid data.

The MPU interface operates asynchronously to the pixel clock. Data transfers that occur between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic and take place in the period between MPU accesses. To reduce noticeable sparkling on the analog outputs during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles (or Y, Cr, and Cb read/write cycles), the address register has 2 additional bits (ADDRa, ADDRb) that count modulo three, as specified in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7), are accessible to the MPU. These bits address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When the MPU is writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input (R0, G0, and B0). Bit D0 also corresponds to data bus bit D0.

Note: The pixel read mask register is not initialized upon power-up. The user must initialize this register for proper operation.

Circuit Description—MPU Interface (continued)

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	0	1	red/Cr value
	01	x	0	1	green/Y value
	10	x	0	1	blue/Cb value
ADDR0–7 (counts binary)	$00–$FF	0	0	1	color palette RAMs
	$x0	1	0	1	reserved
	$x1	1	0	1	overlay color 1
	:	:	:	:	:
	$xF	1	0	1	overlay color 15
	$00	1	1	0	command register_0
	$01	1	1	0	command register_1
	$02	1	1	0	command register_2
	$03	1	1	0	command register_3
	$04	1	1	0	command register_4
	$05	1	1	0	reserved ($00)
	$06	1	1	0	P1 low register (Note 1)
	$07	1	1	0	P1 high register (Note 1)
	$08	1	1	0	P2 low register (Note 1)
	$09	1	1	0	P2 high register (Note 1)
	$0A	1	1	0	Fsc phase adjust low register
	$0B	1	1	0	Fsc phase adjust high register
	$0C	1	1	0	HCOUNT low register
	$0D	1	1	0	HCOUNT high register
	$0E	1	1	0	color key_0 register
	$0F	1	1	0	color mask_0 register

Note 1: Writing to any of these locations automatically resets the timing circuity.

Table 2. Address Register (ADDR) Operation.

Circuit Description—Pixel Input Formats

Overlays

The OL0–OL3 inputs select overlays and have priority over the pixel data. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the R0–R7, G0–G7, and B0–B7 pixel data. Overlay data must be in the same color space as the pixel data, and the overlay palette data must be in 2's complement format.

OL3–OL0	Color Selected
0000	pixel input port
0001	overlay color 1
:	:
1111	overlay color 15

24-bit RGB Input Mode (8, 8, 8)

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN.

The R0–R7 inputs address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

16-bit RGB Input Mode (5, 6, 5)

The OL0–OL3, R0–R7, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R3–R7 inputs address the lower 32 locations of the red color palette RAM. The G5–G7 inputs and R0–R2 address the lower 64 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

16-bit RGB Input Mode (6, 6, 4)

The OL0–OL3, R0–R7, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The B0–B7 inputs are ignored.

The R2–R7 inputs address the lower 64 locations of the red color palette RAM. The G4–G7, R0, and R1 inputs address the lower 64 locations of the green color palette RAM. The G0–G3 inputs address the lower 16 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

15-bit RGB Input Mode (5, 5, 5)

The OL0–OL3, R0–R6, and G0–G7 inputs are latched on the rising edge of CLOCK_IN. The R7 and B0–B7 inputs are ignored.

The R2–R6 inputs address the lower 32 locations of the red color palette RAM. The G5–G7, R0, and R1 inputs address the lower 32 locations of the green color palette RAM. The G0–G4 inputs address the lower 32 locations of the blue color palette RAM. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Circuit Description—Pixel Input Formats (continued)

24-bit YCrCb Mode

The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The Y0–Y7 are input via G0–G7, Cr0–Cr7 are input via R0–R7, and Cb0–Cb7 are input via B0–B7. The Y0, Cr0, and Cb0 are the least significant bits.

The Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each lookup table RAM provides 8 bits of information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation). Before addressing the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation), Y has an input range of 16–235. Values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240 with 128 equal to zero. Values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of YCrCb color information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation).

16-bit YCrCb Mode

The OL0–OL3, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. The R0–R7 inputs are ignored. The Y0–Y7 are input via G0–G7, and multiplexed Cr and Cb data is input via the B0–B7 inputs, as specified in Table 3. The Y0, Cr0, and Cb0 inputs are the least significant bits.

The CbFLAG input is used to indicate when Cb data is present on the B0–B7 inputs. While CbFLAG is a logical one, Cb data is latched; while CbFLAG is a logical zero, Cr data is latched. CbFLAG is latched on the rising edge of CLOCK_IN.

The 16-bit YCrCb (4:2:2) data is converted to 24-bit YCrCb (4:4:4) with a 2-tap interpolation filter to generate the missing Cr and Cb values as follows. The original Cr and Cb values pass through unchanged.

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Y addresses the green color palette RAM, Cr addresses the red color palette RAM, and Cb addresses the blue color palette RAM. Each lookup table RAM provides 8 bits of information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation). Before addressing the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation), Y has an input range of 16–235. Values less than 16 are made 16, and values greater than 235 are made 235. The Cr and Cb have an input range of 16–240 with 128 equal to zero. Values less than 16 are made 16, and values greater than 240 are made 240.

If overlay information is being displayed (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of YCrCb color information to the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation).

Pseudo-Color Mode

The R0–R7, G0–G7, or B0–B7 inputs (as specified by command bits CR04–CR07) address all three lookup table RAMs simultaneously, generating 24 bits of color information. The OL0–OL3, R0–R7, G0–G7, and B0–B7 inputs are latched on the rising edge of CLOCK_IN. Each lookup table RAM provides 8 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation). If overlay information is being generated (i.e., OL0–OL3 are nonzero), the selected overlay register provides 24 bits of color information to the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Circuit Description—Pixel Input Formats (continued)

RGB Inputs	24-bit RGB (8, 8, 8) Mode	16-bit RGB (5, 6, 5) Mode	16-bit RGB (6, 6, 4) Mode	15-bit RGB (5, 5, 5) Mode	24-bit YCrCb Mode	16-bit YCrCb Mode	Pseudo-Color Mode
R7	R7	R4	R5	x	Cr7	(P7)	P7
R6	R6	R3	R4	R4	Cr6	(P6)	P6
R5	R5	R2	R3	R3	Cr5	(P5)	P5
R4	R4	R1	R2	R2	Cr4	(P4)	P4
R3	R3	R0	R1	R1	Cr3	(P3)	P3
R2	R2	G5	R0	R0	Cr2	(P2)	P2
R1	R1	G4	G5	G4	Cr1	(P1)	P1
R0	R0	G3	G4	G3	Cr0	(P0)	P0
G7	G7	G2	G3	G2	Y7	Y7	P7
G6	G6	G1	G2	G1	Y6	Y6	P6
G5	G5	G0	G1	G0	Y5	Y5	P5
G4	G4	B4	G0	B4	Y4	Y4	P4
G3	G3	B3	B3	B3	Y3	Y3	P3
G2	G2	B2	B2	B2	Y2	Y2	P2
G1	G1	B1	B1	B1	Y1	Y1	P1
G0	G0	B0	B0	B0	Y0	Y0	P0
B7	B7	x	x	x	Cb7	Cb7 / Cr7	P7
B6	B6	x	x	x	Cb6	Cb6 / Cr6	P6
B5	B5	x	x	x	Cb5	Cb5 / Cr5	P5
B4	B4	x	x	x	Cb4	Cb4 / Cr4	P4
B3	B3	x	x	x	Cb3	Cb3 / Cr3	P3
B2	B2	x	x	x	Cb2	Cb2 / Cr2	P2
B1	B1	x	x	x	Cb1	Cb1 / Cr1	P1
B0	B0	x	x	x	Cb0	Cb0 / Cr0	P0

Table 3. Data Input Formats.

Circuit Description—Pixel Input Formats (continued)

Mixed Pseudo-Color/YCrCb Mode

In this mode, 8 bits of pseudo-color data are input via the R0–R7 inputs. The data addresses all three lookup table RAMs simultaneously, generating 24 bits of RGB color information. The RGB data drives the RGB-to-YIQ matrix (NTSC operation) or RGB-to-YUV matrix (PAL operation).

Sixteen bits of 4:2:2 YCrCb digital video are input via the G0–G7 and B0–B7 inputs. (The input timing is the same as that for 16-bit YCrCb mode.) The 16-bit YCrCb (4:2:2) data is converted to 24-bit YCrCb (4:4:4) with a 2-tap interpolation filter to generate the missing Cr and Cb values as follows. (The original Cr and Cb values pass through unchanged.)

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

The resulting YCrCb data drives the YCrCb-to-YIQ matrix (NTSC operation) or YCrCb-to-YUV matrix (PAL operation). YCrCb data does not address the lookup table RAMs.

If the OL0–OL3 inputs are not (0000), the overlay color is output rather than the result of the mixed pseudo-color and YCrCb data (because overlays always take priority).

External Key Switching

The KEY_0 input, in conjunction with command bits CR00 and CR01, determine whether the pseudo-color data or the YCrCb data is selected to be used.

KEY_0 Input	CR00, CR01	Selected Source
0	1, 1	pseudo-color data
0	1, 0	YCrCb data
1	1, 1	YCrCb data
1	1, 0	pseudo-color data
x	0, 0	pseudo-color data
x	0, 1	YCrCb data

KEY_0 is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The KEY_0 input may change on a pixel basis.

The KEY_0 input is ignored unless the command bits CR04–CR07 equal (1100). KEY_0 is also ignored during blanking intervals.

Internal Color Key Switching

The Bt858 also generates an internal COLOR KEY_0 control signal, determined by the color key_0 and color mask_0 registers. For a programmed pseudo color, the COLOR KEY_0 control signal will be either a logical one or a logical zero coincident with the specified color being input on the R0–R7 inputs.

CR25, CR24	Color Key_0 Match	Selected Source
0, 0	yes	YCrCb data
0, 0	no	pseudo-color data
0, 1	yes	pseudo-color data
0, 1	no	YCrCb data
1, x	x	pseudo-color data

The COLOR KEY_0 control signal is pipelined to maintain synchronization with the pixel data.

If either the external color key signal (KEY_0) or the internal color key selects the YCrCb data, YCrCb data is selected. This data format is given in Table 3.

Circuit Description—Video Timing

General Video Timing

The Bt858 is designed to accept and output interlaced video to conform to the NTSC or PAL timing specifications. Interlaced 60 Hz, 525-line digital RGB or YCrCb input will produce standard analog NTSC outputs. Interlaced 50 Hz, 625-line digital RGB or YCrCb input will produce standard analog PAL output. Nonstandard line counts in PAL or NTSC modes are not supported.

The Bt858 automatically calculates the width of the analog horizontal sync pulses, and the start and end of color burst. It automatically disables color burst on appropriate scan lines and automatically generates serration and equalization pulses on appropriate scan lines.

In addition, the rise and fall times of sync, blanking, and the burst envelope are internally controlled to conform to the composite video specifications.

The user must only provide information on the number of pixels per scan line (via the HCOUNT register), and program the P1 and P2 registers to generate the correct color subcarrier frequency for a given pixel clock rate.

During NTSC operation, color burst information is automatically disabled on scan lines 1–6, 261–269, and 523–525, inclusively.

During PAL operation, color burst information is automatically disabled on scan lines 1–6, 310–318, and 622–625 during fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is automatically disabled on scan lines 1–5, 311–319, and 623–625, inclusively.

Master Mode 0

External horizontal sync (HSYNC*), vertical sync (VSYNC*), and composite blanking (BLANK*) must be supplied to the Bt858. HSYNC*, VSYNC*, and BLANK* are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

CR43 programmed low will three-state CSYNC*, HSYNC*, and VSYNC*. CR43 programmed high will enable CSYNC* as a valid composite sync output, but HSYNC* and VSYNC* will still be internally gated to three-state.

Coincident falling edges of the HSYNC* and VSYNC* input indicates the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field and is ignored.

Only the falling edges of HSYNC* and VSYNC* are used. HSYNC* need not be the width of the analog horizontal sync pulse desired. VSYNC* need not be the width of the analog vertical sync pulse desired and must not contain serration or equalization pulses.

Figures 2 and 3 illustrate the video timing for NTSC and PAL. Nonstandard NTSC line numbering is used in Figure 2.

Vertical Timing

Coincident falling edges of VSYNC* and HSYNC* reset the 10-bit vertical counter to $001. (The number one scan line is the first scan line of the vertical sync interval at the beginning of an odd field.) The vertical counter increments on the falling edge of HSYNC*.

The Bt858 will generate 525 scan lines (NTSC operation) or 625 scan lines (PAL operation) per frame, 2:1 interlaced. The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC) or 625 (PAL).

Horizontal Timing

The falling edge of HSYNC* resets a 12-bit horizontal counter to $001. The horizontal counter increments on the rising edge of CLOCK_IN. The counter value is compared to various internal values automatically calculated by the device to determine when to start and stop various control signals (such as horizontal sync and burst gate).

The 12-bit horizontal counter is also reset to $001 upon reaching the count specified by HCOUNT.

NTSC Blanking

The BLANK* input specifies when to output active video. Blanking takes place automatically (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–17, 261–279, and 523–525, inclusively.

On scan line 260 (where the first half of the scan line contains active video), the Bt858 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 280 (where the last half of the scan line contains active video), the Bt858 automatically blanks the first half of the scan line regardless of the value of BLANK*.

Circuit Description—Video Timing (continued)

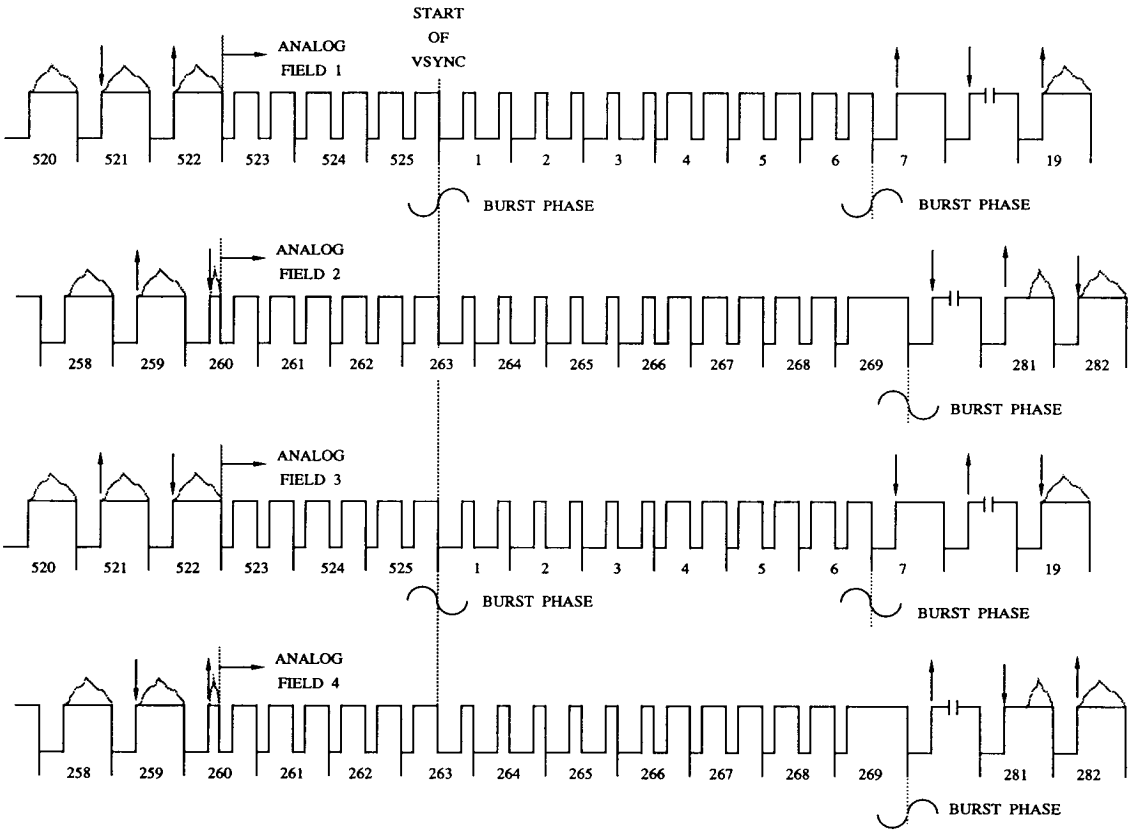
On the remaining scan lines, BLANK* specifies when to display active video. The P2 Low and High Register section contains further information.

PAL Blanking

The BLANK* input specifies when to output active video. Blanking takes place automatically (regardless of the value of BLANK*) for the entire scan line at the beginning of scan lines 1–22, 311–335, and 624–625, inclusively.

On scan line 623 (where the first half of the scan line contains active video), the Bt858 automatically blanks the last half of the scan line regardless of the value of BLANK*. On scan line 23 (where the last half of the scan line contains active video), the Bt858 automatically blanks the first half of the scan line regardless of the value of BLANK*.

On the remaining scan lines, BLANK* specifies when to display active video. The P2 Low and High Register section contains further information.



BURST BEGINS WITH POSITIVE HALF-CYCLE
BURST PHASE = REFERENCE PHASE = 180° RELATIVE TO B - Y

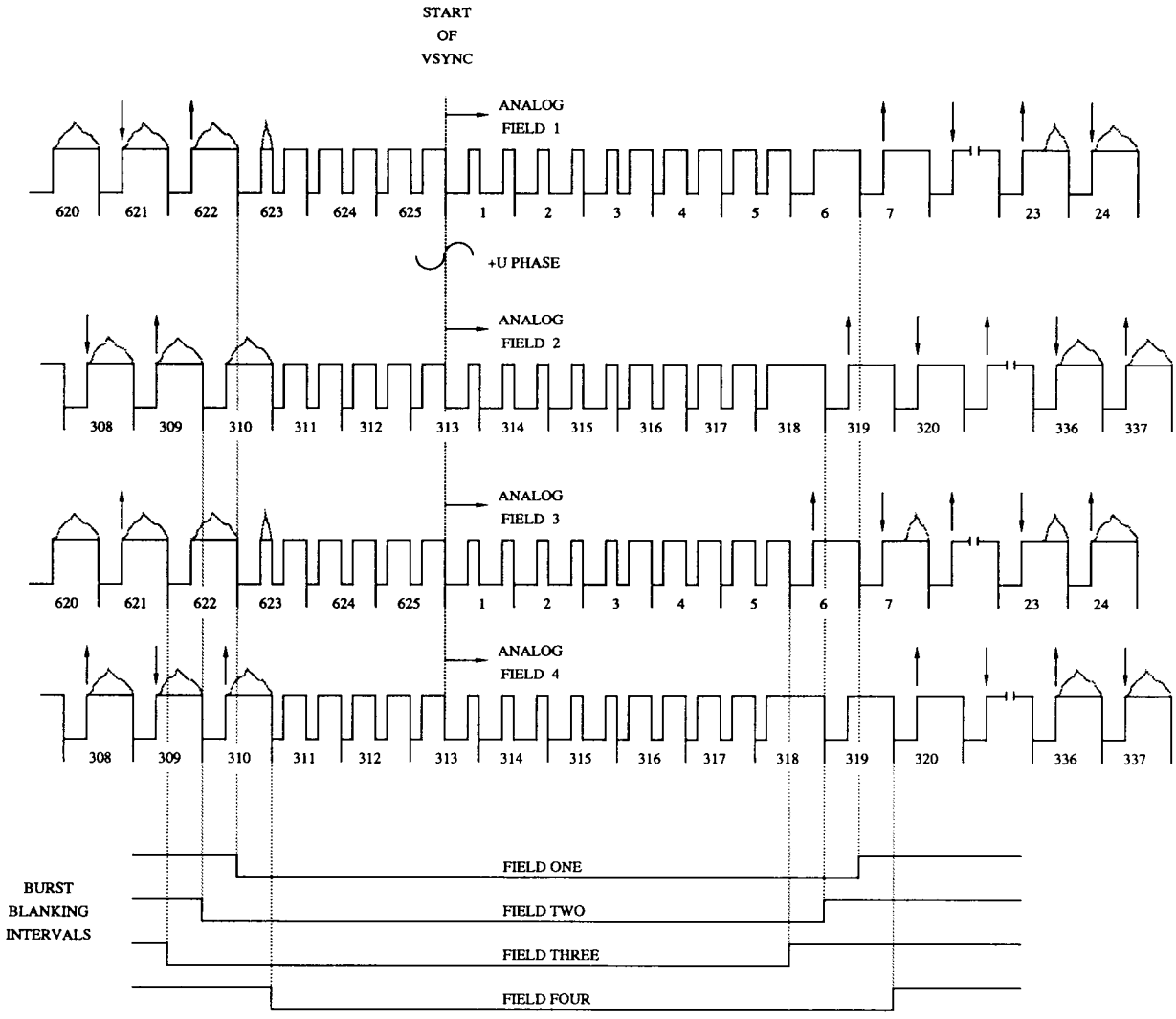
BURST BEGINS WITH NEGATIVE HALF-CYCLE
BURST PHASE = REFERENCE PHASE = 180° RELATIVE TO B - Y

FIELD_0 PIN	
0	FIELD ONE / TWO
1	FIELD THREE / FOUR

To simplify the implementation, the line numbering does not match that used in standard practice for NTSC video signals.

Figure 2. NTSC Video Timing.

Circuit Description—Video Timing (continued)



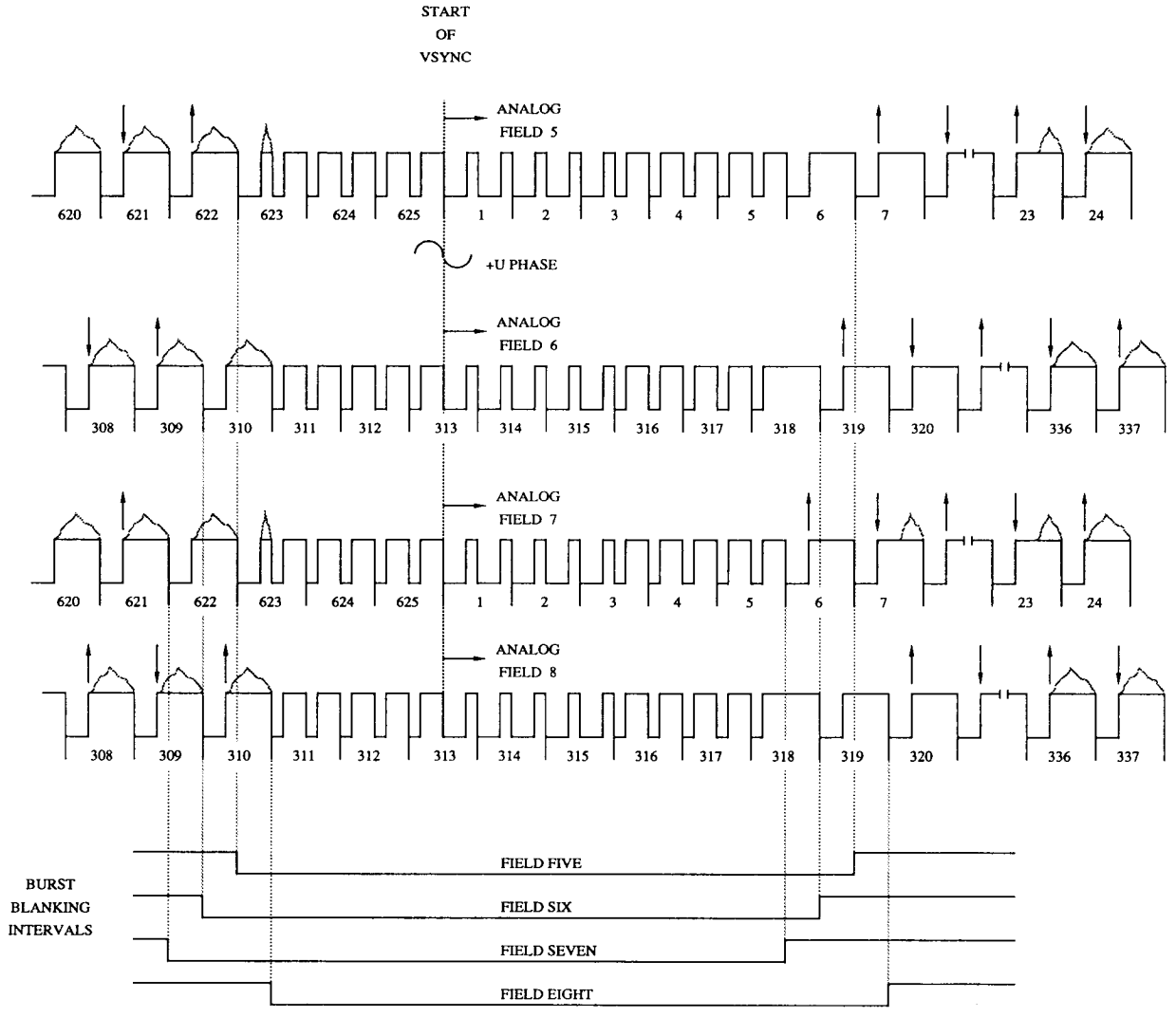
BURST PHASE = REFERENCE PHASE = 135° RELATIVE TO U
PAL SWITCH = 0, +V COMPONENT

BURST PHASE = REFERENCE PHASE + 90° = 225° RELATIVE TO U
PAL SWITCH = 1, –V COMPONENT

FIELD_1 PIN	FIELD_0 PIN	
0	0	FIELD ONE / TWO
0	1	FIELD THREE / FOUR
1	0	FIELD FIVE / SIX
1	1	FIELD SEVEN / EIGHT

Figure 3a. PAL Video Timing.

Circuit Description—Video Timing (continued)



FIELD_1 PIN	FIELD_0 PIN	
0	0	FIELD ONE / TWO
0	1	FIELD THREE / FOUR
1	0	FIELD FIVE / SIX
1	1	FIELD SEVEN / EIGHT

Figure 3b. PAL Video Timing (continued).

Circuit Description—Video Timing (continued)

Master Mode 1

External composite sync (CSYNC*) and composite blanking (BLANK*) must be supplied to the Bt858. CSYNC* and BLANK* are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The HSYNC*/H and VSYNC*/V pins are configured as outputs and three-stated. CR43 must be set low, three-stating all pins CSYNC*, HSYNC*, and VSYNC*.

The composite sync (CSYNC*) information is separated into horizontal and vertical sync information internally. When the horizontal and vertical sync information is separated from the CSYNC* signal, the functionality and timing are the same as that for Master Mode 0.

In this instance, CSYNC* must contain the proper serration and equalization pulses during the vertical retrace intervals for proper operation.

Vertical Timing

If the previous scan line samples of CSYNC* (at one-fourth HCOUNT and three-fourths HCOUNT) were both a logical one and the current scan line sample of CSYNC* (at one-fourth HCOUNT) is a logical zero, it is assumed to be the beginning of an odd field, and the 10-bit vertical counter is reset to $001.

The 10-bit vertical counter is also reset to $001 upon reaching a count of 525 (NTSC operation) or 625 (PAL operation).

Horizontal Timing

After a falling edge of CSYNC* (three-fourths HCOUNT), clock cycles must pass before the next falling edge of CSYNC* is interpreted as a horizontal sync. This filters out any serration and equalization pulses from the composite sync signal. Each gated falling edge resets the horizontal counter to $001.

Master Mode 2

In this mode of operation, the Bt858 is designed to be clocked at 13.5 MHz for digital component video (i.e., CCIR601) applications that use the H (horizontal blanking), V (vertical blanking), and F (even/odd field) control signals.

External horizontal blank (H), vertical blank (V), and even/odd field (F) information must be supplied to the Bt858. The H, V, and F pins are configured as inputs. They are latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While either the H or V input is a logical one, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an output and three-stated.

As in Master Mode 0, H and V are internally gated to three-state, and CR43 configures only CSYNC* as an unused input or a valid CSYNC* output.

The horizontal counter is reset to $001, 63 clock cycles after each rising edge of H (horizontal blanking).

The F (field) input is sampled by horizontal sync. When a falling edge of the F input (while both the H and V inputs are a logical one) has been detected, the vertical counter is reset to $001. Thus, while F is a logical zero, an odd field is generated; while F is a logical one, an even field is generated.

The remaining functionality is the same as that for Master Mode 0.

Master Mode 3

Master Mode 3 is similar to Master Mode 0, except that the Bt858 generates and outputs horizontal sync (HSYNC*) and vertical sync (VSYNC*). Composite blanking (BLANK*) must be supplied to the Bt858. HSYNC* and VSYNC* are output following the rising edge of CLOCK_IN. HSYNC* and VSYNC* are asserted for one clock cycle when the horizontal and vertical counters overflow after reaching the value of HCOUNT, and 525 (NTSC) or 625 (PAL).

Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

BLANK* is an input. It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. While the BLANK* input is a logical zero, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored. The CSYNC* pin is configured as an input and is ignored.

Circuit Description—Video Timing (continued)

FIELD_0 and FIELD_1 Pins

The FIELD_0 and FIELD_1 pins, in conjunction with the HSYNC* and VSYNC* timing relationship (or the F input if the BLANK* input is not required), determine which one of four fields (NTSC) or eight fields (PAL) is being generated.

Even or odd fields may be determined by the HSYNC* and VSYNC* timing relationship. Coincident falling edges of HSYNC* and VSYNC* indicate the beginning of an odd field. A falling edge of VSYNC* without a coincident falling edge of HSYNC* indicates the beginning of an even field.

NTSC

If command bit CR45 is a logical zero, the FIELD_0 pin is configured as an input and is latched on the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether to generate fields one and two (logical zero) or fields three and four (logical one) (see Figure 4). As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

If command bit CR45 is a logical one, the FIELD_0 pin is configured as an output, and is output following the rising edge of CLOCK_IN. The FIELD_0 pin indicates whether fields one and two (logical zero) or fields three and four (logical one) are being generated. As an output, the FIELD_0 pin changes state at the beginning of vertical sync during fields one and three. The FIELD_1 pin is configured as an input and is ignored.

PAL

If command bit CR45 is a logical zero, the FIELD_0 and FIELD_1 pins are configured as inputs and are latched on the rising edge of CLOCK_IN. The FIELD_0 and FIELD_1 pins indicate which field to generate, as shown in Figure 5.
As an input, the FIELD_0 pin should change state only at the beginning of vertical sync during fields one, three, five, and seven. The FIELD_1 pin should change state only at the beginning of vertical sync during fields one and five.

If command bit CR45 is a logical one, the FIELD_0 and FIELD_1 pins are configured as outputs and are output following the rising edge of CLOCK_IN. As an output, FIELD_0 changes state at the beginning of vertical sync during fields one, three, five, and seven. FIELD_1 changes state at the beginning of vertical sync during fields one and five.

Analog Outputs

All of the analog outputs have DC offsets; therefore, they should be AC coupled to the receiving equipment or circuitry. The D/A converter values for 100-percent saturation, 100-percent amplitude color bars are shown in in Figures 6–9.

The Bt858 is configured to drive into a 50 Ω load, and the analog lowpass filter is designed to provide the proper 75 Ω output impedance.

Luminance (Y) Analog Output

The digital composite Y information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x/x D/A converter frequency roll-off.

The result drives the 10-bit D/A converter that generates the analog Y video output (see Figures 4 and 5, and Tables 4 and 5). The Y analog output is designed to drive a 50 Ω load (maximum).

Chrominance (C) Analog Output

The digital chrominance information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x/x D/A converter frequency roll-off.

The result drives the 10-bit D/A converter that generates the analog C video output (see Figures 6 and 7, and Tables 6 and 7). The C analog output is designed to drive a 50 Ω load.

NTSC/PAL Analog Output

The composite video information is optionally processed by a digital $(\sin x/x)^{-1}$ correction filter to compensate for the inherent sin x./ D/A converter frequency roll-off.

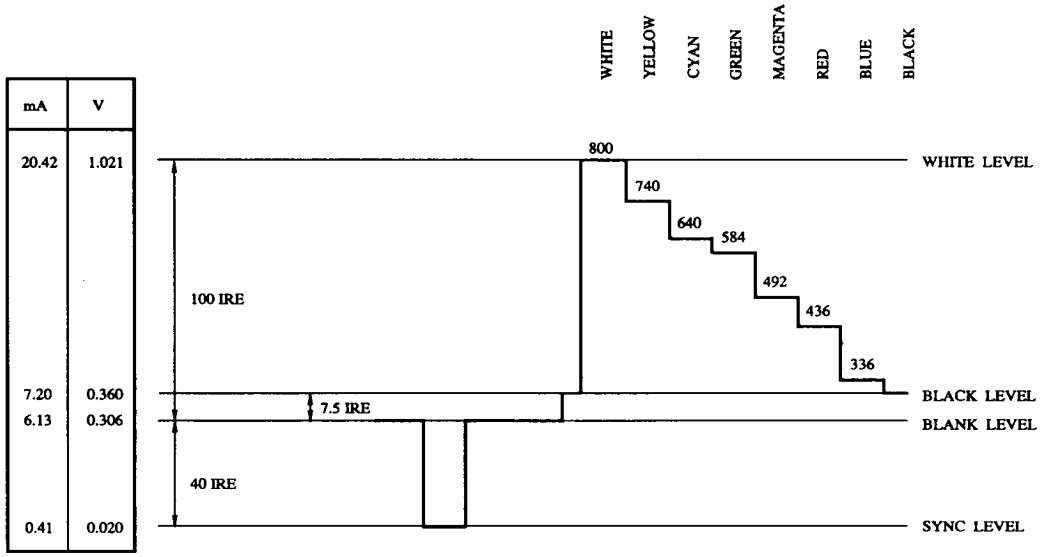
The result drives the 10-bit D/A converter that generates the composite analog NTSC/PAL video output (see Figures 8 and 9, and Tables 8 and 9). The NTSC/PAL analog output is designed to drive a 50 Ω load.

Black Burst Operation

The Bt858 may be configured to generate black burst video signals, as shown in Figures 10 and 11 and listed in Tables 10 and 11.

The black burst video signal contains sync, blank, and burst information only (no active video).

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. RS-170 levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude luminance color bars are shown.

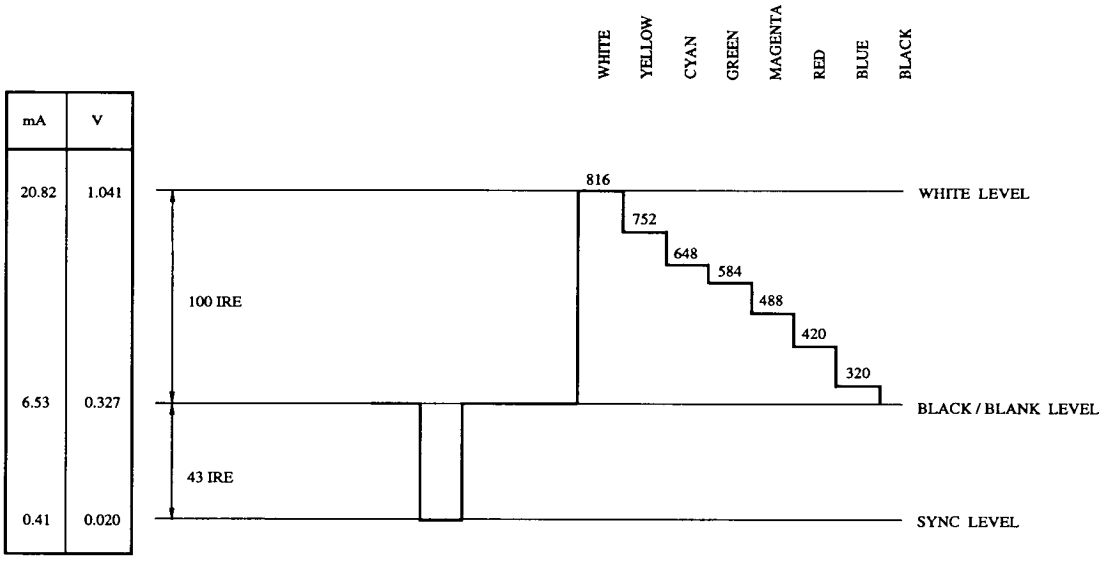
Figure 4. NTSC Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.42	1	1	800
BLACK	7.2	1	1	282
BLANK	6.13	1	0	240
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 4. NTSC Y (Luminance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. RS-170 levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude luminance color bars are shown.

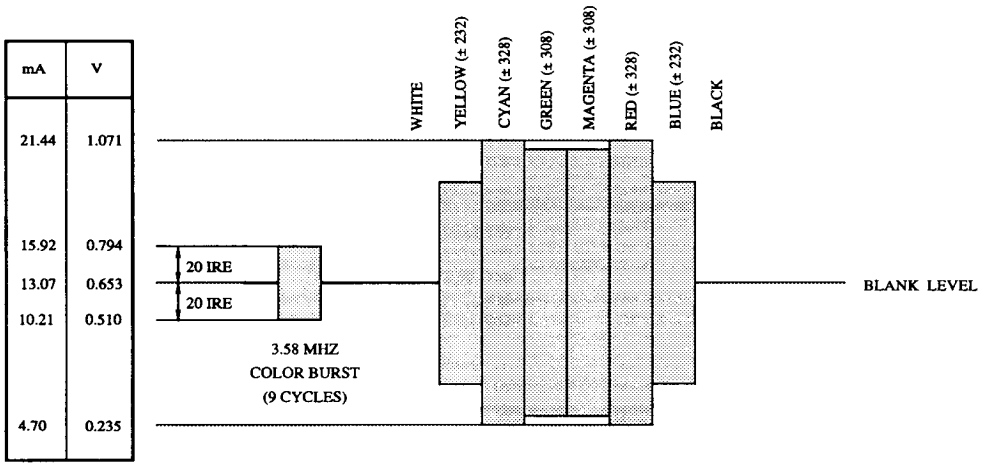
Figure 5. PAL Y (Luminance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
WHITE	20.82	1	1	816
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 Vand RSET = 98.8 Ω.

Table 5. PAL Y (Luminance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. RS-170A levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude chrominance color bars are shown.

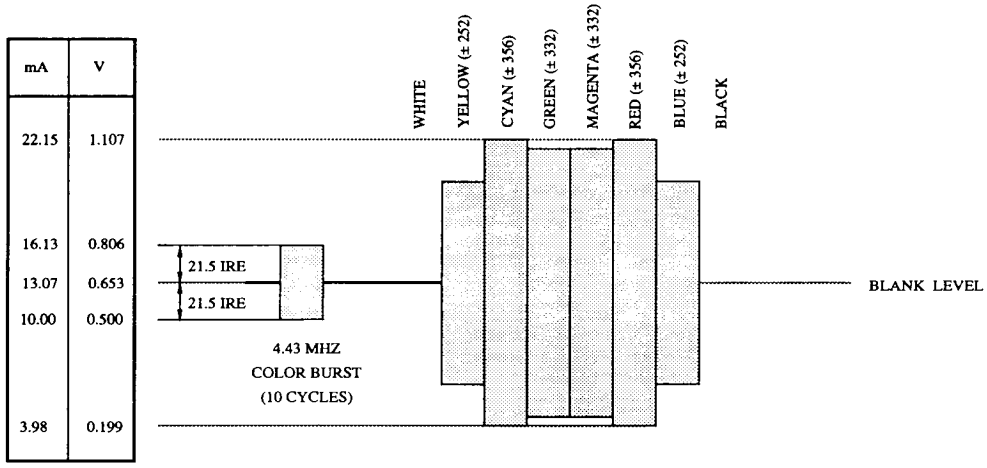
Figure 6. NTSC C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	21.44	x	1	840
Burst (high)	15.92	x	0	624
BLANK	13.07	x	0	512
Burst (low)	10.21	x	0	400
Peak Chroma	4.7	x	1	184

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 6. NTSC C (Chrominance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. PAL levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude chrominance color bars are shown.

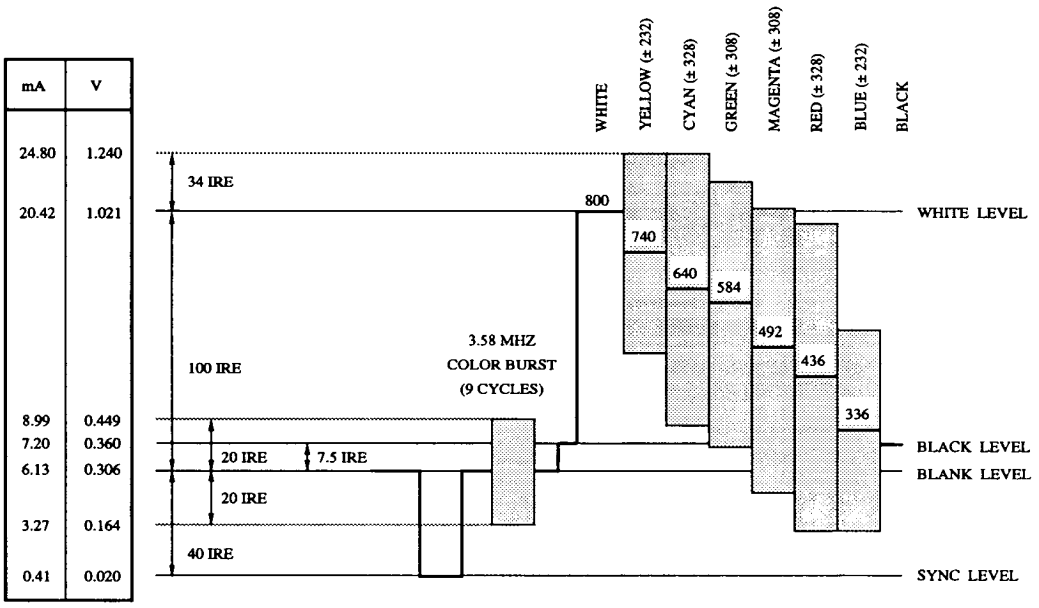
Figure 7. PAL C (Chrominance) Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	22.15	x	1	868
Burst (high)	16.13	x	0	632
BLANK	13.07	x	0	512
Burst (low)	10	x	0	392
Peak Chroma	3.98	x	1	156

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 7. PAL C (Chrominance) Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. RS-170A levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude color bars are shown.

Figure 8. Composite NTSC Video Output Waveform.

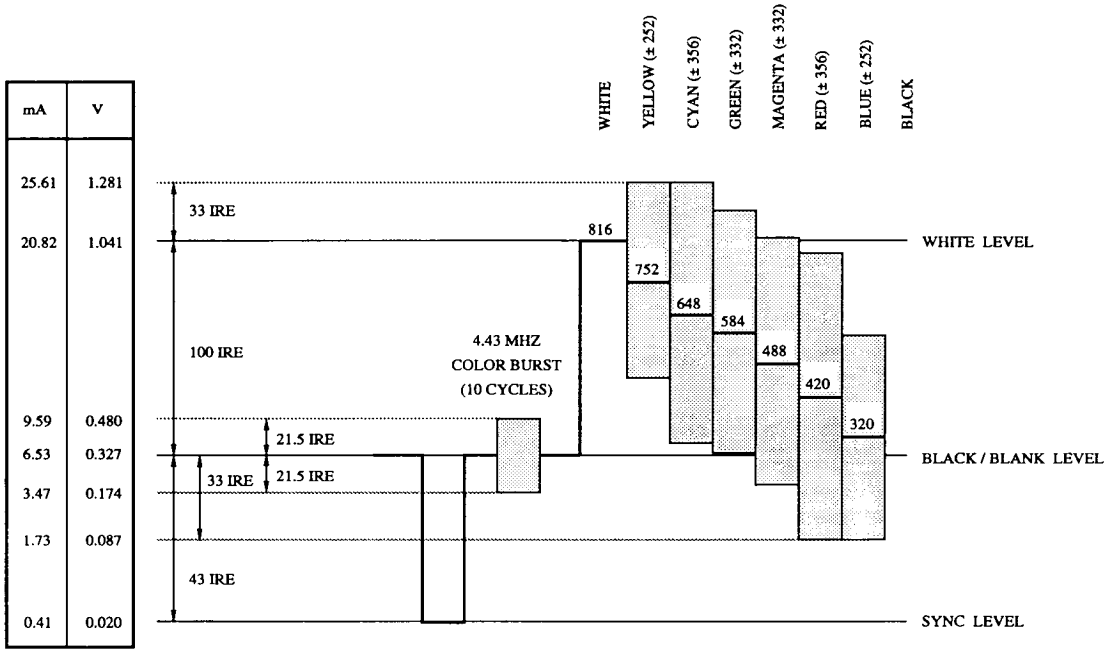
Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	24.80	1	1	972
WHITE	20.42	1	1	800
Burst (high)	8.99	1	0	352
BLACK	7.20	1	1	282
BLANK	6.13	1	0	240
Burst (low)	3.27	1	0	128
Peak Chroma (Note 1)	2.66	1	1	104
SYNC	0.41	0	0	16

Note 1: If command bit CR31 is a logical zero, DAC data values less than 127 are made 127.

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 8. Composite NTSC Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. PAL levels and tolerances are assumed on all levels. One-hundred-percent saturation and 100-percent amplitude color bars are shown.

Figure 9. Composite PAL Video Output Waveform.

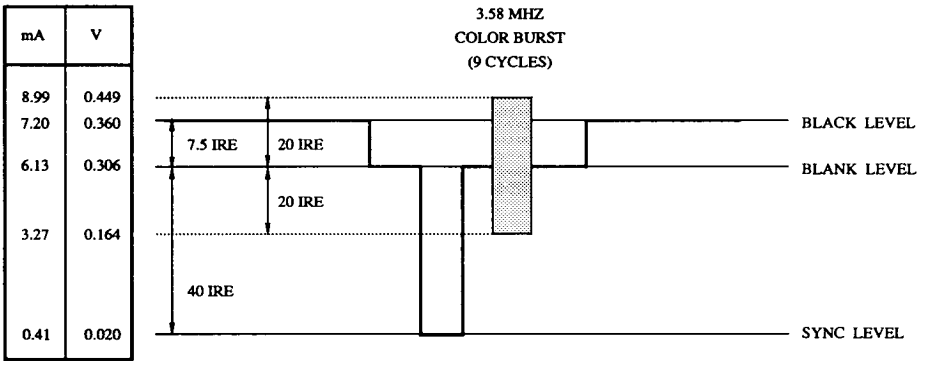
Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Peak Chroma	25.61	1	1	1004
WHITE	20.82	1	1	816
Burst (high)	9.59	1	0	376
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
Burst (low)	3.47	1	0	136
Peak Chroma (Note 1)	1.73	1	1	68
SYNC	0.41	0	0	16

Note 1: If command bit CR31 is a logical zero, DAC data values less than 127 are made 127.

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 9. Composite PAL Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. RS-170A levels and tolerances are assumed on all levels.

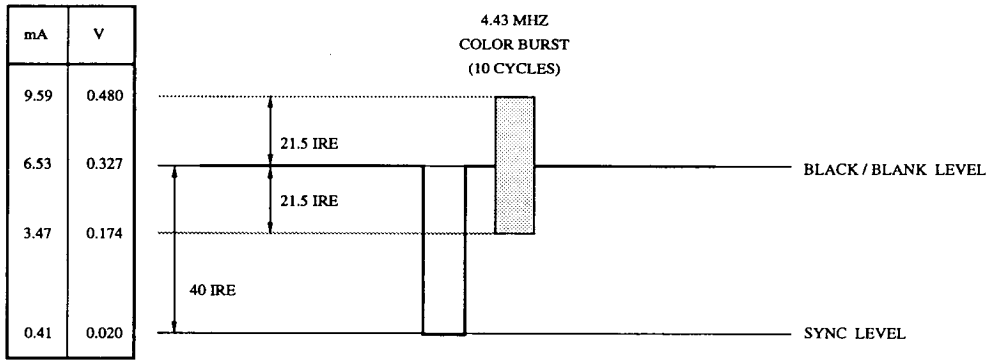
Figure 10. NTSC Black Burst Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Burst (high)	8.99	1	0	352
BLACK	7.20	1	1	282
BLANK	6.13	1	0	240
Burst (low)	3.27	1	0	128
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 98.8 Ω.

Table 10. NTSC Black Burst Video Output Truth Table.

Circuit Description—Video Timing (continued)



Note: 50 Ω load, VREF = 1.235 V, and RSET = 98.8 Ω. PAL levels and tolerances are assumed on all levels.

Figure 11. PAL Black Burst Video Output Waveform.

Description	Iout (mA)	CSYNC*	BLANK*	DAC Data
Burst (high)	9.59	1	0	376
BLACK	6.53	1	1	256
BLANK	6.53	1	0	256
Burst (low)	3.47	1	0	136
SYNC	0.41	0	0	16

Note: Typical with VREF = 1.235 V and RSET = 98.8Ω.

Table 11. PAL Black Burst Video Output Truth Table.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time, and is initialized to $00 following a reset sequence. CR00 is the least significant bit and corresponds to data bus bit D0.

CR07–CR04 Color data input format

(0000) 24-bit true-color RGB (8,8,8)
(0001) 16-bit true-color RGB (6,6,4)
(0010) 16-bit true-color RGB (5,6,5)
(0011) 15-bit true-color RGB (5,5,5)
(0100) 8-bit pseudo-color (red)
(0101) 8-bit pseudo-color (green)
(0110) 8-bit pseudo-color (blue)
(0111) reserved
(1000) reserved
(1001) 24-bit YCrCb (4:4:4)
(1010) 16-bit YCrCb (4:2:2)
(1011) reserved
(1100) mixed VGA / YCrCb
(1101) reserved
(1110) reserved
(1111) reserved

These bits specify the input format of the video data, as listed in Table 3. The pipeline delay remains unchanged regardless of the mode of operation.

YCrCb data is assumed to be derived from gamma-corrected RGB data. The lookup table RAMs may be used to provide gamma correction (typically 2.2 for NTSC and 2.8 for PAL) when RGB or pseudo-color data is being input. If the lookup table RAMs are bypassed, RGB input data should be gamma corrected.

CR03, CR02 reserved

CR01, CR00 KEY_0 read mask

(00) force KEY_0 data to zero
(01) force KEY_0 data to one
(10) invert KEY_0 input data
(11) pass KEY_0 input data

These bits either force the KEY_0 input value to a logical zero or logical one, invert the KEY_0 input value, or let it pass unchanged. These bits are ignored unless CR07–CR04 are (1100).

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time, and is initialized to $00 following a reset sequence. CR10 is the least significant bit and corresponds to data bus bit D0.

CR17	OL3 read mask (0) force OL3 data to zero (1) pass OL3 data	This bit is logically ANDed with the OL3 input prior to addressing the overlay registers.
CR16	OL2 read mask (0) force OL2 data to zero (1) pass OL2 data	This bit is logically ANDed with the OL2 input prior to addressing the overlay registers.
CR15	OL1 read mask (0) force OL1 data to zero (1) pass OL1 data	This bit is logically ANDed with the OL1 input prior to addressing the overlay registers.
CR14	OL0 read mask (0) force OL0 data to zero (1) pass OL0 data	This bit is logically ANDed with the OL0 input prior to addressing the overlay registers.
CR13	8-bit/6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle when the lookup table RAMs are being accessed. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles. D6 and D7 are ignored during color write cycles and a logical zero during color read cycles. In the 6-bit mode, the full-scale output current will be about 1.5-percent lower than when in the 8-bit mode. This is because the 2 LSBs of color data are logical zeros in the 6-bit mode.
CR12	Lookup table RAM bypass enable (0) use lookup table RAMs (1) bypass RAMs	This bit specifies whether to bypass the lookup table RAMs and pixel read mask registers. When internal color bar generation is used (CR32 equals 1), the lookup table RAMs are automatically bypassed regardless of the value of this bit. The selection does not affect the pipeline delay through the device.
CR11, CR10	Reserved	

Internal Registers (continued)

Command Register_2

This command register may be written to or read by the MPU at any time, and is initialized to $F0 following a reset sequence. CR20 is the least significant bit and corresponds to data bus bit D0.

CR27, CR26 — Reserved (logical one)

CR25, CR24 — COLOR KEY_0 invert

- (00) normal value
- (01) invert value
- (10) reserved
- (11) disable color key_0

These bits specify whether to invert the COLOR KEY_0 value generated by the color key_0 and color mask_0 registers. These bits are ignored unless CR07–CR04 are (1100).

CR23 — Reserved (logical zero)

CR22 — Software reset

- (0) normal operation
- (1) reset device

Writing a logical one to this bit resets the device, clearing the pixel pipeline and resetting the command register bits to their initialized state (equivalent to asserting the RESET* input pin). The bit is reset to a logical zero when the software reset sequence is complete.

Following a reset condition, the Bt858 is configured for NTSC operation (square pixels, Master Mode_1) and 24-bit RGB input data format. The lookup table RAMs must be initialized before valid video may be generated.

CR21, CR20 — Y / C output select

- (00) normal video
- (01) black burst video
- (10) composite video
- (11) reserved

The (00) specifies that the Y and C outputs generate normal luminance (Y) and chroma (C) video.

The (01) specifies that both the Y and C outputs generate black burst video (sync, blank, and burst, only).

The (10) specifies that both the Y and C outputs generate composite NTSC/PAL video (the same as the NTSC/PAL output) to drive multiple monitors and tape recorders.

Internal Registers (continued)

Command Register_3

This command register may be written to or read by the MPU at any time, and is initialized to $12 following a reset sequence. CR30 is the least significant bit and corresponds to data bus bit D0.

CR37–CR34 Output mode select

(0000) NTSC master mode 0
(0001) NTSC master mode 1
(0010) NTSC master mode 2
(0011) NTSC master mode 3
(0100) reserved
(0101) PAL master mode 0
(0110) PAL master mode 1
(0111) PAL master mode 2
(1000) PAL master mode 3
(1001) reserved
(1010) reserved
: :
(1110) reserved
(1111) power-down mode

These bits specify the timing and analog output mode of the Bt858.

Mode (1111) turns power off to the DACs and the A/D converter by disabling the output current. It also three-states all TTL-compatible outputs and inhibits clocking to most of the internal circuitry to minimize power consumption. The pixel and control inputs are ignored, and CLOCK_IN is directly output onto CLOCK_OUT. All the control registers and color palette RAMs are still accessible by the MPU. The Bt858 becomes operational about 1 second after the power-down mode is disabled.

CR33 Color kill enable

(0) normal operation
(1) disable color information

This bit enables (logical zero) or disables (logical one) color information on the NTSC/PAL and C video outputs.

CR32 Color bar test enable

(0) normal operation
(1) generate color bars

If this bit is a logical one and the full screen is 100-percent saturated, 75-percent amplitude color bars are generated, consisting of gray, yellow, cyan, green, magenta, red, blue, and black. The first seven colors each occupy 64 pixels of active video each scan line. Black occupies the remaining active pixels each scan line. BLANK* must be negated at the proper time in order to view the color bar output. The input format must be programmed to 24-bit RGB.

CR31 Color level limiting bypass

(0) use level limiting
(1) bypass level limiting

A logical zero enables the NTSC / PAL level limiting circuitry that limits the minimum active composite video levels. Active video values less than 127 (10-bit value) are made 127 (approximately half the sync height) to avoid possible sync detection problems with downstream video equipment.

CR30 Illegal video flag

(0) reset by MPU
(1) illegal value detected

This bit is set to a logical one if active video generates a value less than 127 (10-bit value). The MPU must write a logical zero to this bit to clear it to a logical zero.

Internal Registers (continued)

Command Register_4

This command register may be written to or read by the MPU at any time, and is initialized to $18 following a reset sequence. CR40 is the least significant bit and corresponds to data bus bit D0.

CR47 — IQ/UV low-pass filter bypass

(0) use filters
(1) bypass filters

This bit specifies whether to bypass the IQ and UV low-pass filters (just after the matrix). Regardless of the selection, there is no change in the pipeline delay.

CR46 — $(\text{Sin } x/x)^{-1}$ correction filter bypass

(0) use filters
(1) bypass filters

This bit specifies whether to bypass the $(\text{sin } x/x)^{-1}$ correction filters just prior to the analog outputs. Regardless of the selection, there is no change in the pipeline delay.

CR45 — FIELD input/output select

(0) inputs
(1) outputs

This bit specifies whether the FIELD_0 and FIELD_1 pins are inputs (logical zero) or outputs (logical one). In all modes, FIELD_0 and FIELD_1 are three-stated if CR45 is programmed low.

CR44 — CLOCK_OUT output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the CLOCK_OUT pin asynchronously to the pixel clock.

CR43 — Control output enable

(0) output three-stated
(1) output enabled

A logical zero three-states the FIELD_0, FIELD_1, CSYNC*, HSYNC*, and VSYNC* pins, if they are configured as outputs, asynchronously to the pixel clock. *For HSYNC*, VSYNC*, FIELD_0, and FIELD_1, this three-state is independent of the mode of operation. The CSYNC* pin is not internally gated and must be configured by CR43 according to the mode for proper operation of the part. In all modes, FIELD_0 and FIELD_1 are three-stated if CR43 is programmed low.*

CR43: H/L	CSYNC*	V/VSYNC*	H/HSYNC*
mode 0	Q/Z	Z	Z
mode 1	X/Z	X/Z	X/Z
mode 2	Q/Z	Z	Z
mode 3	Q/Z	Q/Z	Q/Z

Z = Three-State
X = State Not Allowed in Mode
Q = Valid Output

CR42–CR41 — reserved (logical zero)

CR40 — Genlock availablility status

(0) genlock unavailable
(1) genlock available

This bit indicates whether the device has genlock support. On the Bt858, this bit is always a logical zero, indicating genlock is not supported. MPU write cycles to this bit are ignored.

Internal Registers (continued)

HCOUNT Register

This 16-bit register specifies the number of pixels per scan line. It is initialized to $030C (780) following a reset condition and may be written to and read by the MPU at any time. The HCOUNT low and high registers are independent and are individually written to and read by the MPU.

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. The D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. Even values from $0002 (2) to $0FFE (4094) may be specified.

	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

The HCOUNT value automatically calculates many of the horizontal timing parameters. Using the falling edge of horizontal sync as a reference, the following are internally calculated:

analog horizontal sync width (50% amplitude) = (HCOUNT/16) + (HCOUNT/128) + (HCOUNT/256) + 1

start of color burst (50% amplitude) = (HCOUNT/16) + (HCOUNT/64) + (HCOUNT/256) + (HCOUNT/512) + 1

end of color burst (NTSC, 50% amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/128) + 1

end of color burst (PAL, 50% amplitude) = BURST GATE start value + (HCOUNT/32) + (HCOUNT/256) + 1

Fsc Phase Adjust Register

This 16-bit register specifies the amount of phase shift to add to the subcarrier. This may be used to adjust the subcarrier phase generated by the Bt858 to match that of an external source. It is initialized to $0000 (0) following a reset condition and may be written to and read by the MPU at any time. The Fsc phase adjust low and high registers are independent and are individually written to and read by the MPU.

The Fsc phase adjust low and high registers are cascaded to form a 16-bit Fsc phase adjust register. The D3–D7 of Fsc phase adjust high are ignored during MPU write cycles and return a logical zero during MPU read cycles. Values from $0000 (0°) to $07FF (360°) may be specified.

	Fsc Phase Adjust High			Fsc Phase Adjust Low							
Data Bit	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Internal Registers (continued)

P1 and P2 generate the color subcarrier (3.58 MHz for [M] NTSC, 4.43 MHz for [B, D, G, H, I] PAL) from the pixel clock. They must be calculated and the values loaded into the P1 and P2 registers.

P1 Low and High Registers

The P1 low and high registers are cascaded to form a 16-bit P1 register. Values from $0000 (0) to $0400 (1024) may be specified. The 16-bit register is initialized to $0255 (597) following a reset condition and may be written to and read by the MPU at any time. The P1 low and high registers are independent and are individually written to and read by the MPU. The D2–D7 of P1 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P1 High		P1 Low							
Data Bit	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P2 Low and High Registers

The P2 low and high registers are cascaded to form a 16-bit P2 register. Values from $0000 (0) to $1000 (4096) may be specified. The 16-bit register is initialized to $0410 (1040) following a reset condition and may be written to and read by the MPU at any time. The P2 low and high registers are independent and are individually written to and read by the MPU. The D4–D7 of P2 high are ignored during MPU write cycles and return a logical zero during MPU read cycles.

	P2 High				P2 Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

P1 (Fsc) and P2 (Fsc) are calculated as follows:

$$\text{(M) NTSC: } \frac{465{,}920}{\text{HCOUNT}} = \text{P1} + \frac{\text{P2}}{4 \times \text{HCOUNT}}$$

$$\text{(B, D, G, H, I) PAL: } \frac{581{,}123.2768}{\text{HCOUNT}} = \text{P1} + \frac{\text{P2}}{4 \times \text{HCOUNT}}$$

$$\text{(N) PAL: } \frac{469{,}507.2768}{\text{HCOUNT}} = \text{P1} + \frac{\text{P2}}{4 \times \text{HCOUNT}}$$

$$\text{(4.43) NTSC (Note 1): } \frac{577{,}087.69}{\text{HCOUNT}} = \text{P1} + \frac{\text{P2}}{4 \times \text{HCOUNT}}$$

After the appropriate value for HCOUNT value is inserted, the result is separated into an integer value (P1) and a fractional value (whose numerator is P2). Table 12 lists some of the common HCOUNT values and the resulting P1 and P2 values. Table 13 lists some of the common blanking intervals.

Note 1: (4.43) NTSC is NTSC using a 4.43 MHz subcarrier. It is normally used for standards conversion between PAL and NTSC video signals.

Internal Registers (continued)

Color Key_0 Register

The 8-bit color key_0 register may be written to or read by the MPU at any time and is initialized to $00 following a reset condition. Data bit D0 is the least significant bit and corresponds to the R0 input bit.

The color key_0 register is compared to the R0–R7 inputs. If all unmasked bits match, the COLOR KEY_0 control signal is a logical one. This register is used only when CR07–CR04 equals (1100).

Color Mask_0 Register

The 8-bit color mask_0 register may be written to or read by the MPU at any time and is initialized to $FF following a reset condition. Data bit D0 is the least significant bit and corresponds to the R0 input bit.

A logical zero specifies that the corresponding R0–R7 input bit is to be compared against the corresponding bit in the color key_0 register. A logical one specifies that no comparison for the corresponding bit is to take place and is not used in the generation of the COLOR KEY_0 control signal. This register is used only when CR07–CR04 equals (1100).

Typical Application	Total Pixels per Scan Line (HCOUNT)	Active Pixels	4x HCOUNT	P1	P2
13.5 MHz NTSC	858	720	3432	543	104
13.5 MHz PAL	864	720	3456	672	2061
12.27 MHz (square pixels) NTSC	780	640	3120	597	1040
14.75 MHz (square pixels) PAL	944	768	3776	615	2253
14.32 MHz (4x Fsc) NTSC	910	768	3640	512	0
17.72 MHz (4x Fsc) PAL	1135	910	4540	512	0

NTSC refers to (M) NTSC; PAL refers to (B, D, G, H, I) PAL.

Table 12. Typical HCOUNT, P1, and P2 Values.

Typical Application	Sync + Back Porch Blanking (Pixels)	Front Porch Blanking (Pixels)
13.5 MHz NTSC	121	17
13.5 MHz PAL	131	13
12.27 MHz (square pixels) NTSC	118	22
14.75 MHz (square pixels) PAL	145	31
14.32 MHz (4x Fsc) NTSC	120	22
17.72 MHz (4x Fsc) PAL	159	28

NTSC refers to (M) NTSC; PAL refers to (B, D, G, H, I) PAL.

Table 13. Typical BLANK* Input Horizontal Timing.

Pin Descriptions

Pin Name	Description
F/BLANK*	Composite blank control input (TTL compatible). BLANK* is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In all modes, except Master Mode 2, the R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while BLANK* is a logical zero. In Master Mode 2, this pin is the F (field) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. This input must be asserted with the proper timing in all modes.
H/HSYNC*	Horizontal sync control input/output (TTL compatible). In Master Mode 0, HSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the H (horizontal blank) input. This pin is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, HSYNC* is an output. HSYNC* is output following the rising edge of CLOCK_IN. As an output, it should drive a maximum of one LS TTL load. Absolute minimum loading should be observed. When HSYNC* is programmed as an input, the period must match the programmed HCOUNT value.
V/VSYNC*	Vertical sync control input/output (TTL compatible). In master mode 0, VSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Mode 1, this pin is ignored. In Master Mode 2, this pin is the V (vertical blank) input. The V input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. The R0–R7, G0–G7, B0–B7, OL0–OL3, and KEY_0 inputs are ignored while the H or V inputs are a logical one. In Master Mode 3, VSYNC* is an output. VSYNC* is output following the rising edge of CLOCK_IN. As an output, VSYNC* should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
CSYNC*	Composite sync control input/output (TTL compatible). In Master Mode 1, CSYNC* is an input. The input is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. In Master Modes 0, 2, and 3, this pin is ignored.
FIELD_0, FIELD_1	FIELD inputs/outputs (TTL compatible). As inputs, these pins are latched on the rising edge of CLOCK_IN. As outputs, they are output following the rising edge of CLOCK_IN and should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
R0–R7, G0–G7, B0–B7	Pixel inputs (TTL compatible). They are latched on the rising edge of CLOCK_IN. Unused inputs should be connected to GND.
OL0–OL3	Overlay select input (TTL compatible). These inputs specify, on a pixel basis, which overlay color (if any) is to be generated. They are latched on the rising edge of CLOCK_IN, and pipelined to maintain synchronization with the pixel data. Unused inputs should be connected to GND.
KEY_0	Key control input (TTL compatible). It is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. If unused, this pin should be connected to GND. This input is ignored unless command bits CR07–CR04 are (1100).

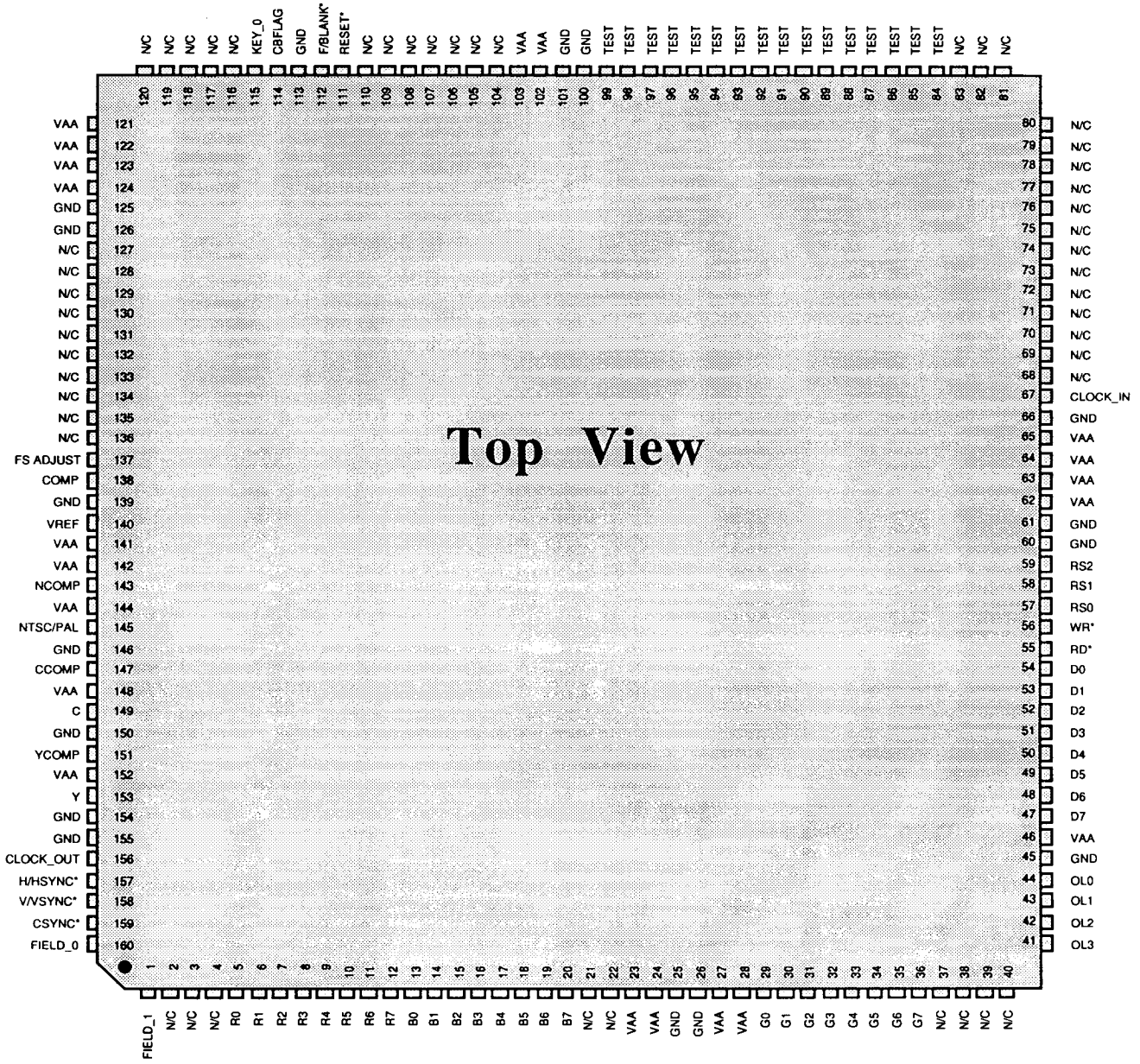
Pin Descriptions (continued)

Pin Name	Description
CLOCK_IN	Pixel clock input (TTL compatible). This clock input is output onto the CLOCK_OUT pin when enabled by CR43.
CLOCK_OUT	Pixel clock output (TTL compatible). This pin should drive a maximum of one LS TTL load. Absolute minimum loading should be observed.
CbFLAG	CbFLAG control input (TTL compatible). When inputting 16-bit YCrCb pixel data, this input indicates whether Cb (logical one) or Cr (logical zero) data is present on the B0–B7 inputs. CBFLAG is latched on the rising edge of CLOCK_IN and pipelined to maintain synchronization with the pixel data. If unused, this pin should be connected to GND.
NTSC/PAL, Y, C	Composite NTSC/PAL, luminance, and chroma current outputs. These high-impedance current sources can drive a 50 Ω load (see Figure 12 in the PC Board Layout section).
COMP, NCOMP, YCOMP, CCOMP	Compensation pins. A 0.1 µF ceramic capacitor must be used to bypass each pin (except COMP) to VAA. Each capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. All pins must also be connected together as close to the device as possible.
VREF	Voltage reference input. An external voltage reference must supply this input with a 1.235 V (typical) reference. A 0.1 µF ceramic capacitor must be used to decouple this input to GND, as shown in Figure 12. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
FS ADJUST	Full-scale adjust control pin. A resistor (RSET) connected between this pin and GND controls the full-scale output current on the NTSC/PAL, Y, and C outputs. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = 2086 * VREF (V) / Iout (mA)
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as specified in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
RESET*	Reset control input (TTL compatible). A logical zero for a minimum of three pixel clock cycles initializes the device. RESET* must be a logical one for normal operation. It is latched on the rising edge of CLOCK_IN.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Number	Signal
1	FIELD_1
2	N/C
3	N/C
4	N/C
5	R0
6	R1
7	R2
8	R3
9	R4
10	R5
11	R6
12	R7
13	B0
14	B1
15	B2
16	B3
17	B4
18	B5
19	B6
20	B7
21	N/C
22	N/C
23	VAA
24	VAA
25	GND
26	GND
27	VAA
28	VAA
29	G0
30	G1
31	G2
32	G3
33	G4
34	G5
35	G6
36	G7
37	N/C
38	N/C
39	N/C
40	N/C
41	OL3
42	OL2
43	OL1
44	OL0
45	GND
46	VAA
47	D7
48	D6
49	D5
50	D4
51	D3
52	D2
53	D1
54	D0
55	RD*
56	WR*
57	RS0
58	RS1
59	RS2
60	GND
61	GND
62	VAA
63	VAA
64	VAA
65	VAA
66	GND
67	CLOCK_IN
68	N/C
69	N/C
70	N/C
71	N/C
72	N/C
73	N/C
74	N/C
75	N/C
76	N/C
77	N/C
78	N/C
79	N/C
80	N/C
81	N/C
82	N/C
83	N/C
84	TEST
85	TEST
86	TEST
87	TEST
88	TEST
89	TEST
90	TEST
91	TEST
92	TEST
93	TEST
94	TEST
95	TEST
96	TEST
97	TEST
98	TEST
99	TEST
100	GND
101	GND
102	VAA
103	VAA
104	N/C
105	N/C
106	N/C
107	N/C
108	N/C
109	N/C
110	N/C
111	RESET
112	F/BLANK*
113	GND
114	CBFLAG
115	KEY_0
116	N/C
117	N/C
118	N/C
119	N/C
120	N/C
121	VAA
122	VAA
123	VAA
124	VAA
125	GND
126	GND
127	N/C
128	N/C
129	N/C
130	N/C
131	N/C
132	N/C
133	N/C
134	N/C
135	N/C
136	N/C
137	FS ADJUST
138	COMP
139	GND
140	VREF
141	VAA
142	VAA
143	NCOMP
144	VAA
145	NTSC/PAL
146	GND
147	CCOMP
148	VAA
149	C
150	GND
151	YCOMP
152	VAA
153	Y
154	GND
155	GND
156	CLOCK_OUT
157	H/HSYNC*
158	V/VSYNC*
159	CSYNC*
160	FIELD_0

Pin Descriptions (continued)



Note: N/C and test pins *must* remain floating.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt858 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Place components as close as possible to the associated pin. Whenever possible, place components so traces can be connected point to point.

The optimum layout enables the Bt858 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt858 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 12 This bead should be located within 3 inches of the Bt858 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, using the shortest possible leads (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1-µF ceramic capacitor in parallel with a 0.01-µF chip capacitor, decoupling each of the five groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 47 µF capacitor shown in Figure 12 is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

When using a linear regulator, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

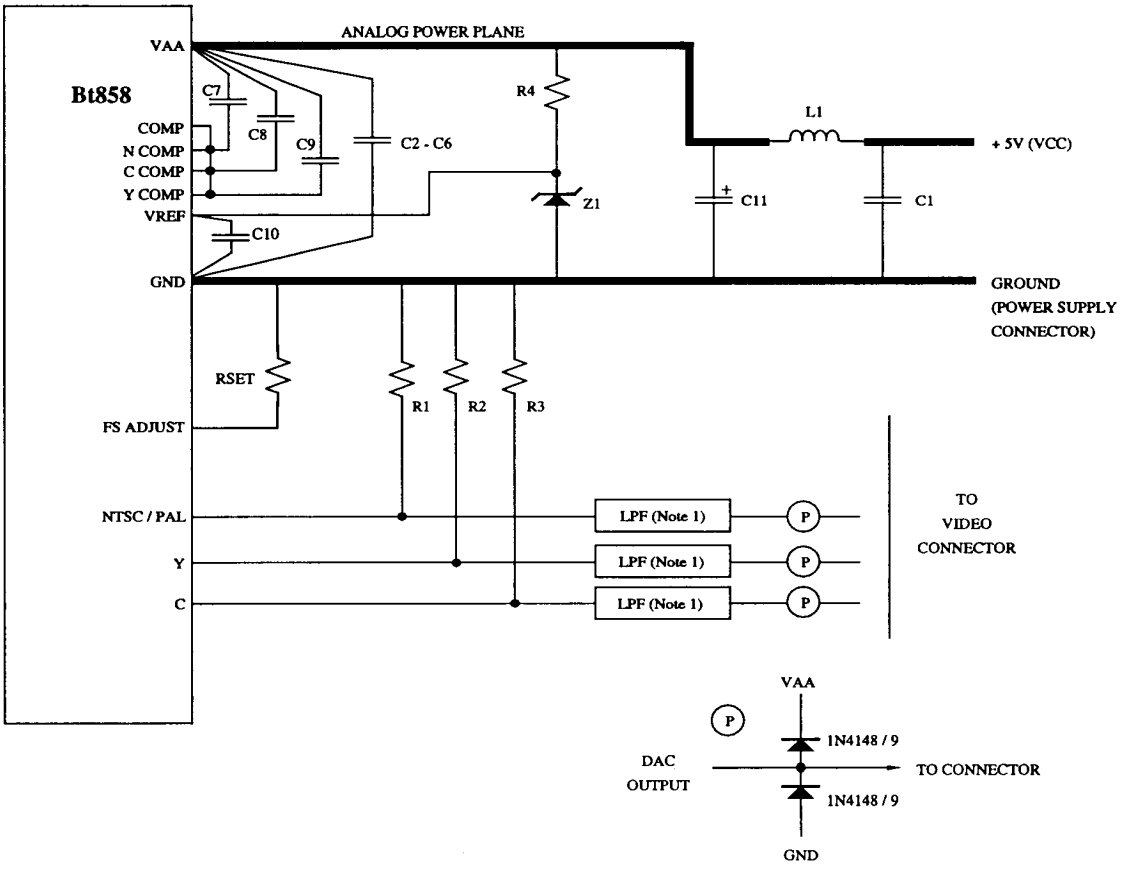
COMP Decoupling

The COMP pins must be decoupled to VAA, typically using 0.1 µF ceramic capacitors. Low-frequency supply noise will require larger values. The COMP capacitors must be as close as physically possible to the COMP and VAA pins. Surface-mount ceramic chip capacitors are preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to VAA. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. Providing alternate PCB pads (one to VAA and one to GND) is recommended for the VREF decoupling capacitor.

PC Board Layout Considerations (continued)



Note 1: A 150 Ω-to-75 Ω impedance-matching reconstruction filter is necessary on each output for proper video levels and fidelity. For specific filter designs call Brooktree Applications Engineering at 1-800-VIDEOIC.

Note 2: The value of RSET may require slight variance, depending on the reconstruction filter used.

Location	Description	Vendor Part Number
C1–C10	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C11	47 µF tantalum capacitor	Mallory CSR13F476KM
L1	ferrite bead	Fair-Rite 2743001111
R1–R3	150 Ω 1% metal film resistor	Dale CMF-55F
R4	1k-Ω 5% resistor	
RSET	98.8 Ω 1% metal film resistor	Dale CMF-55C (24.9 + 51.1)
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt858.

Figure 12. Typical Connection Diagram and Parts List for Parallel 150 Ω and 75 Ω Termination, and 150 Ω-to-75 Ω Impedance-Matching Reconstruction

PC Board Layout Considerations (continued)

Digital Signal Interconnect

The digital inputs to the Bt858 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates shouldn't be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Analog Signal Interconnect

The Bt858 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt858 to minimize reflections. Unused analog outputs should be connected to GND.

Analog Output Protection

The Bt858 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 12 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

Application Information

(Sin x/x)$^{-1}$ Correction Filters

The transfer function of the five-tap (sin x/x)$^{-1}$ correction filter prior to the D/A converters is:

$$H(Z) = 294/256 * Z0 + (-24/256)*(Z^{-1} + Z^{+1}) + (5/256)*(Z^{-2} + Z^{+2})$$

Figure 13 illustrates the pass-band and stop-band characteristics of the (sin x/x)$^{-1}$ correction filter.

IQ/UV Low-pass Digital Filters

The transfer function of the 19-tap filters that are used to low-pass filter the IQ or UV color difference video signals is:

$$H(Z) = 74/256 * Z0 + (64/256)*(Z^{-1} + Z^{+1}) + (37/256)*(Z^{-2} + Z^{+2}) + (9/256)*(Z^{-3} + Z^{+3}) + (-8/256)*(Z^{-4} + Z^{+4}) + (-11/256)*(Z^{-5} + Z^{+5}) + (-5/256)*(Z^{-6} + Z^{+6}) + (3/256)*(Z^{-8} + Z^{+8}) + (2/256)*(Z^{-9} + Z^{+9})$$

Figure 14 illustrates the pass-band and stop-band characteristics of the low-pass filters.

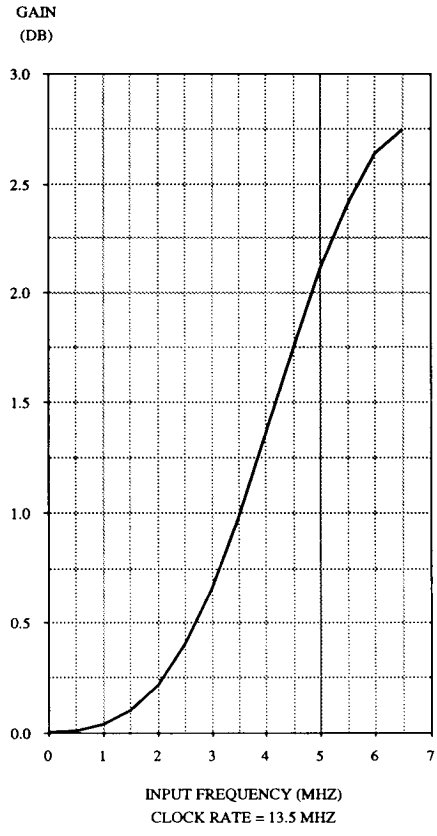


Figure 13. (Sin x/x)$^{-1}$ Correction Filter Characteristics.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by ensuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

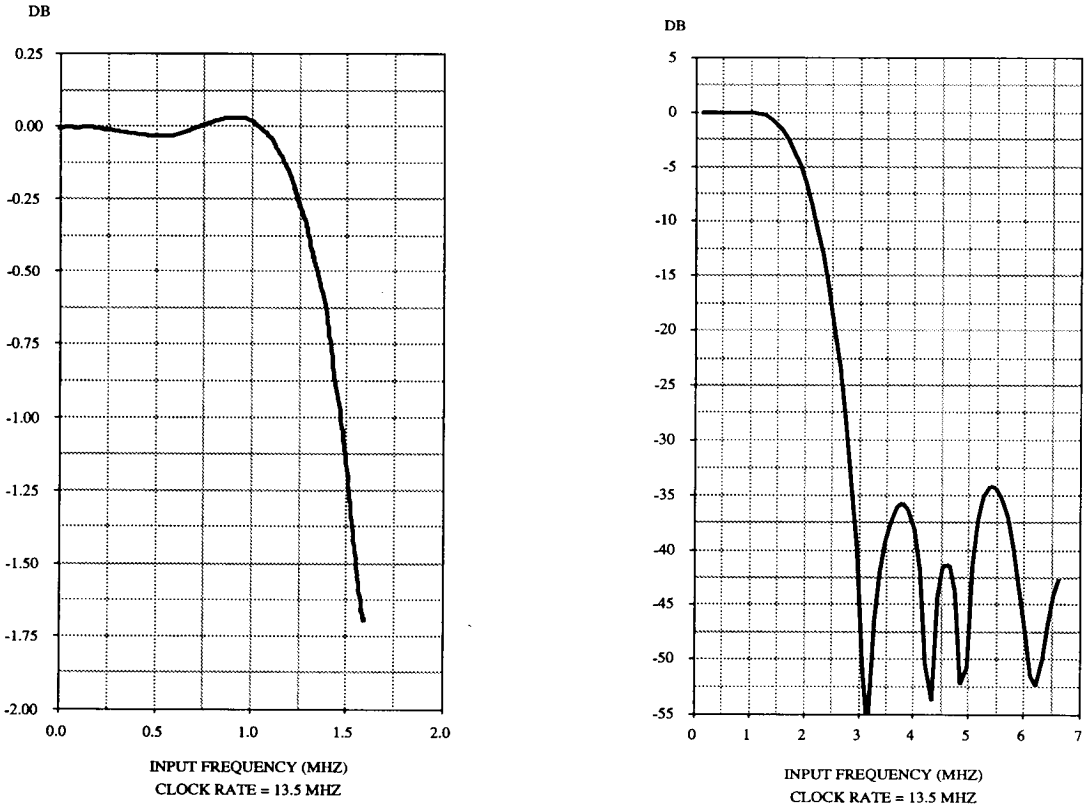


Figure 14. IQ/UV Low-pass Digital Filter Pass-Band and Stop-Band Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		50		Ω
External Voltage Reference	VREF	1.14	1.235	1.26	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating, only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Video D/A Resolution		10	10	10	Bits
Video D/A Accuracy					
Integral Linearity Error	IL			±2	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Video D/A Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF
Video Analog Outputs					
Output Disabled Current		0	5	50	µA
LSB Size			34		µA
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
C Analog Output					
Output Current (NTSC)					
Peak Chroma Relative to Blank		±7.95	±8.37	±8.79	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.72	±2.86	±3.00	mA
Output Current (PAL)					
Peak Chroma Relative to Blank		±8.63	±9.08	±9.53	mA
Blank Level		12.42	13.07	13.72	mA
Peak Burst Relative to Blank		±2.91	±3.06	±3.21	mA

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Blank Level Relative to Sync		5.43	5.72	6.01	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.58	14.29	15.00	mA
Black Level Relative to Blank		0	0	0	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
NTSC / PAL Analog Output					
Output Current (NTSC)					
White Level Relative to Black		12.56	13.22	13.88	mA
Black Level Relative to Blank		1.03	1.08	1.13	mA
Burst Relative to Blank		±2.72	±2.86	±3.00	mA
Blank Level Relative to Sync		5.43	5.72	6.01	mA
Sync Level		0.39	0.41	0.43	µA
Output Current (PAL)					
White Level Relative to Black		13.58	14.29	15.00	mA
Black Level Relative to Blank		0	0	0	mA
Burst Relative to Blank		±2.91	±3.06	±3.21	mA
Blank Level Relative to Sync		5.82	6.13	6.43	mA
Sync Level		0.39	0.41	0.43	µA
VREF Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		tbd		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 98.8 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
RS0–RS2 Setup Time	1	10			ns
RS0–RS2 Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	3			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	5			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
RD*, WR* Pulse Width Low	9	40			ns
RD*, WR* Pulse Width High	10	6*p15			ns
Analog Output Delay	19			30	ns
Analog Output Rise/Fall Time	20		3		ns
Analog Output Settling Time	21		13		ns
Clock and Data Feedthrough (Note 1)			tbd		dB
Glitch Impulse			tbd		pV–sec
DAC-to-DAC Crosstalk			tbd		dB
Analog Output Skew			0	5	ns
Pipeline Delay					
Blank/Sync into Sync/Field Out		3	3	3	Clocks
Blank/Sync into Analog Out		34	34	34	Clocks
VAA Supply Current (Note 2)	IAA		tbd	tbd	mA
Power-Down Mode			tbd	tbd	µA

See test conditions following this section.

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Y Bandwidth			Fin/2		MHz
Color Difference (IQ, UV) Bandwidth			1.3		MHz
Burst Frequency (Note 3)					
(M) NTSC		3.579535	3.579545	3.579555	MHz
(B, D, G, H, I) PAL		4.433614	4.433619	4.433623	MHz
Burst Envelope Rise / Fall Time		8	8	8	Clocks
Burst Cycles					
NTSC		8		9	Fsc Cycles
PAL		9		10	Fsc Cycles
Analog Sync Rise/Fall Time					
NTSC		6	6	6	Clocks
PAL		10	10	10	Clocks
Analog Blank Rise/Fall Time					
NTSC		10	10	10	Clocks
PAL		8	8	8	Clocks
Differential Gain			1		%
Differential Phase			1		Degree
SNR (per CCIR410)			60		dB
Hue Accuracy (Note 4)			0.5	1.2	%
Color Saturation Accuracy (Note 4)			0.5	1.2	%
Residual Subcarrier			-60		dB
Pixel and Control Setup Time	11	0			ns
Pixel and Control Hold Time	12	15			ns
Control Output Delay Time	13			tbd	ns
Control Output Hold Time	14	tbd			ns
CLOCK_IN Rate	Fin				
Normal Operation				18	MHz
Power Down Mode				80	MHz
CLOCK_IN Cycle Time (p15)	15				
Normal Operation		55.5			ns
Power Down Mode		12.5			ns
CLOCK_IN Pulse Width High Time	16	4			ns
CLOCK_IN Pulse Width Low Time	17	4			ns
CLOCK_IN to CLOCK_OUT Delay	18		tbd	tbd	ns

See test conditions following this section.

AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 98.8 Ω, VREF = 1.235 V, NTSC operation, and CLOCK_IN frequency = 13.5 MHz. Analog output load ≤10 pF; and D0–D7, FIELD_0, FIELD_1, HSYNC*, VSYNC*, and CLOCK_OUT output load ≤75 pF. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

Note 2: At Fmax. IAA (typ) at VAA = 5.0 V and TA = 20° C. IAA (max) at VAA = 5.25 V and TA = 0° C.

Note 3: Burst frequency tolerance is dependent on CLOCK_IN frequency tolerance and jitter. This also assumes that P1 and P2 registers are correctly configured.

Note 4: This is measured with a Matthey Vs618H filter; accuracy is dependent on pixel clock rate and the color space used.

Timing Waveforms

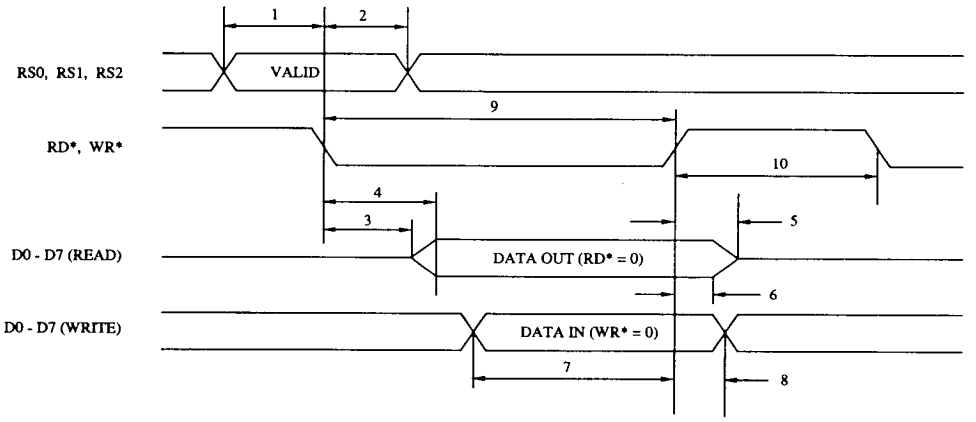
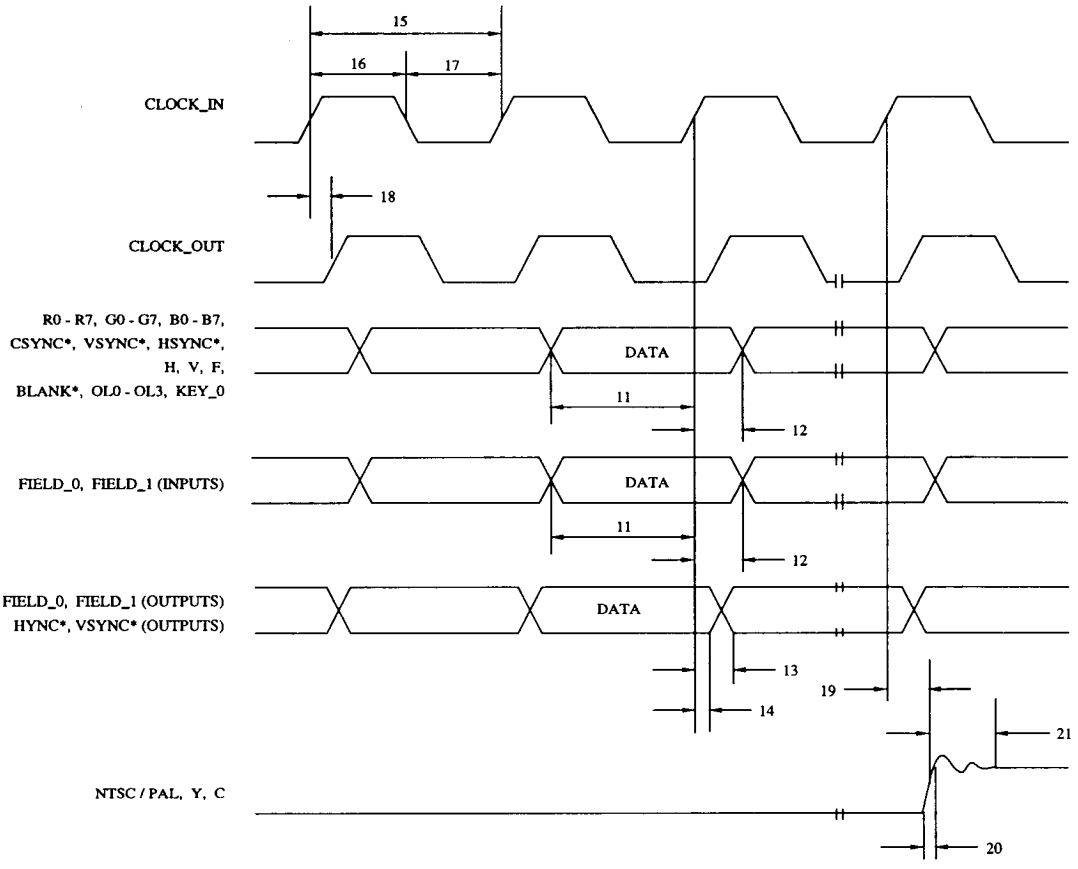


Figure 15. MPU Read/Write Timing.

Timing Waveforms (continued)



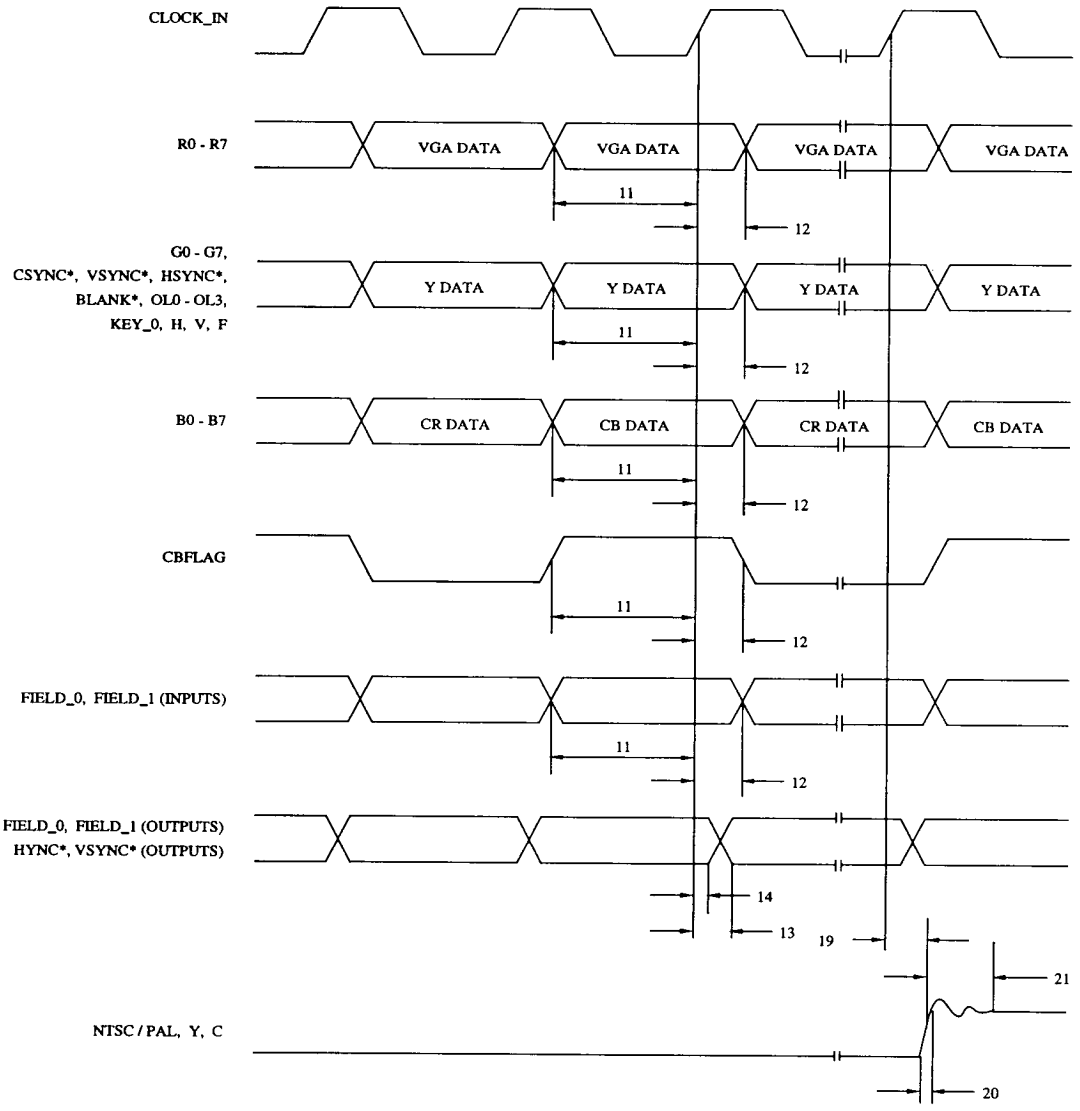
Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full- scale transition.

Figure 16. Video Input/Output Timing. (All Input Formats Except 16-bit YCrCb).

Timing Waveforms (continued)



Note 1: Analog output delay is measured from the 50-percent point of the rising edge of CLOCK_IN to the 50-percent point of full-scale transition.

Note 2: Analog settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±2 LSB.

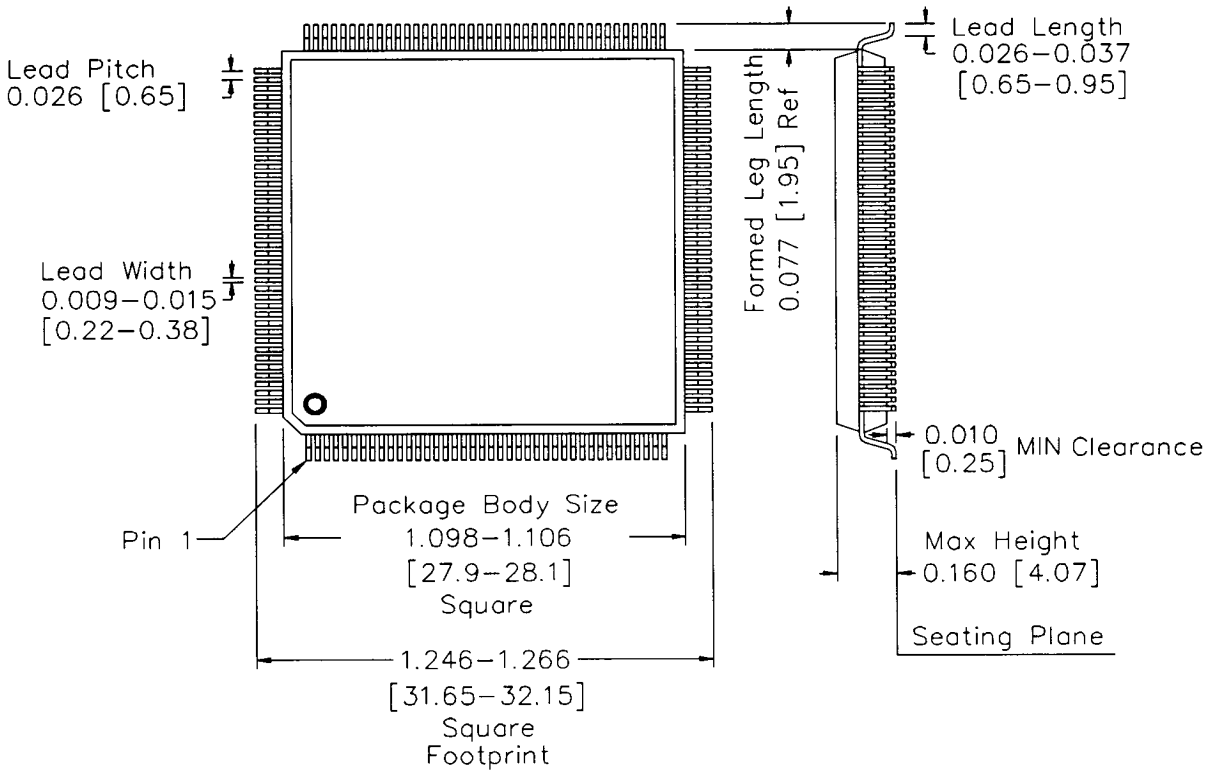
Note 3: Analog output rise/fall time is measured between the 10-percent and 90-percent points of full- scale transition.

Figure 17. Video Input/Output Timing (16-Bit YCrCb Input Format).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt858KPF	160-pin Plastic Quad Flatpack	0° to +70° C

Package Drawing—160-pin Plastic Quad Flatpack (EIAJ-PQFP)



Notes—Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Package body size does not include mold protrusion or mismatch.

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CAUTION

ESD-sensitive device. Permanent damage may occur on unconnected devices subjected to high-energy electrostatic fields. Unused devices must be stored in conductive foan or shunts.

Do not insert this device into powered sockets.

Remove power before insertion or removal.

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