

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at $T_{amb} = 25^\circ\text{C}$; $I_D = 200 \mu\text{A}$; $V_{DG} = 15 \text{ V}$

	BFQ10	11	12	13	14	15	16	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	mV
Thermal drift of gate-source voltage difference	$\frac{d\Delta V_{GS}}{dT}$	< 5	5	10	20	20	40	$\mu\text{V/K}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0.98	0.98	0.98	0.98	0.98	0.95	
	$\frac{g_{2fs}}{g_{1fs}}$	< 1.02	1.02	1.02	1.02	1.02	1.05	
Difference in transfer impedance	$ \Delta \frac{1}{g_{fs}} $	< 6	6	12	12	12	20	Ω
Difference in penetration factor	$ \Delta \frac{g_{os}}{g_{fs}} $	< 18	30	40	50	60	70	$\mu\text{V/V}$
Common mode rejection ratio	CMRR	> 95	90	85	85	80	80	dB

MECHANICAL DATA

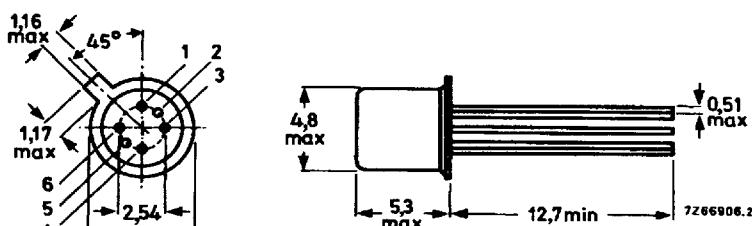
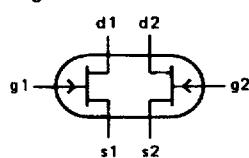
Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.

Pinning

- 1 = source 1
- 2 = drain 1
- 3 = gate 1
- 4 = source 2
- 5 = drain 2
- 6 = gate 2



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40 V
Drain current	I_D	max.	30 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 75^\circ\text{C}$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		-65 to +200 °C
Junction temperature	T_j	max.	200 °C

THERMAL RESISTANCEFrom junction to ambient in free air $R_{th \ j-a}$ = 500 K/W

CHARACTERISTICS (total device) $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specifiedMeasured at: $I_D = 200 \mu\text{A}$; $V_{DG} = 15 \text{ V}$ except for drain current ratio.

	BFQ10	11	12	13	14	15	16	
Drain current ratio (note 1) $V_{DG} = 15 \text{ V}; V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	> 0.97 < 1.03	0.95 1.05	0.95 1.05	0.95 1.05	0.92 1.08	0.90 1.10	0.80 1.20
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10 pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50 mV
Thermal drift of gate-source voltage difference	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50 $\mu\text{V/K}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0.98 < 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.95 1.05	0.95 1.05
Difference in transfer impedance (note 2)	$\left \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30 Ω
Difference in penetration factor (note 3)	$\left \frac{g_{os}}{g_{fs}} \right $	< 18	30	40	50	60	70	100 $\mu\text{V/V}$
Common mode rejection ratio (note 4)	CMRR	> 95	90	85	85	80	80	80 dB

Notes

1. Measured under pulse conditions.

2. The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d\Delta V_{GS}}{dI_D} \text{ at } V_{DG} = \text{constant} \right).$$

3. The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d\Delta V_{GS}}{dV_{DG}} \text{ at } I_D = \text{constant} \right).$$

4. Common mode rejection ratio:

$$\text{CMRR (in dB)} = -20 \log \left| \Delta \frac{g_{os}}{g_{fs}} \right|.$$

CHARACTERISTICS (Individual transistor) $T_{amb} = 25^\circ\text{C}$ unless otherwise specified**Gate cut-off current**

$-V_{GS} = 20 \text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 pA
$-V_{GS} = 20 \text{ V}; V_{DS} = 0; T_{amb} = 125^\circ\text{C}$	$-I_{GSS}$	<	20 nA

Gate current

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}; T_{amb} = 125^\circ\text{C}$	I_G	<	10 nA
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Drain current (note 1)

$V_{DS} = 15 \text{ V}; V_{GS} = 0$	I_{DSS}		0.5 to 10 mA
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Gate-source voltage

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}$	$-V_{GS}$	<	2.7 V
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Gate-source cut-off voltage

$I_D = 1 \text{ nA}; V_{DG} = 15 \text{ V}$	$-V_{(P)GS}$		0.5 to 3.5 V
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Transfer conductance at $f = 1 \text{ kHz}$

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}$	g_{fs}	>	1.0 mS
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Output conductance at $f = 1 \text{ kHz}$

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}$	g_{os}	<	5 μS
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Input capacitance at $f = 1 \text{ MHz}$ (note 2)

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}$	C_{is}	<	8 pF
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Feedback capacitance at $f = 1 \text{ MHz}$ (note 2)

$I_D = 200 \mu\text{A}; V_{DG} = 15 \text{ V}$	C_{rs}	<	1.0 pF
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Equivalent noise voltage

$I_D = 200 \mu\text{A}; V_{DS} = 15 \text{ V};$ $B = 0.6 \text{ to } 100 \text{ Hz}$	V_n	<	0.5 μV
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Notes

1. Measured under pulse conditions.
2. Measured with case grounded.

