ISM6258/MSM6258V

ADPCM SPEECH PROCESSOR FOR SOLID STATE RECORDER

TO CUSTOMERS FOR NEW CIRCUIT DESIGN

For a new circuit design, it is recommended to use not the MSM6258, but the MSM6388/MSM6588 as described later.

The MSM6258 has an 8-bit AD converter and does not have a built in low pass filter. On the other hand, the MSM6388/MSM6588 has a 12-bit AD converter and includes a low pass filter. Therefore, the MSM6388/MSM6588 can realize a high quality voice.

In addition, the same control as a CPU interface of the MSM6258 can be performed by using the EPLAY/EREC command of the MSM6388 and the EXT command of the MSM6588.

GENERAL DESCRIPTION

The MSM6258 is a complex and highly integrated ADPCM speech processor, implemented in CMOS technology for low power consumption. The integrated A/D and D/A converters make the chip more self-contained, relieving the need for external conversion circuitry. The device comprises internally. A DRAM controller permitting the use of DRAMs alternatively to SRAMs and ROMs to store speech data. In other words, less periphery, thus less system vulnerability a voice detection circuit and phrase select provision are successfully added features for increased performance.

The ADPCM analysis and synthesis block is identical to the popular OKI MSM5218, that is, the bit overflow protection is included in for improved reproduction quality. The device is offered in two basic versions one of which comes in two package types. One is the version designed to be interfaced with an 8-bit CPU like the OKI MSM80C85 or MSM80C51 microcontroller, and comes in a 40-pin flat package; the other operates as a stand-alone solution that includes 19-pin programmable output lines for memory addressing and chip select in a 60-pin flat package or in a 68-pin PLCC, respectively, to permit full surface mount implementation.

MSM6258 accepts 4 to 8MHz master clocks, out of which two sets of sampling frequencies can be derived. Additionally, the ADPCM bit number is pin-selectable between 3 or 4 bits per sample. When using 256k or 1Mb DRAMs, the maximum I/O time is approximately 17 minutes at a bit-rate of 16kbps, while 256k SRAMs offer a little more than a minute of speech, both in their maximum memory configurations. At the higher bit-rates, 21.2 and 32 kbps, the I/O times are reduced proportionally.

In the case of DRAMs, the OKI MSC2304 (2-Megabit, module) or MSC2305 (4-Megabit module) are recommendable for space and cost saving benefits and in the interest of simplified handling. In the external mode, the built-in 8-bit ADC is looped so that a separate ADC can be connected to MSM6258, the accuracy of which may be between 8 to 12-bit for 'recording' speech. When the playback mode is set, the internal 10-bit DAC will be disabled to permit the connection of an external DAC of 10 to 12-bit of resolution.

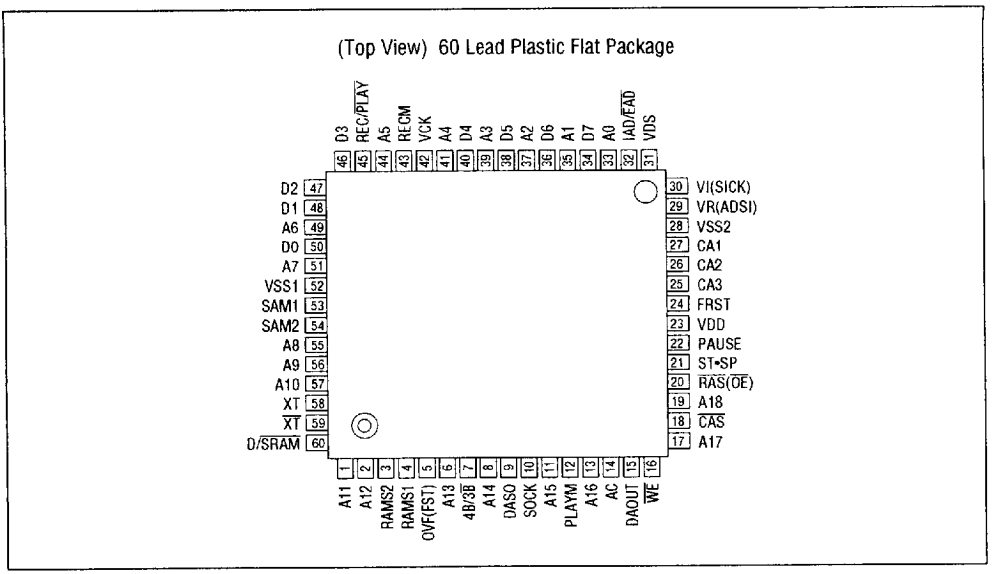
FEATURES

1. STAND-ALONE VERSION
   - Switch or microcomputer interface is possible
   - Straight ADPCM (3-bit/4-bit)
   - Built-in voice detection circuit
   - Built-in DRAM refresh circuit
   - SRAM/DRAM can be directly connected.
     Maximum 16 M-bit (with 256K or 1M DRAM used)
   - Sampling frequency selection
     3.9, 5.2, 7.8kHz (for original oscillation frequency of 4.0 MHz)
     4.0, 5.3, 8.0kHz (for original oscillation frequency of 4.096 MHz)
     7.8, 10.4, 15.6kHz (for original oscillation frequency of 8.0 MHz)
   - Maximum number for words recorded: 7-word
   - Original oscillation frequency: 4~8 MHz
   - Built-in AD converter: 8-bit
   - Built-in DA converter: 10-bit (voltage type of class A)
   - Operable with a single power supply
   - 60-pin plastic QFP (QFP60-P-1519-K)
     - 60-pin V plastic QFP (QFP60-P-1519-VK)
     - 68-pin plastic QFJ (PLCC) (QFJ68-P-S950)

2. CPU INTERFACE VERSION
   - Command/status can be input and output through the data bus.
   - Straight ADPCM (3-bit/4-bit)
   - Sampling frequency selection
     3.9, 5.2, 7.8kHz (for original oscillation frequency of 4.0 MHz)
     4.0, 5.3, 8.0kHz (for original oscillation frequency of 4.096 MHz)
     7.8, 10.4, 15.6kHz (for original oscillation frequency of 8.0 MHz)
   - Maximum number for words recorded: 7-word
   - Original oscillation frequency: 4~8 MHz
   - Built-in AD converter: 8-bit
   - Built-in DA converter: 10-bit (voltage type of class A)
   - Operable with a single power supply
     - 40-pin plastic DIP (DIP40-P-600)
     - 44-pin plastic QFP (QFP44-P-910-K)
     - 44-pin-V plastic QFP (QFP44-P-910-V1K)
     - 44-pin plastic QFJ (PLCC) (QFJ44-P-S650)

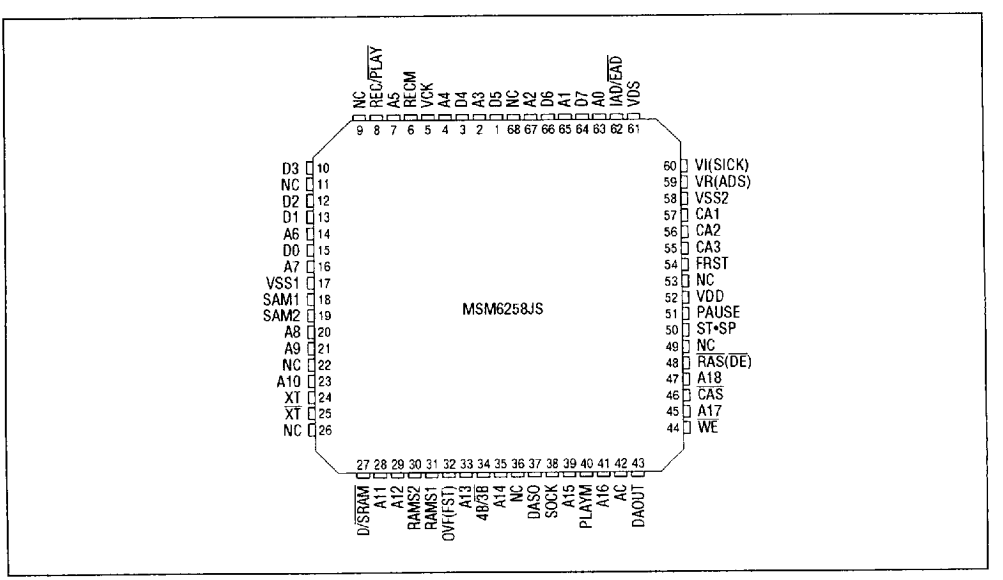
PIN CONFIGURATION

1. Stand-alone version



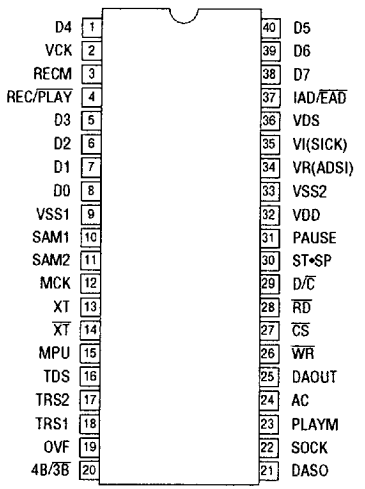
Note 1: Applicable to the MSM6258GS-K, GS-VK.

68-lead plastic leaded chip carrier



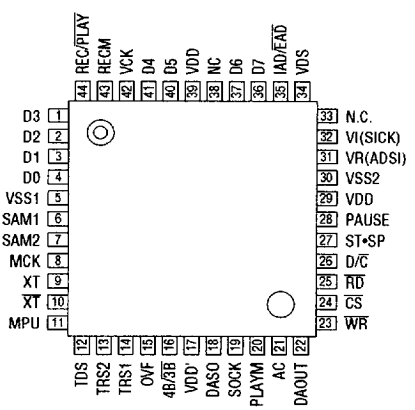
2. CPU interface verison

(Top View) 40 Lead Plastic DIP



Note 1: Applicable to the MSM6258VRS.

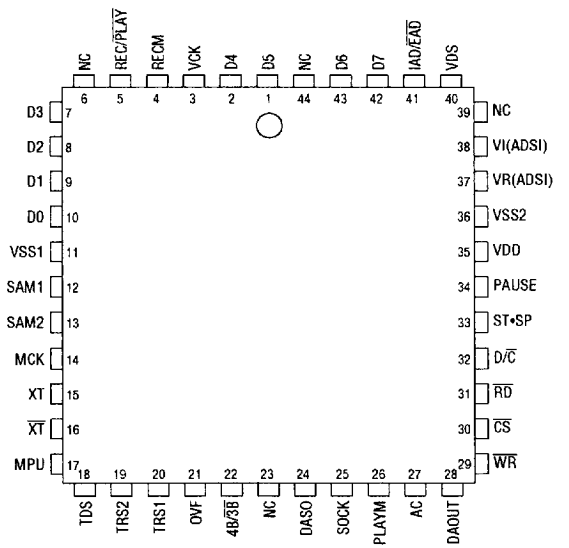
(Top View) 44 Lead Plastic Flat Package



Note 1: Applicable to the MSM6258VGS-K & GS-V1K
Note 2: VDD' connected to VDD Pin

MSM6258VJS

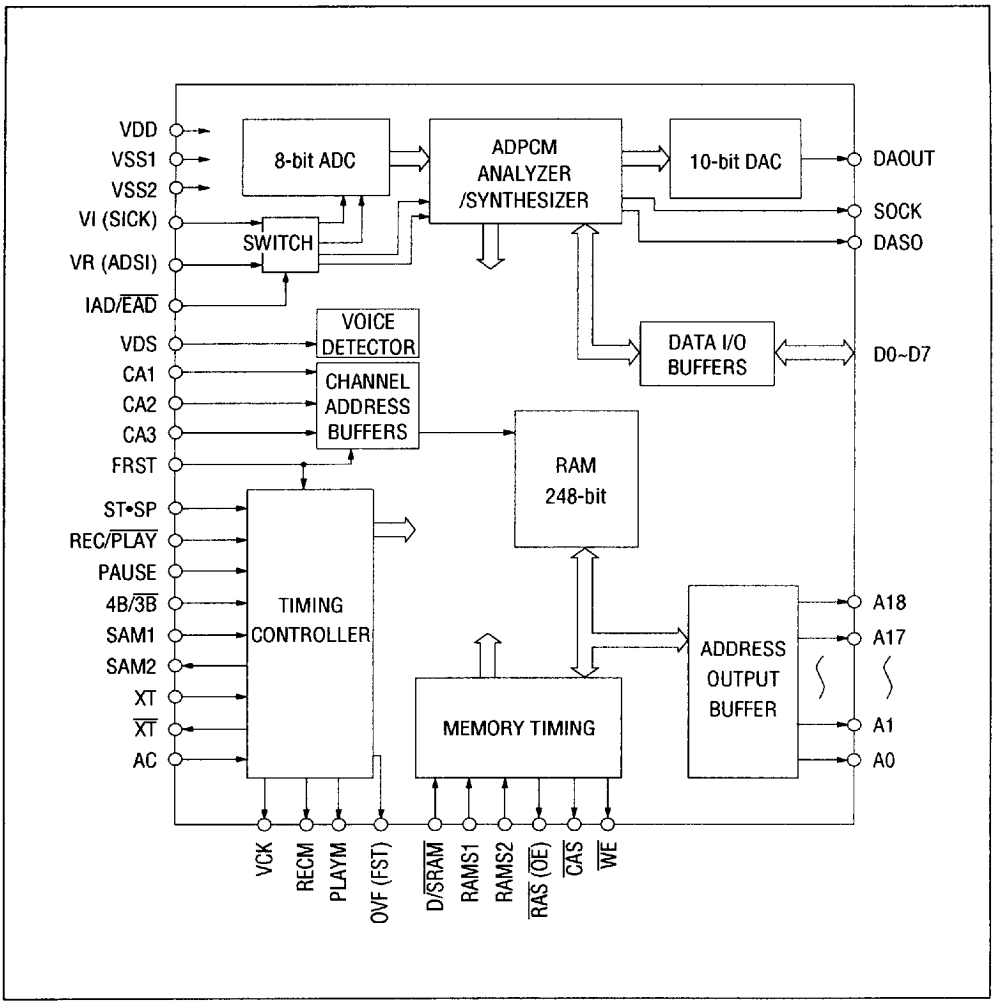
(Top View) 44-Pin Plastic Leaded Chip Carrier



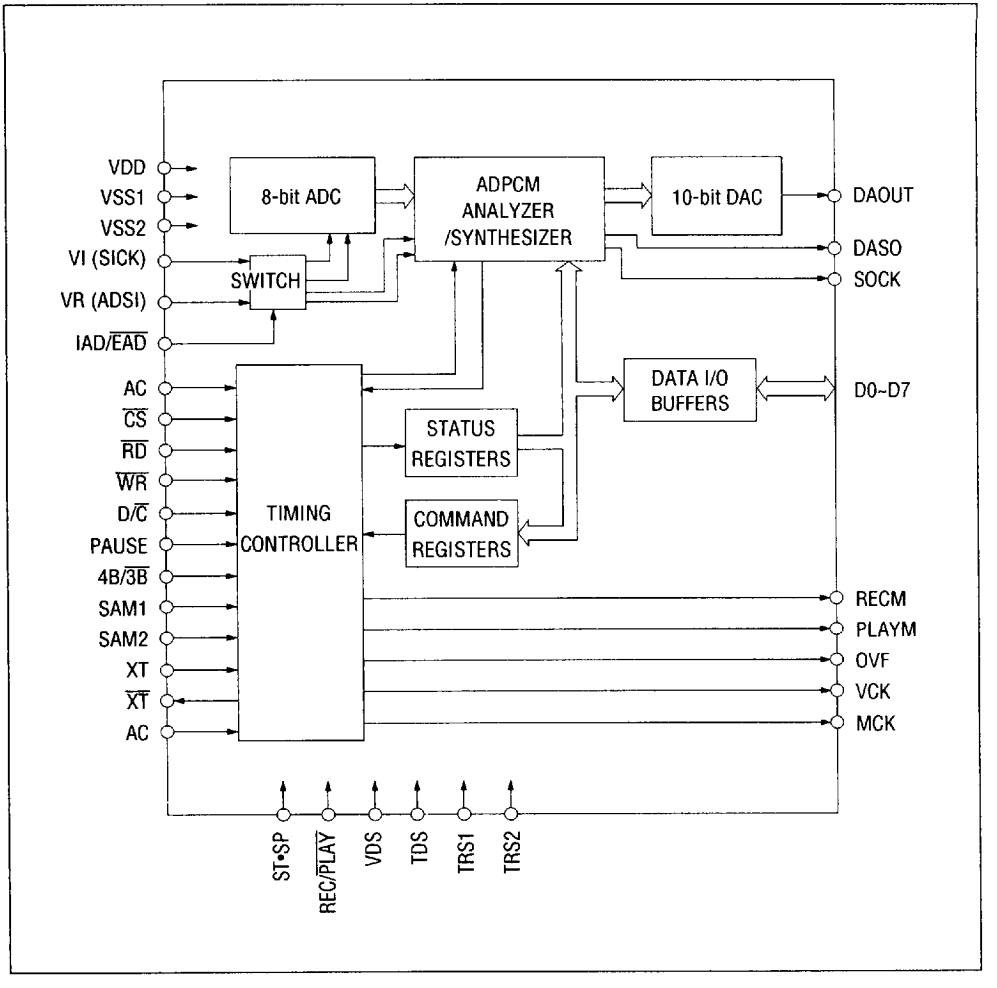
Note 1: Applicable to the MSM6258VJS.

FUNCTIONAL BLOCK DIAGRAM

1. Stand-alone version



2. CPU interface version



ABSOLUTE MAXIMUM RATINGS

STAND-ALONE & MPU interface version

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	T_a = 25°C	−0.3 ~ +7.0	V
Input voltage	V_{IN}	T_a = 25°C	−0.3 ~ VDD +0.3	V
Storage temperature	T_{stg}	–	−55 ~ +150	°C

Note: Permanent device damage may occur it ABSOLUTE MAXIMUM RATINGS are exceeded Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value	Unit
Power supply voltage	VDD	V_{SS1} = V_{SS2} = 0V	+3 ~ +6.0	V
Ambient range	T_{OP}	–	−40 ~ +85	°C
Oscillation frequency	F_{OSC}	–	4.0 ~ 8.0	MHz

DC CHARACTERISTICS

(VDD = 5V/10%, Ta = –40 to +85°C) STAND–ALONE VERSION
(VDD = 5V/10%, Ta = –40 to +70°C) CPU I/F VERSION

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating current	I_{DD}	F_{OSC} = 4.0MHz	–	–	4	mA
Stand by current	I_{DS}	With SRAM, AC=H	–	–	10	µA
H input voltage	V_{IH1}	–	3.6	–	–	V
H input voltage (Note 1)	V_{IH2}	–	0.8 × VDD	–	–	V
L input voltage	V_{IL}	–	–	–	0.8	V
H output voltage	V_{OH}	IOH = –40µA	4.2	–	–	V
L output voltage	V_{OL}	IOL = 2mA	–	–	0.45	V
H input current	I_{IH1}	Without pull down VIH=VDD	–	–	10	µA
H input current (Note 2)	I_{IH2}	With pull down VIL=0V	20	–	400	µA
L input current	I_{IL}	$V_{IL}=V_{SS}$	–10	–	10	µA
Output leakage current	I_{LO}	OV < VO < VDD	–10	–	10	µA
DA–output relative error	$\lvert V_{DAE} \rvert$	No-load	–	–	40	mV
AD conversion precision	$\lvert V_{ADE} \rvert$	VSS1=VSS2=0V VR=VDD	–	–	40	mV
DA output impedance	R_{DA}	–	12	17	22	kΩ
VR input impedance	R_{VR}	–	–	35	–	kΩ
VR input voltage	V_{VR}	–	0.9 × VDD	–	VDD	V
VI input voltage	V_{VI}	–	0	–	V_{VR}	V
VI input impedance	R_{VI}	–	10	–	–	kΩ

- S/N = (n-1) × 6
  n = ADC bit number

Note 1: Applies to XT
Note 2: Applies to ST•SP and PAUSE and MPU, FRST, VDS (only CPU I/F version)

AC CHARACTERISTICS

1. Stand-Alone Version

VDD = 4.5 - 5.5V, Ta = –40 - 85°C
fosc = 4.096 MHz, fs= 8.0 kHz

Item		Symbol	Min.	Typ.	Max.	Unit
AC pulse width		t_{ACP}	2.0	–	–	µs
PAUSE pulse width		t_{PAP}	2.0	–	–	µs
FRST pulse width		t_{FRP}	2.0	–	–	µs
ST•SP pulse width (1) (STOP pulse width when D SRAM ="L", and REC/$\overline{PLAY}$="H") (Note 2)		t_{SPP}	66	–	–	ms
ST•SP pulse width(2) (STOP pulse width excepting (1) above)		t_{STP}	2.0	–	–	µs
Time from entry of start pulse to rise of RECM when DRAM is selected (Note 1)		t_{DRR}	–	16.3	–	ms
Time from starting of oscillation to rise of RECM when SRAM is selected		t_{SRR}	56.2	–	70	ms
Time from starting of oscillation to initial change of DAOUT when SRAM is selected (Note 1)		t_{XDS}	–	40	–	ms
Time from entry of STOP pulse to fall of RECM (Note 1)		t_{SRF}	0	–	66	ms
Time for DAOUT to change from GND to 1/2 VDD (Note 1)		t_{DAR}	–	16	–	ms
Time from entry of STOP pulse to change of DAOUT to GND (Note 1)	REC/$\overline{PLAY}$ "H"	t_{DAL}	0	50	100	ms
	REC/$\overline{PLAY}$ "L"	t_{DAF}	0	16	32	ms
Time from setting of PLAYM to "L" to entry of restart pulse (Note 1)		t_{PRS}	52	–	–	ms
Time from entry of START pulse to rise of PLAYM (Note 1)		t_{SPR}	0	–	4	µs
Time from entry of STOP pulse to fall of PLAYM (Note 1)		t_{SPF}	0	–	4	µs
Time from setting of REC/$\overline{PLAY}$, CA1 - CA3 to entry of START pulse		t_{STC}	2	–	–	µs
Time from completion of entry of STOP pulse to change of REC/$\overline{PLAY}$, CA1 - CA3		t_{SPC}	2	–	–	µs

(Note 1) Proportionate to fosc (Raising fosc shortens the time.)

(Note 2) Proportionate to fs (Raising fs shortens the time.)

2. CPU Interface Version

VDD = 4.5 - 5.5V, Ta = −40 - 85°C
fosc = 4.096 MHz, fs = 8.0 kHz

Item		Symbol	Min.	Typ.	Max.	Unit
Time during which the level of VCK remains "H"	(Note 1)	t_{VH}	–	62.5	–	µs
Time during which the level of VCK remains "L"	(Note 1)	t_{VL}	–	62.5	–	µs
Time during which the level of MCK remains "H"	(Note 2)	t_{MH}	–	39.1	–	µs
Time during which the level of MCK remains "L"	(Note 3)	t_{ML}	–	210.9	–	µs
Time from rise of VCK to rise of MCK	(Note 2)	t_{VM}	–	19.5	–	µs
Setup time for fall of MCK during ADPCM data reading	(Note 2)	t_{RMS}	15	–	–	µs
Hold time for fall of MCK during ADPCM data reading	(Note 2)	t_{RMH}	55	–	–	µs
Setup time for fall of MCK during ADPCM data writing	(Note 2)	t_{WMS}	70	–	–	µs
Hold time for fall of MCK during ADPCM data writing	(Note 2)	t_{WMH}	2	–	–	µs
$\overline{RD}$ pulse width		t_{RR}	250	–	–	ns
D/$\overline{C}$ setup time for fall of $\overline{RD}$		t_{DCR}	50	–	–	ns
D/$\overline{C}$ hold time for rise of $\overline{RD}$		t_{RDC}	100	–	–	ns
$\overline{CS}$ setup hold time for $\overline{RD}$		t_{CR}	0	–	–	ns
Data establishment time from fall of $\overline{RD}$		t_{DRE}	–	–	200	ns
Data float time from rise of $\overline{RD}$		t_{DRF}	10	–	200	ns
$\overline{WR}$ pulse width		t_{WW}	250	–	–	ns
D/$\overline{C}$ setup time for fall of $\overline{WR}$		t_{DCW}	50	–	–	ns
D/$\overline{C}$ hold time for rise of $\overline{WR}$		t_{WDC}	100	–	–	ns
$\overline{CS}$ setup hold time for $\overline{WR}$		t_{CW}	0	–	–	ns
Data setup time for rise of $\overline{WR}$		t_{DWS}	100	–	–	ns
Data hold time for rise of $\overline{WR}$		t_{DWH}	30	–	–	ns
Time from fall of AC to entry of start command	(Note 2)	t_{AS}	16.0	–	–	ms
Setup time for entry of start command in rise of VCK	(Note 2)	t_{WVS}	4	–	120	µs
Hold time for entry of stop command in rise of VCK	(Note 2)	t_{WVP}	4	–	120	µs

Item	Symbol	Min.	Typ.	Max.	Unit
Time from fall of VCK to rise of RECK	t_{VRR}	0.0	–	2.0	µs
Time from fall of VCK to fall of RECM	t_{VRF}	0.0	–	2.0	µs
Time from fall of AC to time when DAOUT is set to 1/2 VDD (Note 2)	t_{DAR}	–	15.6	–	ms
Time from entry of start command to rise of PLAYM	t_{WPR}	0.0	–	4.0	µs
Time from entry of stop command to fall of PLAYM (Note 2)	t_{WPF}	0.0	–	2.0	µs
Time from entry of stop command to entry of start command (Note 1)	t_{SPT}	260	–	–	µs
Duty cycle for input of original oscillation clock to XT	f_{DUTY}	40	50	60	%

(Note 1) Proportionate to fs (Raising fs extends the time.)

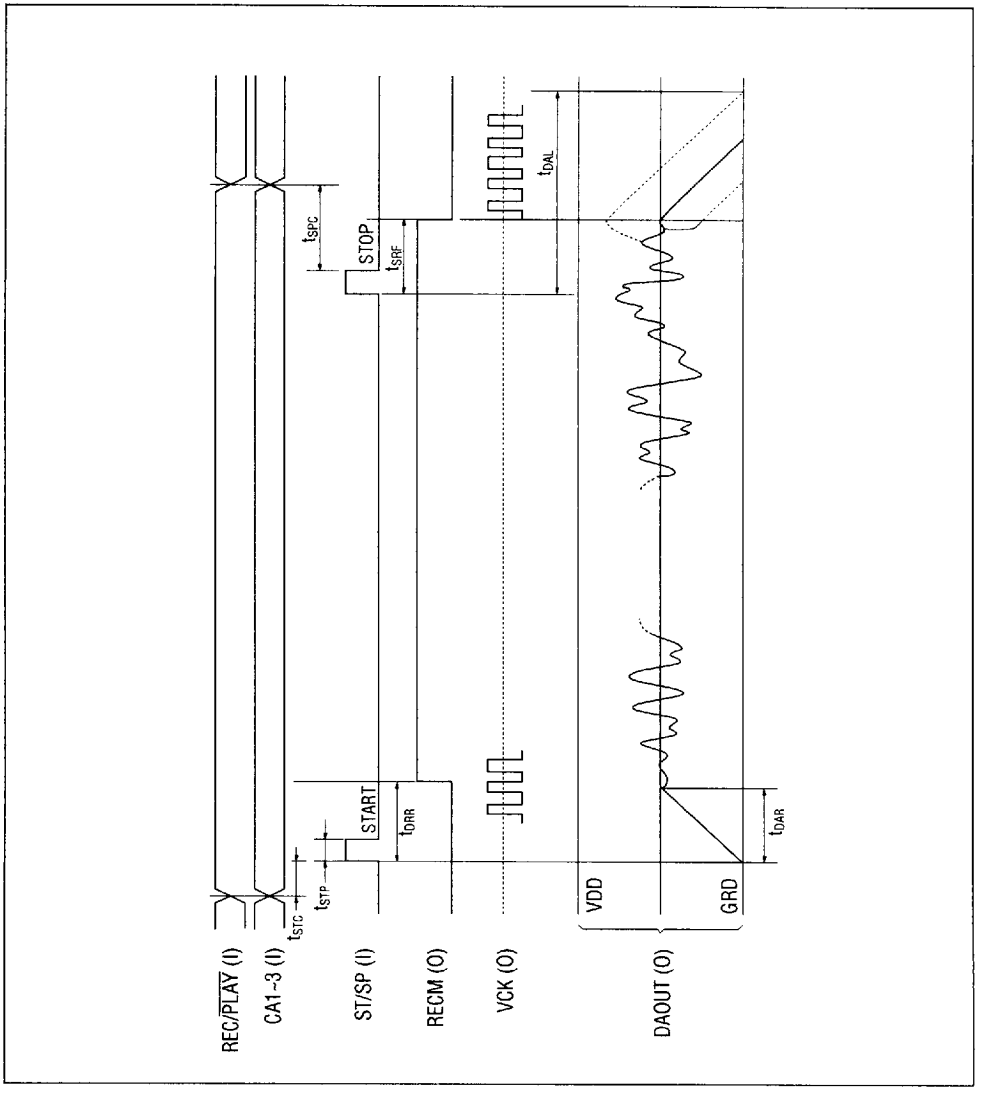
(Note 2) Proportionate to fosc (Raising fosc shortens the time.)

(Note 3) Equivalent to two times the sampling period minus t_{MH}

TIMING CHART

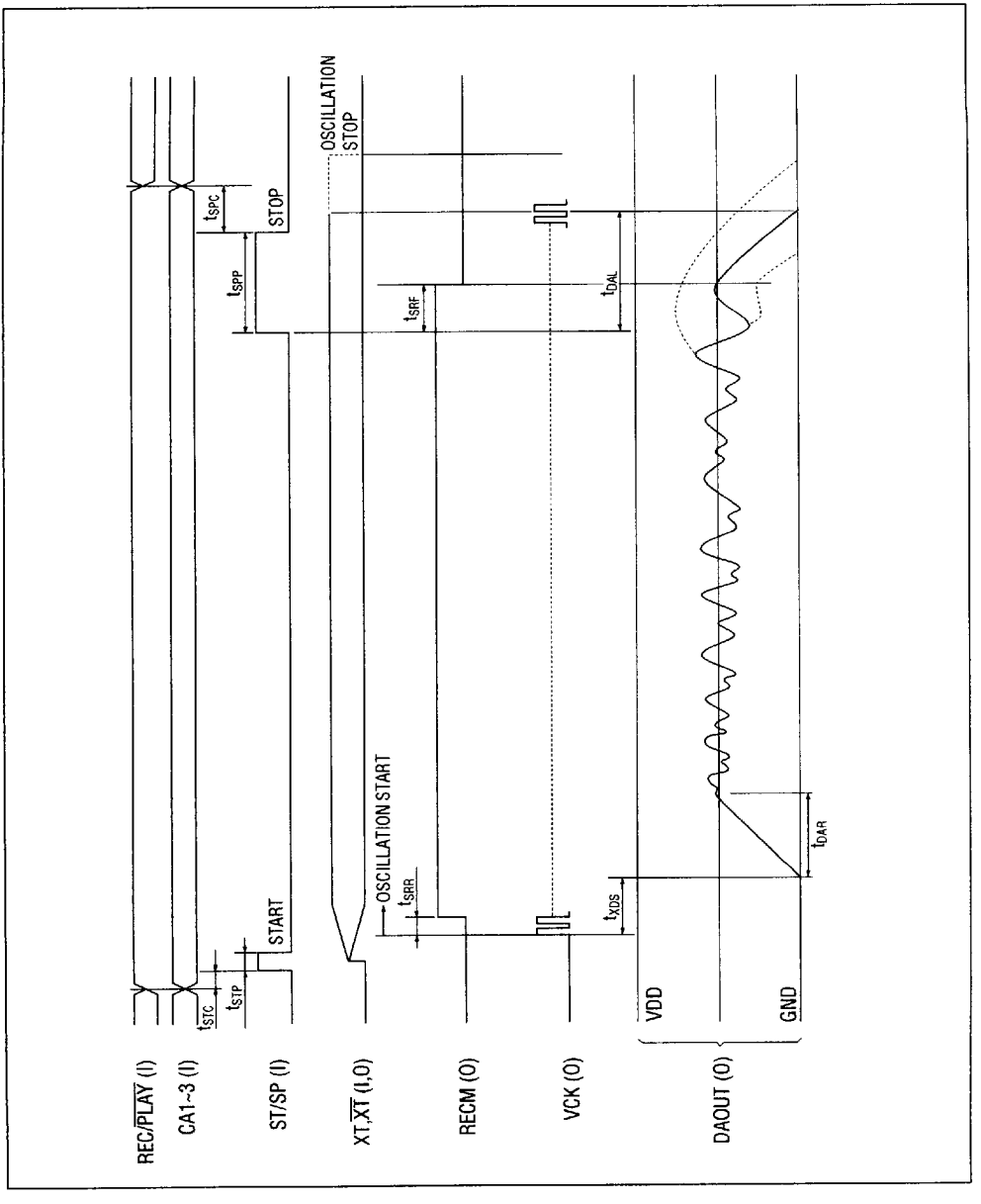
1. Stand-Alone Version

- **RECORD TIMING** (with DRAM selected, VDS = "L")



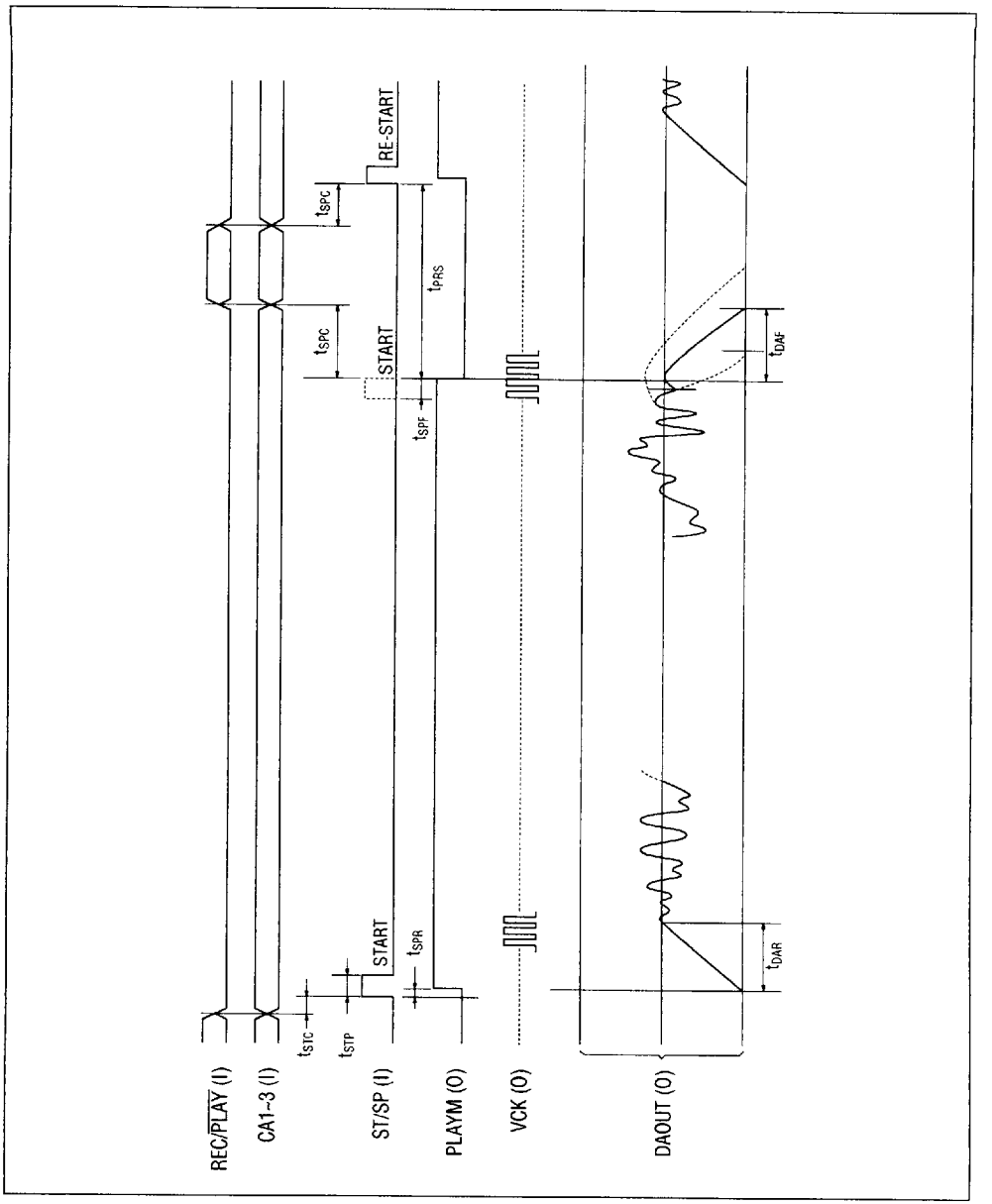
Note If VDS = "H", RECM outputs 2 Hz clock during detection of voice.

- **RECORD TIMING** (with SRAM selected, VDS = "L")



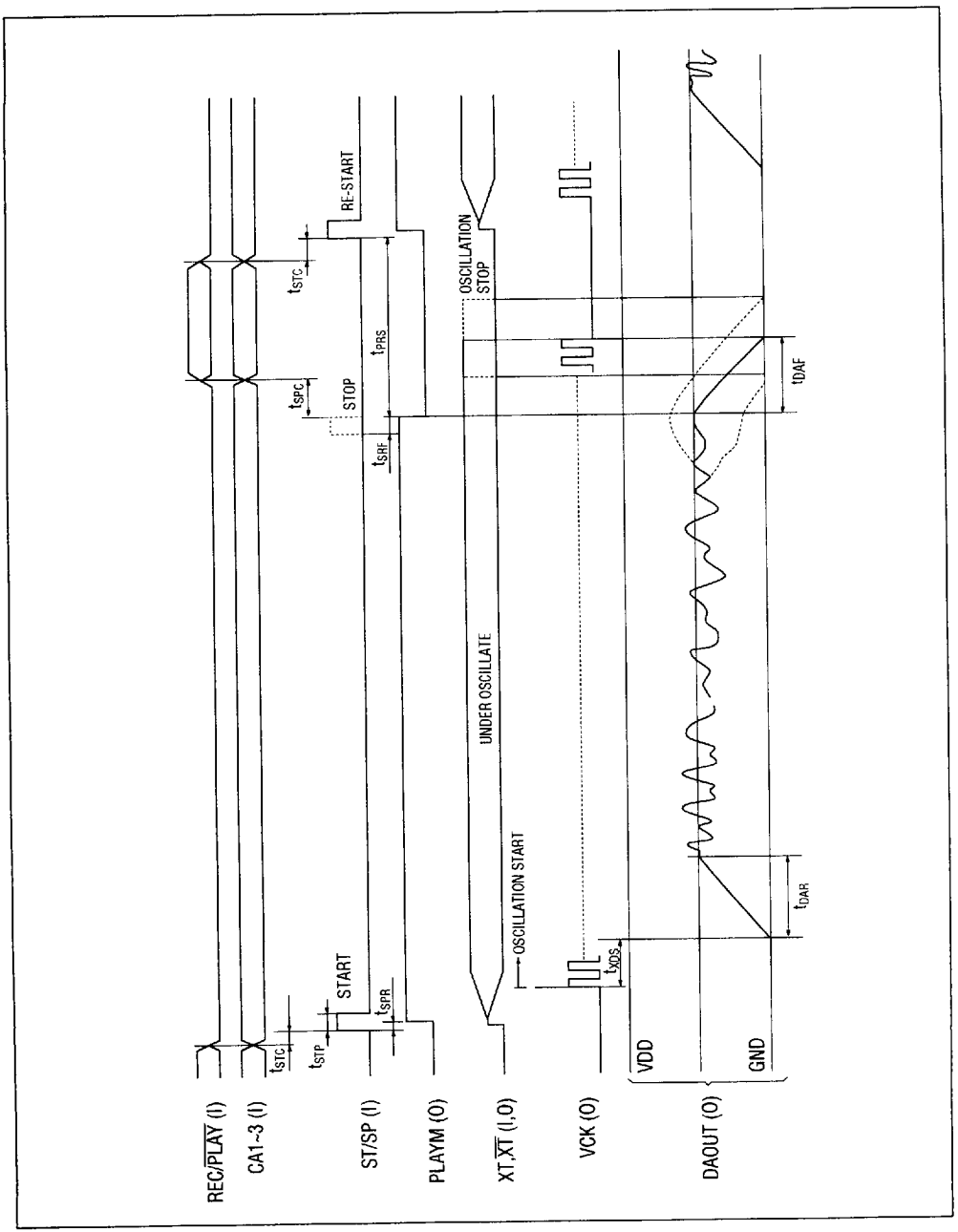
Note If VDS = "H", RECM outputs 2 Hz clock during detection of voice.

- **PLAYBACK TIMING** (with DRAM selected)



Note t_{DAF} = 16 msec when DAOUT signal level is 1/2 VDD,
t_{DAF} = 32 msec when DAOUT signal level is VDD.

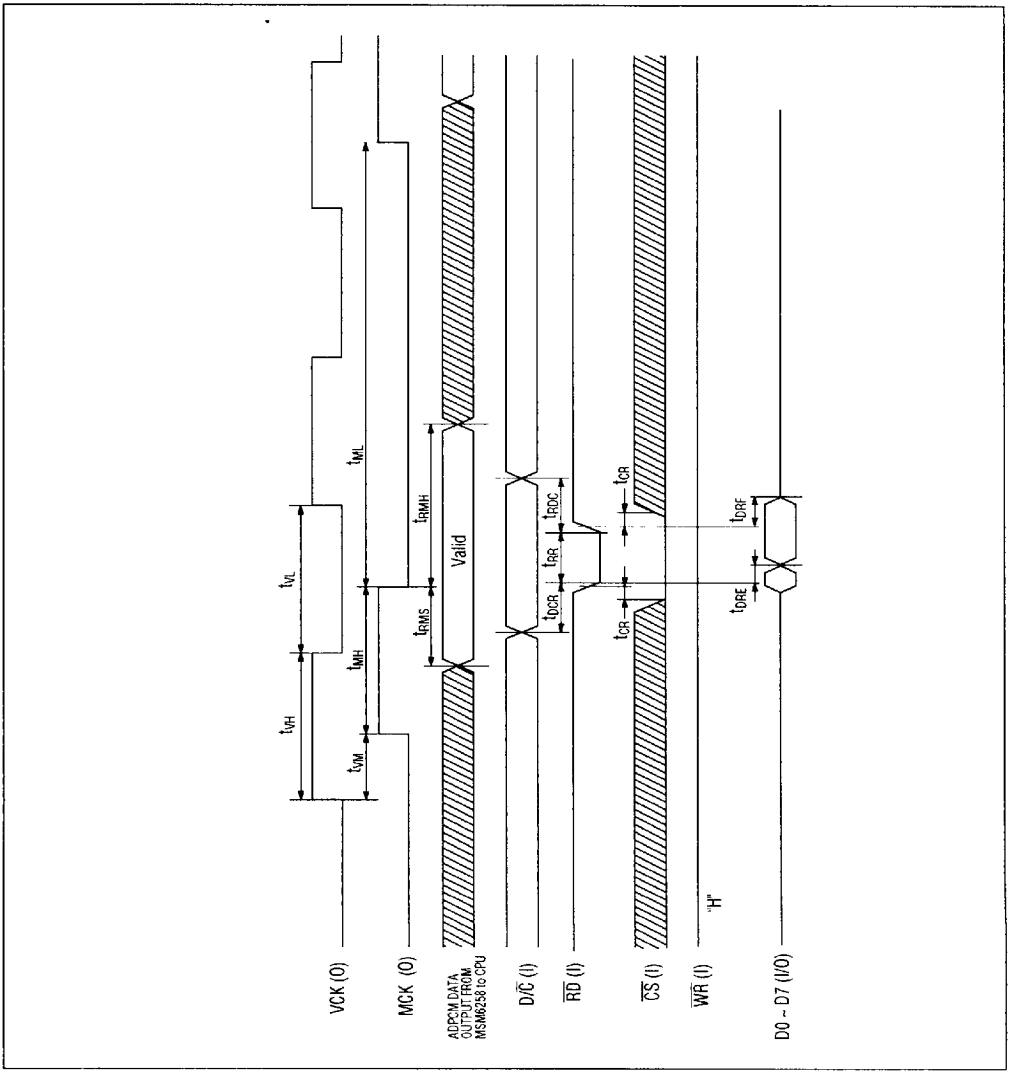
- **PLAYBACK TIMING** (with SRAM selected)



2. CPU INTERFACE VERSION

- **READ TIMING** (with record or status output)

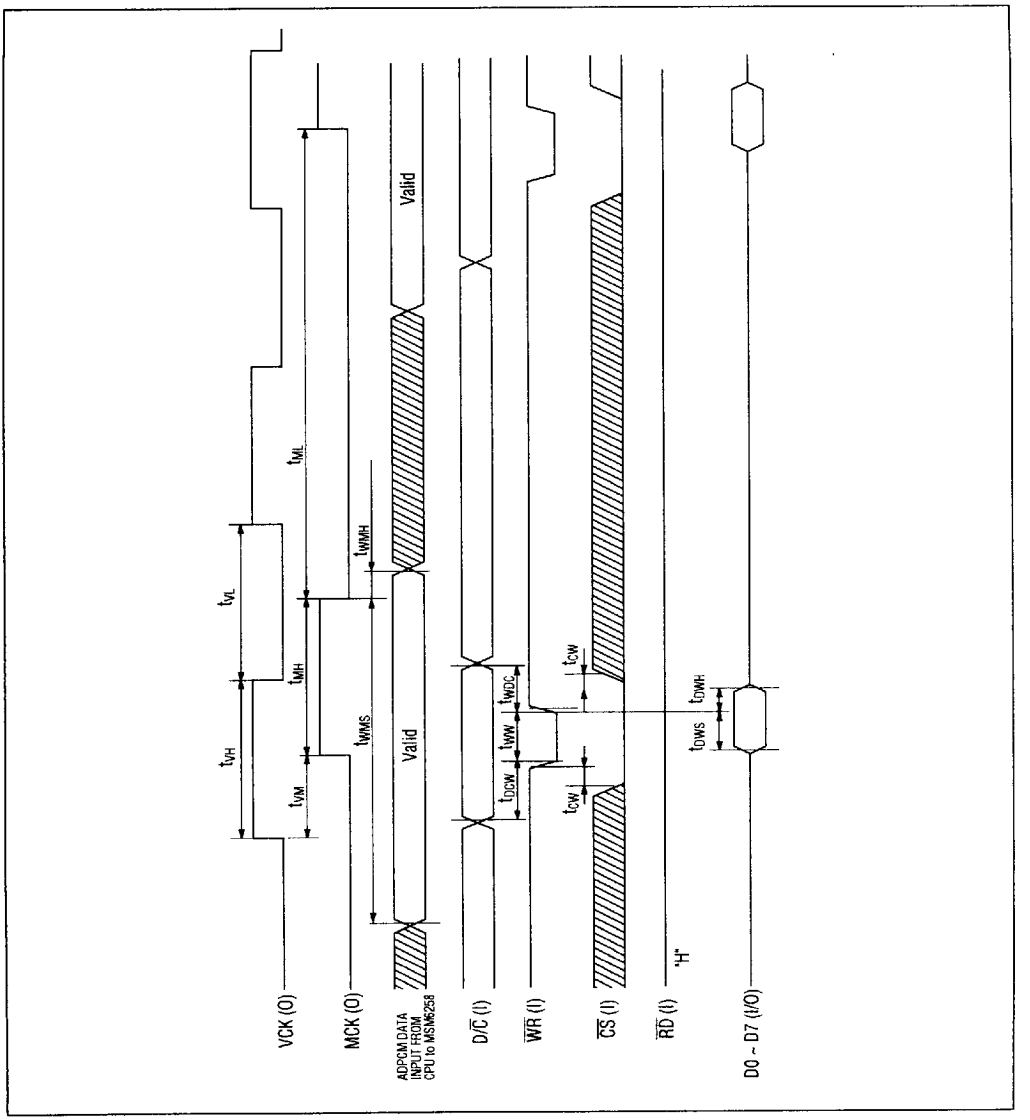
• **READ TIMING** (with record or status output)



Note Use the above valid section to reference ADPCM data output from the MSM6258 to CPU. Status reading may be performed anywhere.

- **WRITE TIMING** (with playback or command input)

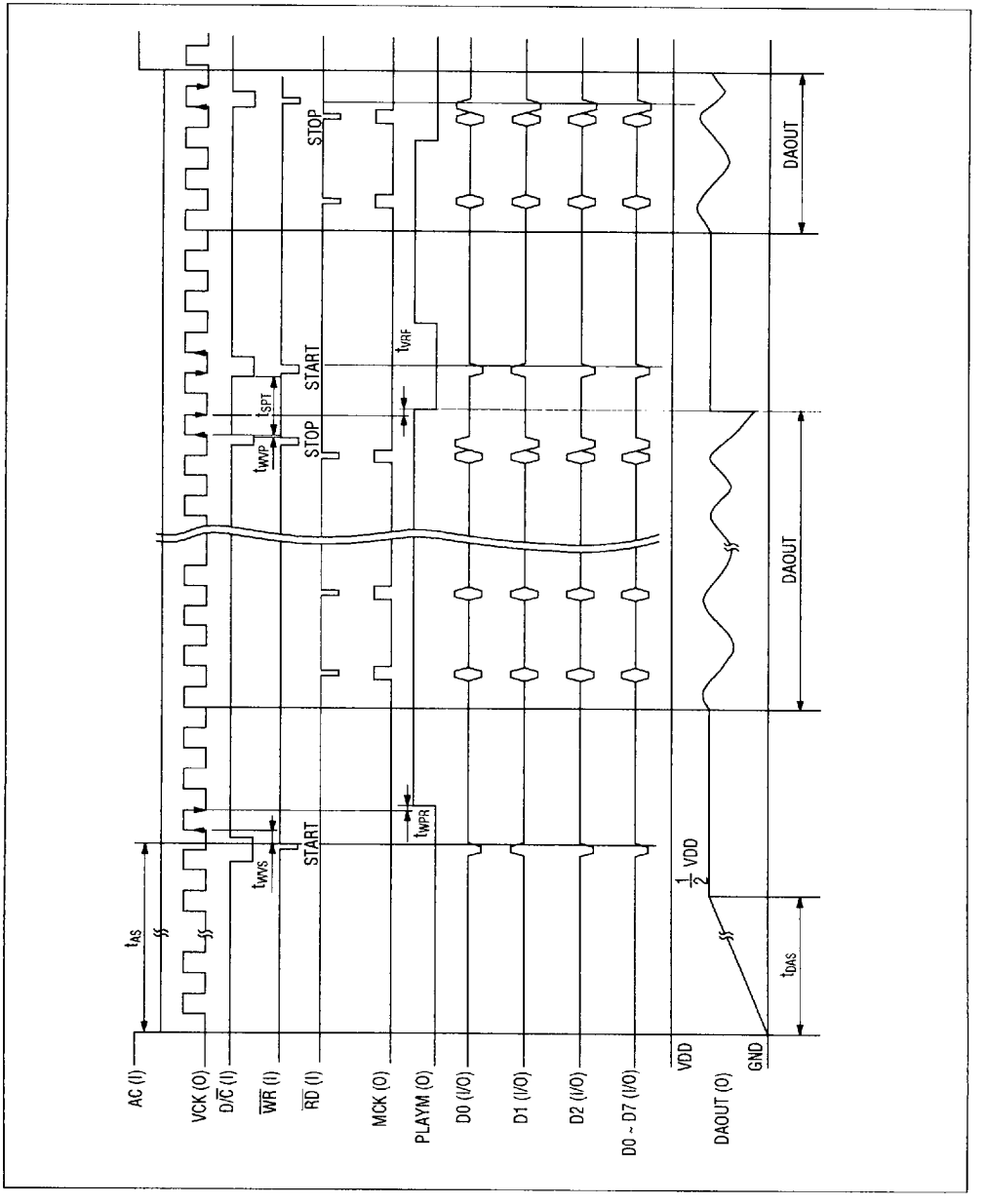
• **WRITE TIMING** (with playback or command input)



Note Use the above valid section to reference ADPCM data input from CPU to the MSM6258. Command write may be performed anywhere.

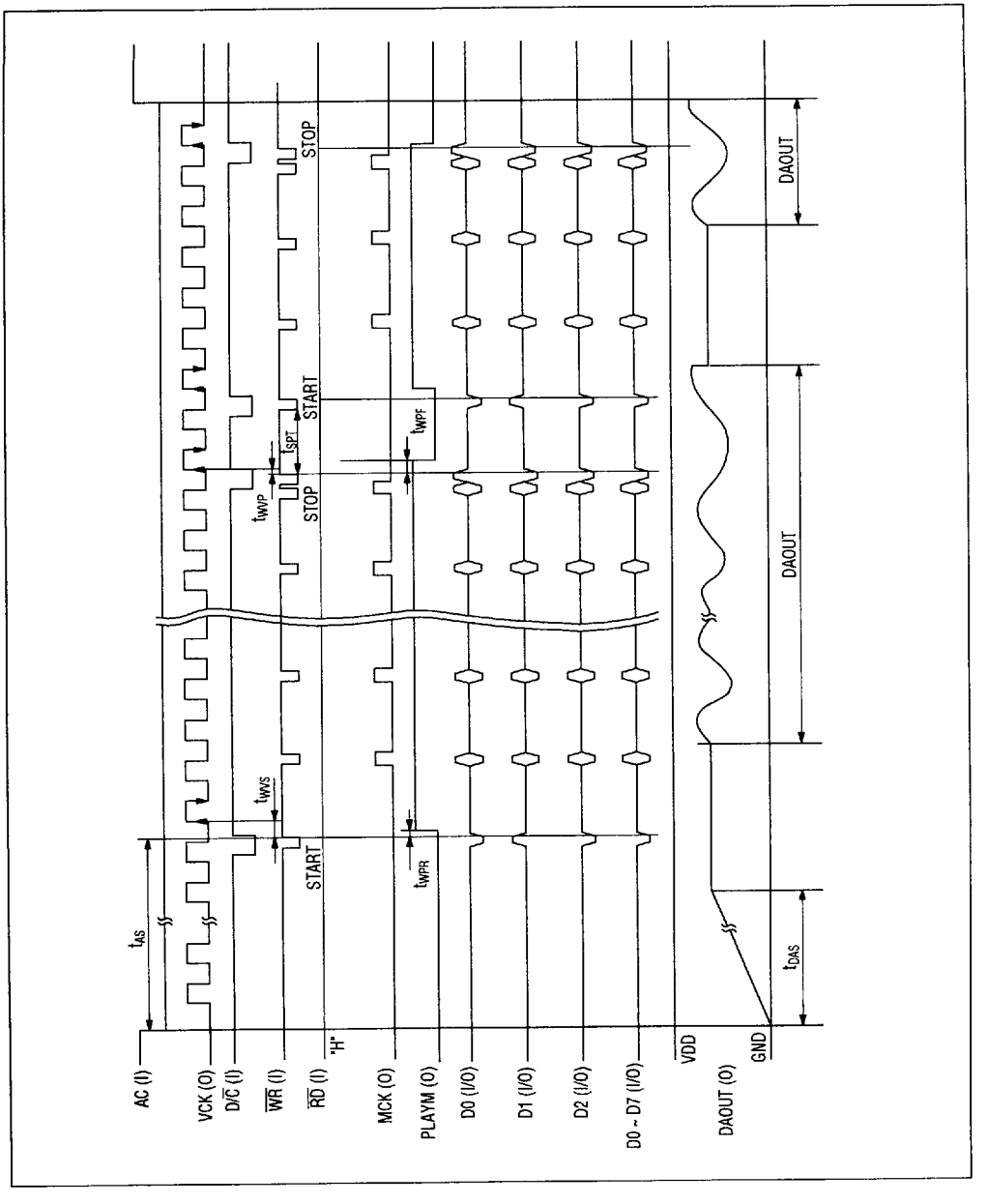
- **RECORD TIMING**

• RECORD TIMING



- **PLAYBACK TIMING**

• PLAYBACK TIMING



DESCRIPTION OF TERMINALS

1. Stand-Alone Version

Pin Name	I/O	Function
VDD	–	Power supply pin
VSS1	–	Digital GND pin
VSS2	–	Analog GND pin
AC (All Clear)	I	If the level of this pin is set to "H", the internal circuitry is set to the initial state. So, the output level of DAOUT is set to GND, the flag for each channel is reset to inhibit reproduction in channel 1 through channel 7 ; and oscillation is stopped if SRAM has been selected. The built-in power-on resetting circuit causes the level of this pin to go "H". For assurance, it is recommended to connect an external power-on resetting circuit.
REC/$\overline{\text{PLAY}}$	I	Selects recording or playing. If the level of this pin is set to "H", record mode is invoked. Do not change the input level of this pin during recording or playing.
ST•SP	I	Enables entry of pulses to start and terminate recording or playing. It is internally pulled down. A chatter prevention circuit is provided.
PAUSE	I	When momentarily connected to VDD, the record or playback operation is temporarily suspended. It is internally pulled down.
PLAYM (PLAY MONITOR)	O	Its output level is set to "H" during vocalization in play mode. Its output level is set to "L" during standby and record mode.
RECM (REC MONITOR)	O	Outputs "L", "H", and "2 Hz clock output" depending on the state of the LSI. In play or standby mode, its output level is set to "L". During recording, the level of this pin is set to "H". It outputs 2 Hz clock during detection of voice, and during pause.
DAOUT	O	Voice output pin. Voice is output during recording and playing. For reference, a muting circuit, which inhibits the output of voice during recording, is given in Figure 34. In standby mode, its level is set to GND level to make the power consumption of the speaker driving transistor null. At this time, pop noise is eliminated internally.
CA1~CA3	I	Specifies channels for recorded phrases or phrases to be reproduced. Up to eight channels can be specified. Do not change the input level of this pin during recording or playing.
OVF(FST) Overflow (Flag Status)	O	Outputs the flag status ("H" level if the selected channel has already been used for recording) for the selected channel in standby mode. Outputs "H" level pulses if the voice signal exceeds approximately 80% of the dynamic range in record or play mode.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>FRST
(FLAG RESET)</td><td>I</td><td>Setting the level of this pin to "H" resets the flag for the selected channel to inhibit reproduction in that channel.
The signal from this pin is valid only in standby mode. Do not set the level to "H" during recording or playing. A pull down resistor is used.</td></tr>
<tr><td>VDS
(Voice Detect Select)</td><td>I</td><td>In record mode, when VDS="H", this input determines whether the silence preceding the voice input is silence or voice and if voice then recording is started. This is called a "Voice Triggered Starting Circuit".</td></tr>
<tr><td>SAM1
SAM2</td><td>I</td><td>Selects a sampling frequency.
If the original oscillation frequency is 4.096 MHz, a sampling frequency is selected as shown below:
<table>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>fs</td><td>4.0kHz</td><td>5.3kHz</td><td>8.0kHz</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>4B/$\overline{3B}$</td><td>I</td><td>Selects bit length for ADPCM. "H" stands for 4-bit, and "L" stands for 3-bit.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>This bi-directional data bus conveys the ADPCM-coded data to and from the memory. One byte consists of two nibbles in the 4-bit ADPCM data format. In the case of 3-bit data format, two nibbles are presented, but the LSB of each is always externally pulled-down. The MSB of every nibble indicates whether the input waveform is ascending (MSB=0) or descending (MSB=1). D0 to D7 output or input a pair of ADPCM nibbles during every sampling period, which is VCK.</td></tr>
<tr><td>D/$\overline{SRAM}$</td><td>I</td><td>Selects either DRAM or SRAM. Set the level to "H" if DRAM is to be used.</td></tr>
<tr><td>RAMS1
RAMS2
(RAM SIZE SELECT)</td><td>I</td><td>According to the type of memory connected, do the following settings:
<table>
<tr><th>D/$\overline{SRAM}$</th><th>RAMS1</th><th>RAMS2</th><th>Connectable memory</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>64K × 1-bit (64K DRAM)
64K × 4-bit (256K DRAM)</td></tr>
<tr><td></td><td>H</td><td>L</td><td>256K × 1-bit (256K DRAM)
256K × 4-bit (1M DRAM)</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1M × 1-bit (1M DRAM)</td></tr>
<tr><td></td><td>H</td><td>H</td><td>Inhibited.</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>64K SRAM, 64K ROM</td></tr>
<tr><td></td><td>H</td><td>L</td><td>256K SRAM, 256K ROM</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>*SRAM, EPROM, Madk ROM</td></tr>
<tr><td></td><td>H</td><td>H</td><td>Internal RAM access mode</td></tr>
</table>
* Address pins A0 through A18 output binary data.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>A0 ~ A18</td><td>O</td><td>External memory address pins and chip select pins.
Depending on the type of memory, pins A0 through A18 are used as shown below. In standby mode, the address pins output "L" level signals, and the chip select terminals output "H" level signals.
<table>
<tr><th colspan="2">Type of memory</th><th>Maximum q'ty</th><th>Address pin(*2)</th><th>Chip select pin</th></tr>
<tr><td rowspan="3">DRAM</td><td>64K × 1-bit
64K × 4-bit</td><td>11 sets
(*1)</td><td>A0 ~ A7</td><td>A8 ~ A18</td></tr>
<tr><td>256K × 1-bit
256K × 4-bit</td><td>8 sets
(*1)</td><td>A0 ~ A8</td><td>A9 ~ A16</td></tr>
<tr><td>1M × 1-bit</td><td>2 sets
(*1)</td><td>A0 ~ A9</td><td>A10 ~ A11</td></tr>
<tr><td rowspan="2">SRAM</td><td>8K × 8-bit (64K)</td><td>6</td><td>A0 ~ A12</td><td>A13 ~ A18</td></tr>
<tr><td>32K × 8-bit (256K)</td><td>4</td><td>A0 ~ A14</td><td>A15 ~ A18</td></tr>
</table>
(*1) A set consists of six or eight DRAMs for one-bit data input/output. A set consists of two DRAMs for 4-bit data input/output.
(*2) If RAMS1 and RAMS2 are set to select binary output, A0 through A18 are all used as address pins.</td></tr>
<tr><td>VCK
(Voice Clock)</td><td>O</td><td>This pin outputs the selected sampling frequency.</td></tr>
<tr><td>XT
$\overline{XT}$</td><td>I
O</td><td>Oscillator connecting pin (4 MHz - 8 MHz)
If external clock signal is to be used, enter it through the XT pin with the $\overline{XT}$ pin open.</td></tr>
<tr><td>IAD/$\overline{EAD}$
(Internal AD/
Externla/AD)</td><td>I</td><td>Determines whether the built-in ADC is used or not. Entry of "H" level signal enables the use of the built-in ADC.</td></tr>
<tr><td>VI (SICK)</td><td>I</td><td>If the built-in ADC has been selected, this pin functions as V1 (analog signal input) pin. If the external ADC has been selected, it functions as SICK (serial clock input to read PCM data before AD conversion into LSI) pin.</td></tr>
<tr><td>VR (ADSI)</td><td>I</td><td>This pin functions as VR (AD converter reference voltage input terminal) pin if the built-in ADC has been selected. If the potential of VR is made equal to that of VDD, the input level for V1 and the output level for DAOUT become almost equivalent. If the external ADC has been selected, this pin functions as ADSI (serial input of PCM data after AD conversion) pin.</td></tr>
<tr><td>SOCK</td><td>O</td><td>Serial output clock. Used to output PCM data before DA conversion to the outside of LSI.</td></tr>
<tr><td>DASO</td><td>O</td><td>Output pin used to output serial PCM data before DA conversion to an external D/A.</td></tr>
</table>

Pin Name	I/O	Function
$\overline{RAS}$ ($\overline{OE}$)	O	DRAM and SRAM control timing output pin. It functions as RAS if DRAM is selected, and functions as OE if SRAM is selected. In standby mode, OE outputs "H" level signal.
$\overline{CAS}$	O	pin enabling the monitoring of CAS signal to DRAM. Do not directly connect this terminal to CAS pin on DRAM, but connect it to the chip select pins (A8 through A18).
$\overline{WE}$	O	This pin outputs timing signals used to control reading from and writing to DRAM and SRAM. It outputs "H" level signals in play or standby mode.

2. CPU Interface Version

Pin Name	I/O	Function
VDD	–	Power supply pin
VSS1	–	Digital GND pin
VSS2	–	Analog GND pin
MPU	I	If ther level of this pin is set to "H", LSI is switched to CPU interface. Since this input is internally pulled-down, be sure to apply a "H" level to this pin.
MCK (Main Clock)	O	Outputs signal for synchronization with CPU. During recording and playing, a frequency equivalent to 1/2 of the sampling frequency is output.
VCK (Voice Clock)	O	Outputs the selected sampling frequency. While the level of AC is set to "L", a sampling frequency is always output.
AC (All Cler)	I	Setting the level of this pin to "H" sets LSI to initial state, and sets the output level of DAOUT to GND. The built-in power-on resetting circuit sets AC to the "H" level temporarily when power is turned on. For assurance, however, it is recommended to connect an external power-on resetting circuit.
D0 ~ D7	I/O	These pins input and output ADPCM data, command data, and status data.
$\overline{CS}$ (Chip Select)	I	Setting the level of this pin to "L" enables data transfer with CPU. When setting the level of this pin to "H", data bus (D0 ~ D7) become high impedance, inhibiting reading and writing through the data bus.
$\overline{RD}$ (Read)	I	Setting this pin to the "L" level enables the CPU to read ADPCM data and status data from the MSM6258.
$\overline{WR}$ (Write)	I	Enables writing of ADPCM data and command data from the CPU to the MSM6258 at the rising edge of $\overline{WR}$.

Pin Name	I/O	Function
D/$\overline{C}$ (Data/Command)	I	Setting this pin to the "H" level sends ADPCM data through the data bus (D0 ~ D7). Setting it to the "L" level sends command data or status data through the data bus.
RECM (Record Monitor)	O	during recording, this pin outputs a "H" level signal.
PLAYM (Play Monitor)	O	During playback, this pin outputs a "H" level signal.
IAD/$\overline{EAD}$ (Internal AD/ External AD)	I	Makes a selection to use the build-in AD converter or an external AD converter. Setting the pin to the "H" level enables the use of the built-in AD converter.
VI (SICK) Voice in serial In Clock	I	Setting IAD/$\overline{EAD}$ to the "H" level causes this pin to function as analog signal input pin (VI). Setting IAD/$\overline{EAD}$ to the "L" level causes this pin to function as a serial input clock (SICK), which enables loading of PCM data after AD conversion into the LSI.
VR(ADSI) (Voltage Reference AD DATA Serial IN)	I	Setting IAD/$\overline{EAD}$ to the "H" level makes this pin function as AD converter reference voltage input pin (VR). If VR and VDD are made common, the input level of VI becomes equivalent to the output level of DAOUT. Setting IAD/$\overline{EAD}$ to the "L" level makes this pin function as input pin for serial PCM data subject to AD conversion.
DAOUT	O	Voice output pin. If outputs voice during recording and playing. For reference, an example of a muting circuit which inhibits voice output during recording is given in Figure 34. Setting AC to the "H" level sets the level of this terminal equivalent to the GND level. Changing AC from the "H" to "L" level gradually increases the level until it reaches 1/2 VDD.
SOCK (Serial Out Clock)	O	This pin outputs a clock used to output serial PCM data for external DA conversion.
DASO (DA Data Serial Out)	O	This pin outputs serial PCM data for external DA conversion.
4B/$\overline{3B}$ (4-bit/3-bit)	I	ADPCM bit length selection pin. Setting it to the "H" level makes the data bus (D0 ~ D7) send 4-bit ADPCM data. Setting the terminal to the "L" level makes the data bus send 3-bit ADPCM data.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>SAM1
SAM2
(Sampling 1,2)</td><td>I</td><td>Sampling frequency selecting pin.
If the original oscillaiton frequency is 4.096 MHz, any of the following sampling frequencies can be selected:
<table>
<tr><td>SAM1</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>SAM2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>fs</td><td>4.0kHz</td><td>5.3kHz</td><td>8.0kKz</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>OVF (Overflow)</td><td>O</td><td>This pin outputs a "H" level signal if voice signal reaches more than 80% of the dynamic range during reocrding and playing. It outputs a "H" level signal in any mode other than record and play modes.</td></tr>
<tr><td>XT
$\overline{XT}$</td><td>I
O</td><td>Oscillator connecting pin.
If an external clock is to be used, enter it through the XT pin with the $\overline{XT}$ pin open.</td></tr>
<tr><td>VDS
ST•SP
REC/$\overline{PLAY}$
TDS
TRS 1
TRS 2
PAUSE</td><td>I</td><td>Set all these pins to the GND level.</td></tr>
</table>

DESCRIPTION OF FUNCTIONS

• Recording Time and RAM Capacity

Recording time varies with the capacity of external RAM, sampling frequency, and ADPCM bit length. Their relations are given by the following expression:

$$\text{Recording time (sec.)} = \frac{1.024 \times \text{RAM capacity (K-bit)}}{\text{Sampling frequency (kHz)} \times \text{bit length (3 or 4)}}$$

If two 256K DRAMs are used with the sampling frequency set to 4 kHz, and with ADPCM bit length set to 4-bit, recording can be performed for 32.7 seconds as calculated below:

$$\text{Recording time (sec.)} = \frac{1.024 \times 256 \text{ (K-bit)} \times 2}{4 \text{ (kHz)} \times 4 \text{ (bit)}} = 32.7 \text{ seconds}$$

• Analog Input

1. Waveform Input to VI

The analog input (voice waveform) to VI should be so designed to oscillate around 1/2VR. The maximum amplitude can equal VR.

As the input amplitude approaches VR, S/N during AD conversion is improved. Therefore, it is recommended to set the input amplitude in the range between 1/2VR and VR.

2. Conversion Method & Impedance of Analog Input to VI

MSM6258 employs an AD converter of the load comparison type, which uses a capacitor.

The VI terminal is connected to the internal capacitor for 8 μs each time the sampling frequency is given (125 μs for 8 kHz sampling), and disconnected from it for the rest of the time. So, input equivalent impedance varies with the frequency of the input waveform, ambient temperature, etc. by 10 k-ohms to more than several tens of M-ohms. Therefore, design should be performed so as to connect a low impedance output circuit to the VI terminal. The capacity of the internal capacitor is 100 - 200pF.

3. Input Filter Section

The low pass filter located before the VI terminal eliminates the repeated noise during AD conversion. The cutoff frequency should generally be set to 0.8 x 1/2 to 1/2 of the sampling frequency.

For the construction of the filter, refer to "Q&A" of this data book.

• Analog Output

1. Output Waveform from DAOUT

The maximum amplitude of the output from DAOUT is 1023/1024 x VDD The waveform is a stair step waveform synchronous with the sampling frequency.

Input/output waveform for the VI, VR, and DAOUT terminals are illustrated below:

2. Output Filter Section

Because the output from DAOUT is a stair step waveform, add a low pass filter.

The output impedance of DAOUT varies in the range between 12 kΩ and 22 kΩ

Determine a filter constant so that resistance variations caused by the change of the output impedance may not affect the cutoff frequency for the filter.

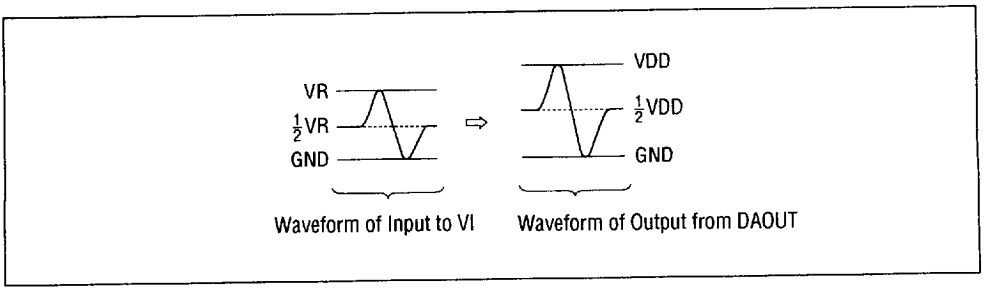


Figure 1

- **Use of External AD and DA Converters**

To establish a high quality recording/playing system, a 12-bit AD and 12-bit DA converters can be externally mounted.

1. Use of External AD Converter

Enter data, which has underwent straight binary conversion with the AD converter, to ADSI, and enter clock signal through SICK.

Read data from ADSI at the rise of SICK. Figure 2-1 shows the timing:

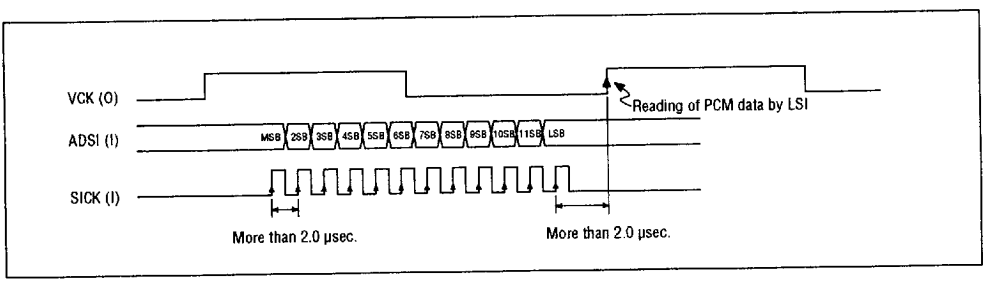


Figure 2-1 Use of External AD Converter and Timing

2. Use of External DA Converter

According to the timing of DASO and SOCK shown in Figure 2-2, straight binary data and clock are output. The data from DASO changes at the rise of SOCK.

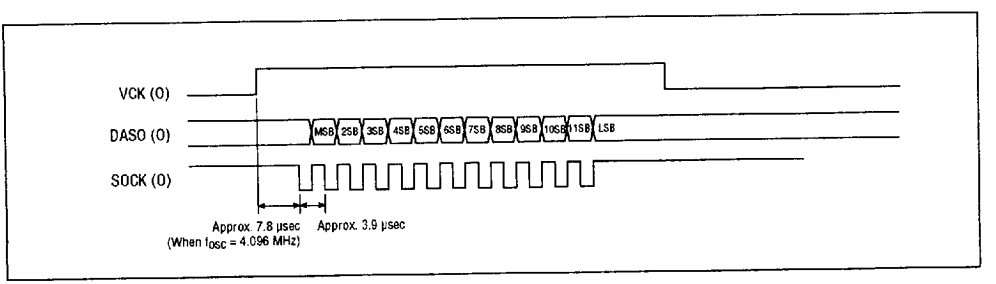


Figure 2-2 Use of External DA Converter and Timing

- **Original Oscillation Frequency and Sampling Frequency**

1. Relationship between the Original Oscillation Frequency and the Sampling Frequency

The LSI can use an original oscillation frequency in the range between 4 and 8MHz. The sampling frequency (fs) can be selected as shown in the table below:

Table 1 Relationship between SAM1, SAM2 and Sampling Frequency

SAM1	L	H	L	H
SAM2	L	L	H	H
fs	$\frac{f_{osc}}{1024}$	$\frac{f_{osc}}{768}$	$\frac{f_{osc}}{512}$	Inhibited

f_{osc} : Original oscillation frequency

2. Connection of Oscillator

Figure 3 illustrates how to connect an oscillator. For reference, the optimum capacity when a Kyocera-produced ceramic oscillator is connected to XT and $\overline{XT}$ is shown in the table below. If a Murata Seisakusho-produced ceramic oscillator is to be used, connect 30pF to C1 and C2.

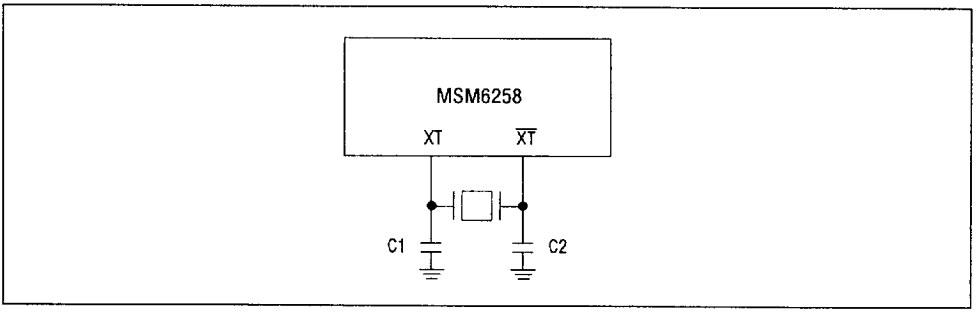


Figure 3 Connection of Oscillator

Ceramic oscillator		Optimum capacity	
Model	**Frequency (kHz)**	**C1 (pF)**	**C2 (pF)**
KBR-4.0MS	4000	33	33
KBR-4.096MS	4096	33	33
KBR-5.0MS	5000	33	33
KBR-6.0 MS	6000	33	33
KBR-8.0 MS	8000	22	22

- **Relationship between D0-D7 and ADPCM Data**

Table 2 Relations between D0-D7 and ADPCM Data

D0	D1	D2	D3	D4	D5	D6	D7	
B0n	B1n	B2n	B3n	B0n+1	B1n+1	B2n+1	B3n+	← 4-bit ADPCM
*	B0n	B1n	B2n	*	B0n+1	B1n+1	B2n+1	← 3-bit ADPCM

4-bit ADPCM
- B3n ..... Polarity bit for n-th sampling
- B2n ..... MSB for n-th sampling
- B1n ..... 2SB for n-th sampling
- B0n ..... LSB for n-th sampling

3-bit ADPCM
- B2n ..... Polarity bit for n-th sample
- B1n ..... MSB for n-th sampling
- B0n ..... LSB for n-th sampling
- * ..... Pull down when the resistance reaches approximately 100 k-ohms.

As shown above, data D0 through D3 precedes data D4 through D7.

To prepare ADPCM data for MSM6295 or to perform reproduction using ADPCM data, connection must be changed to exchange D0-D3 with D4-D7.

- **Operation for Stand-Alone Version**

1. Power Saving Function

When SRAM is selected, the power saving function for the LSI is activated to stop oscillation in standby mode (in any mode other than record or play mode).

It may sometimes take 20 to 30 msec. before oscillation is stabilized.

To shorten the stabilizing time, it is recommended to use a ceramic oscillator.

2. Basic procedure for recording and playing

Basic procedure for recording and playing using channel 1 is described in this section. Recording and playing can be done very easily.

2.1 Recording

Set the REC/$\overline{\text{PLAY}}$ terminal to record mode, and select channel 1 using CA1 through CA3. Enter a pulse to the ST•SP terminal, and recording begins. To terminal recording, enter a pulse to the ST•SP terminal again. Recording is done between these two pulses. If 8kHz sampling is selected, recording time can be extended by up to 64ms (equivalent to 2k-bit). Figure 4 shows the relations between ST•SP and recording time.

In the initial state, recording is not terminated automatically. So, it is necessary to enter a pulse for termination.

2.2 Playing

Playing begins if the REC/$\overline{\text{PLAY}}$ terminal is set to play mode, and a pulse is entered to the ST•SP terminal. When recording time is reached, playing is terminated automatically. To suspend playing half way, enter a pulse to the ST•SP terminal again. Figure 5 shows the relationship between ST•SP and playing time.

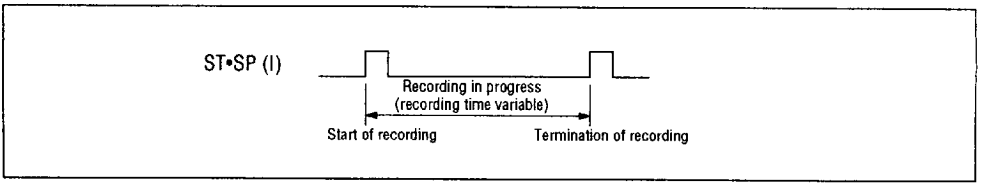


Figure 4 Recording Sequence

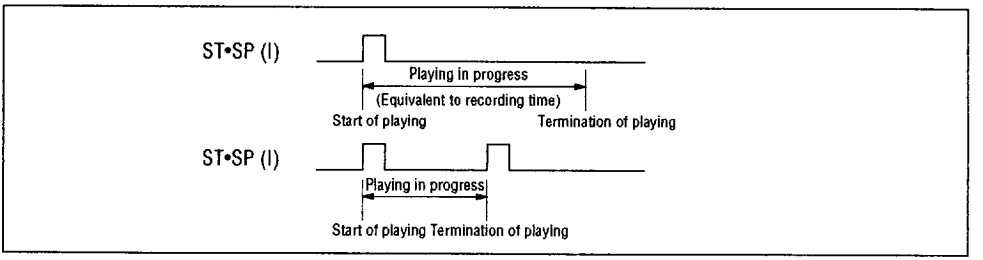


Figure 5 Playing Sequence

3. Use of Channels

MSM6258 allows selection of eight channels: channel 0 through channel 7. Each channel has flag status (FST). Use of the channels is described below.

3.1 Initial Recording conditions of channels 1 through 7 and external RAM

To start recording in the initial state (nothing is recorded in any channel), channel 1 through channel 7 must be used in that order. Table 3 shows the channels and their addresses.

The external RAM after completion of recording in channel 1 through 7 is demarcated in proportion with recording time in 2 K-bit steps. The length of each channel can be freely set so far as the capacity of the external RAM allows. Figure 6 shows an example. FST for the channel that was used for recording is set to the "H" level.

3.2 Use of Channel 0

If channel 0 is selected, FST is always set to the "H" level, and the data saved beginning with the start address of the external RAM. This is helpful if only one word is to be recorded in the external RAM or if voice data written to EPROM or masked ROM is to be reproduced. (See an example of an applied circuit in Figure 27.)

To terminate recording or playing, enter a stop pulse to the ST•SP terminal.

Do not forget to set the VDS terminal to the "L" level.

Table 3 Channels and Addresses

Channel	Channel address		
	CA1	CA2	CA3
0	L	L	L
1	H	L	L
2	L	H	L
3	H	H	L
4	L	L	H
5	H	L	H
6	L	H	H
7	H	H	H

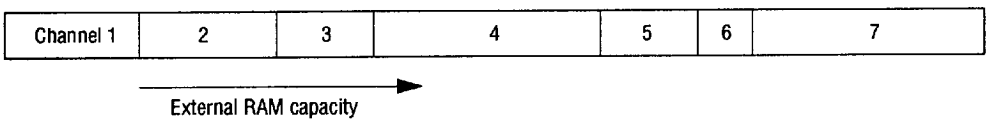


Figure 6 Example of External RAM and Channel Length

4. Recording/Playing and FST

The LSI enables selection of channels using CA1, CA2, and CA3. Each of channels 1 through 7 has flag status (FST). The relationship between recording/playing and FST are shown in Table 4:

Table 4 Relationship between recording/playing and FST

	FST = "L"	FST = "H"
Recording	a	b
Playing	c	d

a: Recording time is variable. Recording can be done according to the procedure described in 2.1. When the power is turned on, this status ensues.

b: Recording can be done for the time equivalent to that of the previous recording. Entry of a pulse to the ST•SP terminal starts recording, and terminates it automatically. A pulse entered during recording is invalid. Without external control of addresses, the data in the other channels is preserved as illustrated in Figure 7. However, if VDS is set to the "H" level, recording time can become 0.12 second shorter.

c: Playing is inhibited. When the power is entered, this status ensues.

d: Recording is possible. For recording, follow the procedure described in 2.2.

Notice that FST for channel 0 is always set to the "H" level.

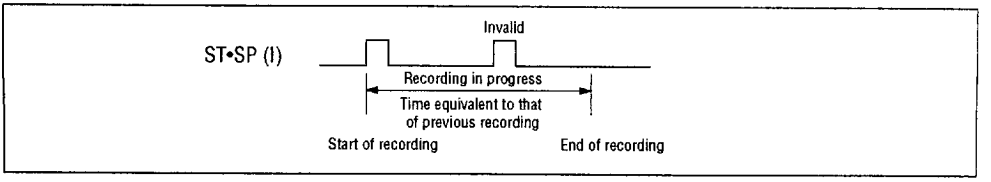


Figure 7 Recording in Status B (Preservation of Data in Channel)

5. Function of Pause Terminal

5.1 Two Pauses after Start

Entering a pulse to the PAUSE terminal temporarily stops a record or play operation.

Entering a pulse again re-starts the paused record or play operation.

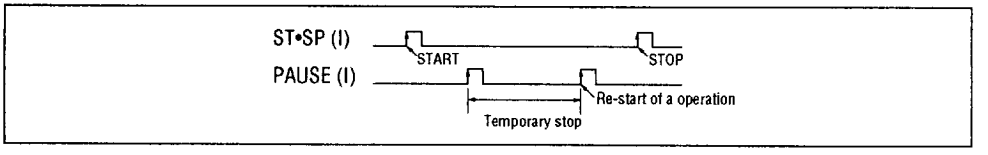


Figure 8

5.2 One Pause after Start

If a pause is invoked once after start, the stop pulse has preference.

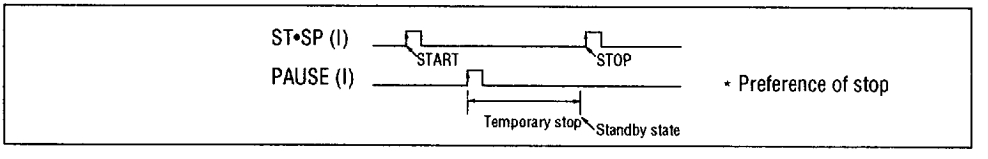


Figure 9

5.3 Pause in Standby Mode

A pause is invalid.

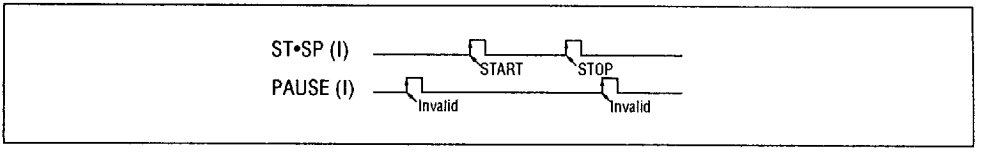


Figure 10

6. Recording

(1) Set the selecting terminals (SAM1, SAM2, ETC.).

(2) Set the REC/PLAY terminal to the "H" level.

(3) Set the channel address terminals CA1 through CA3, and check the OVF (FST) terminal to make sure of the flag status for the channel selected.

If the level of the output from OVF (FST) is "H", it means that data is already recorded in the selected channel. If it is "L", no data is recorded in the selected channel.

(4) Enter a pulse to the ST•SP terminal to start recording.

If the flag of the selected channel is set to "H", recording is automatically terminated when the recording time saved in the selected channel is reached. In this case, entry of a pulse from the ST•SP terminal does not terminate recording half way.

If the flag for the selected channel is "L", a pulse can be entered for the ST•SP terminal to terminate recording.

7. Playing

(1) Set the REC/PLAY terminal to "L".

(2) Set a channel desired to play using the CA1 through CA3 terminals.

(3) Make sure that the OVF (FST) terminal is "H". (If it is "L", playing is not possible.)

(4) Enter a pulse from the ST•SP terminal, and playing begins.

(5) When playing for the selected channel is completed, playing stops automatically.

(6) To terminate playing half way, enter a pulse from the ST•SP terminal.

8. Re-Recording (with Recording length Changed)

MSM6258 has a function to protect the contents in channels other than the one that is selected. To change the recording length for a certain channel, the protection function must be cleared using the flag reset (FRST) terminal.

Suppose recording is done with channels 1 through 4 in the external RAM as shown in Figure 11(a). Let us see how to change the recording lengths for channels 2 thorough 4.

First select channel 2, and reset it using the flag FRST for channel 2. (See Figure 11(b)).

Perform re-recording in channel 2. Because FST is set to "L", pulses have to be entered to the ST•SP terminal to set the start and end of recording. If the recording time for channel 2 is made longer than before, FST for channel 3 is automatically set to "L". At the same time, reproduction for channel 3 is inhibited. (See Figure 11(c).)

In an example shown in figure 11 (d), channel 3 is selected, and re-recording is done so as not to trespass the area of channel 4.

Figure 11 (e) shows an example in which the flag for channel 4 is reset, and re-recording done in channel 4.

In this manner, the external RAM is efficiently used for the channels of the MSM6258.

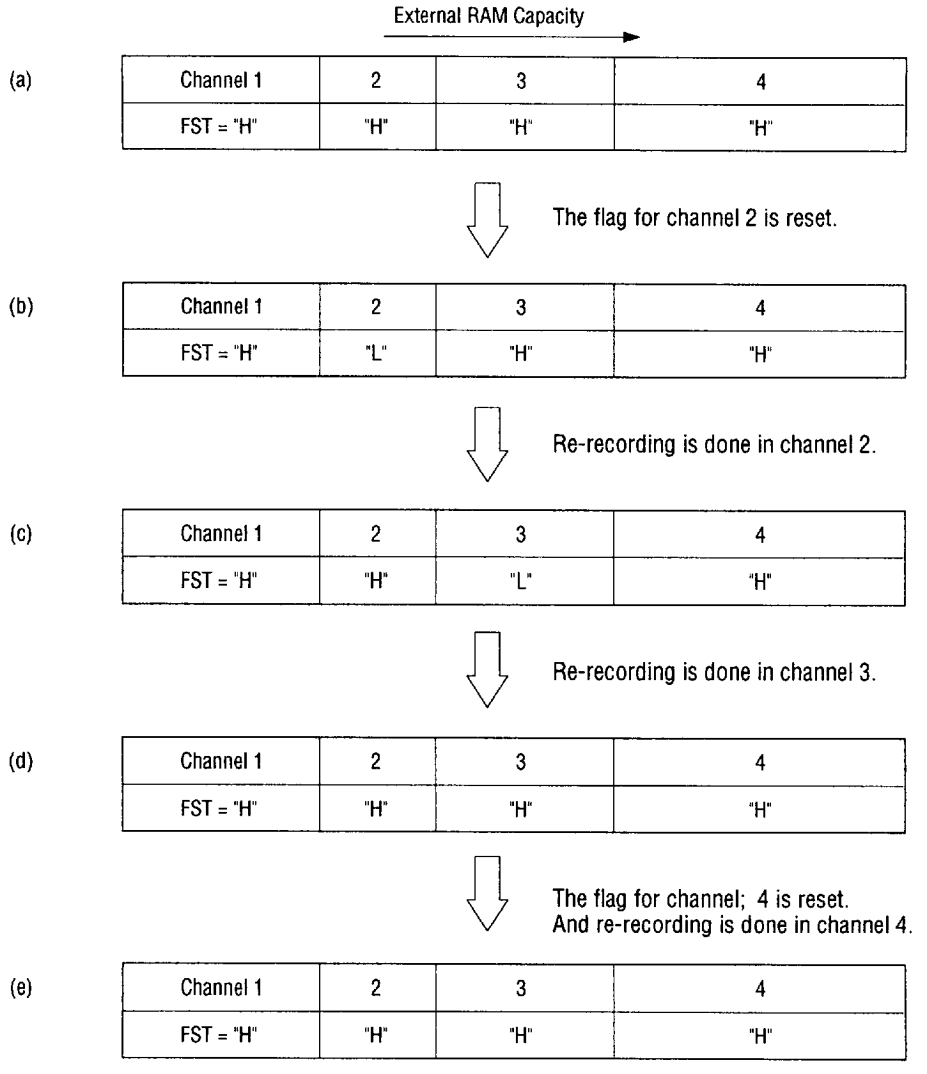


Figure 11 Re-Recording (examples in which recording lengths are changed)

9. Voice Starting

Setting the VDS terminal to "H" activates the voice triggered starting circuit. The circuit decides that there is voice if the difference between the input amplitude for the (n-1)-th sampling and that for the n-th sampling reaches a certain value, and if the number of occurrences reaches a certain value. Saving of ADPCM data in the external RAM begins 64-128 mseconds (fosc=4.096MHz, and fs=8.0kHz) after that time.

10. Access to Internal RAM

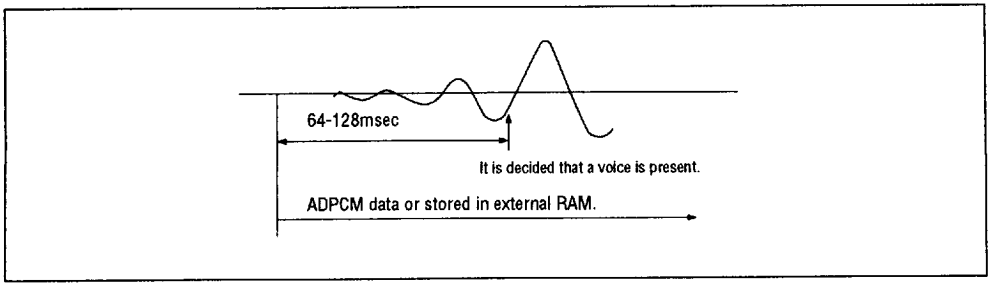


Figure 12 Outline of Voice-Triggered Starting

The start address and stop address for each channel are stored in the internal RAM in MSM6258.

The start/stop addresses for each channel can be changed by writing data to RAM inside the MSM6258.

Using this function, a certain word can be reproduced by externally connecting masked ROM or EPROM. (See an example of circuit shown in Figure 28.)

Procedure for writing the start/stop addresses for channel 1, and time chart are described below:

10.1 Procedure for Writing Start/Stop Addresses

(1) Set RAMS1 to "H", and D/$\overline{\text{SRAM}}$ to "L",

RAMS2 to "H", and REC/$\overline{\text{PLAY}}$ to "L"

Then, the internal RAM can be directly accessed.

(2) Set CA1 to "H", CA2 to "L", and CA3 to "L" to select channel 1.

(3) Set D4 to "L" to invoke start address write mode.

(4) Enter address data to D0, read clock signals (18) to D1, and write signal to D5.

(5) Set D4 to "H" to invoke stop address write mode, and follow the step (4) above again.

Then, the flag status for channel 1 is set to "H".

10.2 Timing Chart

Figure 13 shows a timing chart.

10.3 Control of Addresses in External Memory

RAM inside MSM6258 controls the start/stop addresses of the external memory. Figure 14 shows the outline of the circuit.

In Figure 14, the internal addresses are total 21-bit: the low-order 8-bit and D0 through D12. However, the external addresses are 19-bit: A0 through A18.

If SRAM or ROM is externally connected, D11 and D12 for the internal addresses are not used externally.

Write addresses in all the thirteen bits D0 through D12 to write start/stop addresses in the internal RAM.

At this time, D0 through D12 correspond to A0 through A18 as follows:

D12	→	None
D11	→	None
D10	→	A18
|		|
D0	→	A8

If DRAM is connected, all the 21-bit of the internal addresses are output.

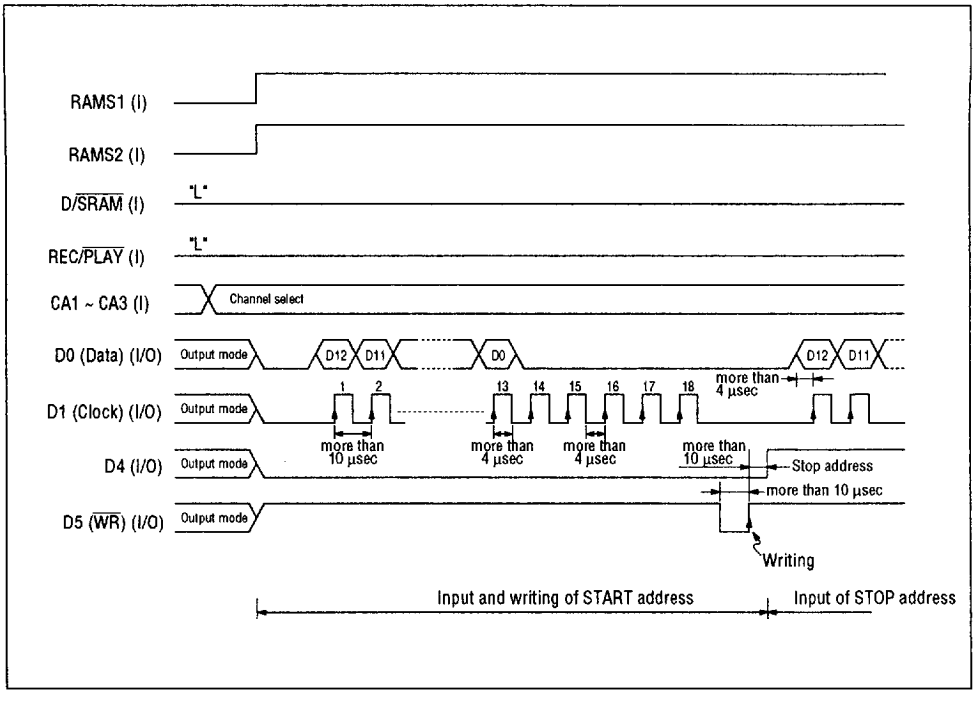


Figure 13

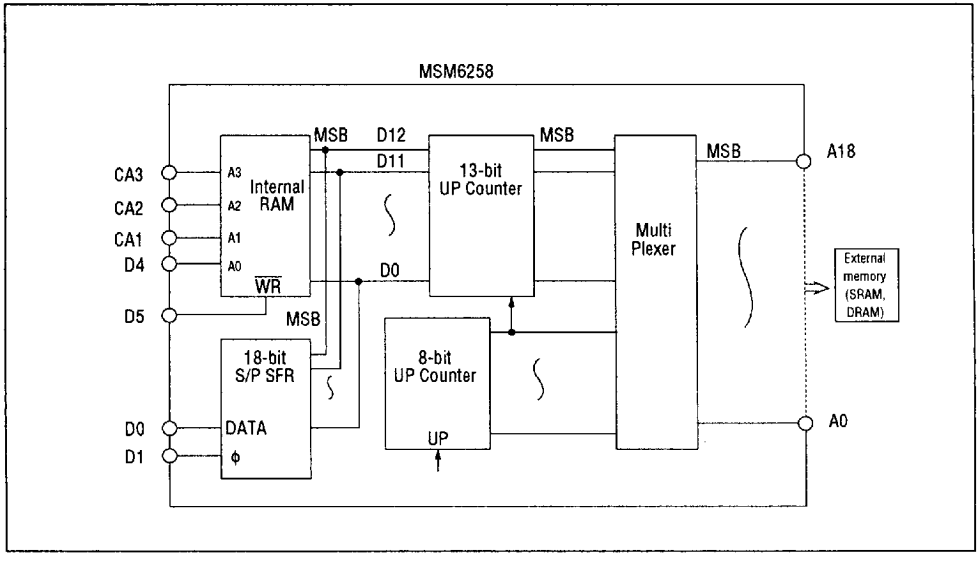


Figure 14

11. Connection and Use of DRAMS

11.1 Connection of DRAMs

64K × 1-bit, 64K × 4-bit, 256 × 1-bit, and 256 × 4-bit, and 1M × 1-bit DRAMs can be connected. MSM6258 allows the connection of up to 16 M-bit. Therefore, DRAMs can be added easily.

Use buffers if sixteen or more DRAMs are to be connected.

Figure 25 shows an example of a circuit in which four DRAMs are connected. As apparent from the figure, MSM6258 has eight data lines: D0 through D7. If the ADPCM bit length is 4-bits, ADPCM data is input and output through 8 data lines. ×4-bit DRAMs installed must be even in number, and the number of ×1 bit DRAMs must be a multiple of 8. If the ADPCM bit length is 3-bit, data is input and output through 6 data lines. So, the number of ×1-bit DRAMs installed must be a multiple of 6.

11.2 Use of DRAMs

DRAM is refreshed by "RAS only refresh" method. So almost any DRAM can be used. MSM6258 has the address terminals A0 through A18. If DRAM is used, the high order address outputs CAS signal, and it also works for chip selection.

Timing charts when 256 × 1-bit or 256 × 4-bit DRAMs are given in Figures 15, 16, and 17. These figures show timing for fosc=4MHz, and fs=7.8kHz.

11.3 Termination of Recording

If recording is started when FST is "L", recording is not terminated until a stop pulse is entered. If recorded data exceeds the capacity of the externally connected RAM, noise is generated when they are reproduced.

So, a stop pulse must be entered according to the RAM size. For this purpose, a timer may be used to control recording time, or chip select signal may be used.

Suppose two 256K × 4-bit DRAMs are connected. If a signal whose polarity is reverse to the signal from the chip select terminal A10 (shown in Figure 15) is entered to the ST • SP terminal as a stop pulse, recording is automatically terminated when recording has been done in two 1M DRAMs.

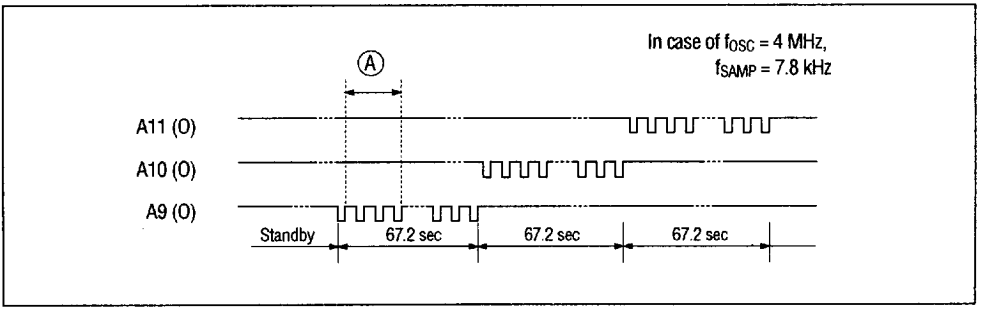


Figure 15 Address Timing for 256 x 4-Bit DRAM

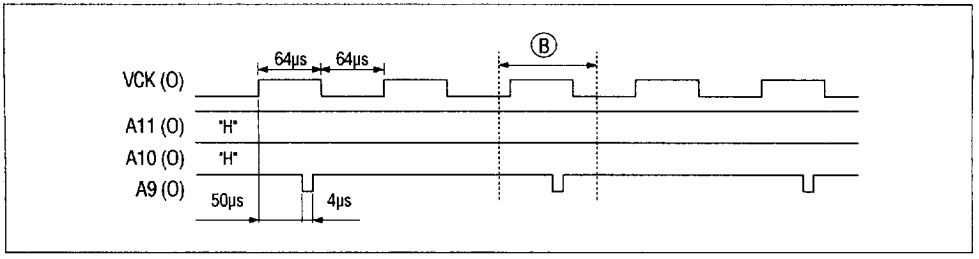


Figure 16 Enlarged View of A

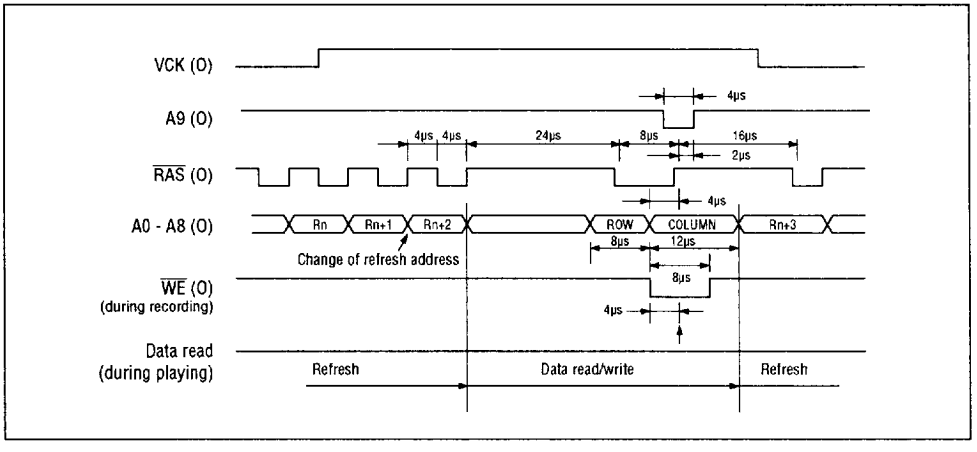


Figure 17 Enlarged View of B

12. Connection and Use of SRAMs

12.1 Connection of SRAMs

MSM6258 allows the direct connection of two types of SRAMs: 64K-bit and 256K-bit SRAMs. The maximum capacity of SRAMS that can be directly connected is 1M-bit (for 256K SRAMs).

The SRAM size can be expanded to up to 4M-bit if A0 through A18 are set for binary output using the RAMS1 and RAMS2 terminals, and a decoder is externally connected.

12.2 Use of SRAMs

Figures 18 and 19 show timing charts when 256K SRAM is selected.

The high-order address terminal automatically functions as a chip select terminal according to the type of SRAM.

These figures show timing when fosc is 4MHz, and fs is 7.8 kHz.

12.3 Recording Termination

If recording is started when FST is "L", recording is not terminated until a stop pulse is entered. If recorded data exceeds the capacity of the externally connected RAM, noise is generated when they are reproduced.

So,a stop pulse must be entered according to the RAM size. For this purpose, a timer may be used to control recording time, or chip select signal may be used.

Suppose two 256K SRAMs are connected. If a signal whose polarity is reverse to the signal from the chip select terminal A17 (shown in Figure 18) is entered to the ST•SP terminal as stop pulse, recording is automatically terminated when recording has been done in two 1M DRAMs.

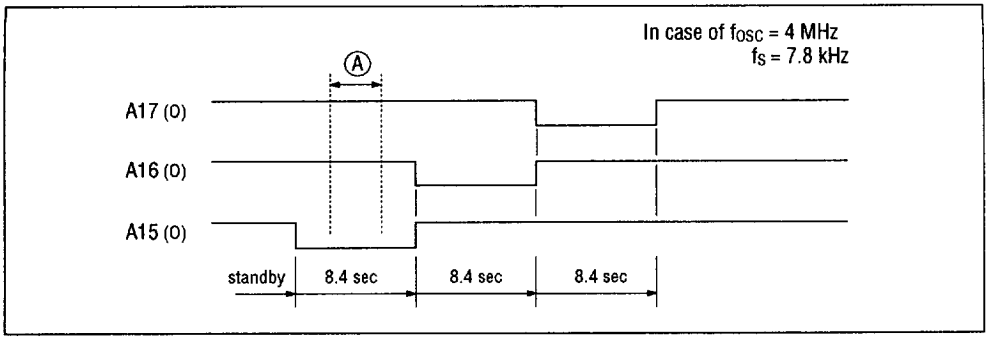


Figure 18 Address Timing for 256K SRAM

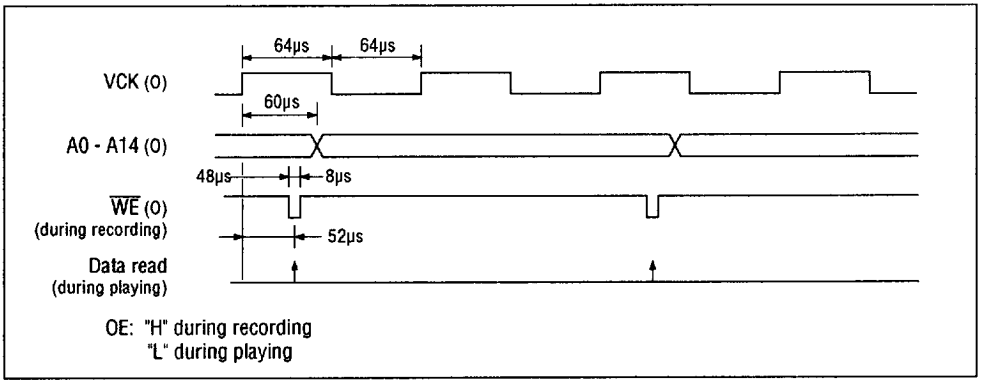


Figure 19 Enlarged View of A

13. Connection and Use of External ROMs

EPROM or masked ROM storing ADPCM data may be connected to reproduce either the entire contents of ROM or part of them.

13.1 Reproduction of Entire Contents of ROM

To reproduce the entire contents of External ROM, set the address to binary output mode using the RAMS1 and RAMS2 terminals, and enter a stop pulse to the ST•SP terminal within 50µs after the level of the A14 terminal is set to "H". Timing is shown in Figure 20.

Similarly, the contents of ROM can be easily reproduced by entering a stop pulse using the A15 terminal for 256K ROM, and the A16 terminal for 512K ROM.

13.2 Reproduction of Part of Contents of External ROM

By connecting ROM, to which many words of ADPCM data is written, to MSM6258, and controlling the internal RAM in MSM6258 using a microcomputer, individual words stored in ROM can be randomly reproduced. Figure 21 shows a flow chart.

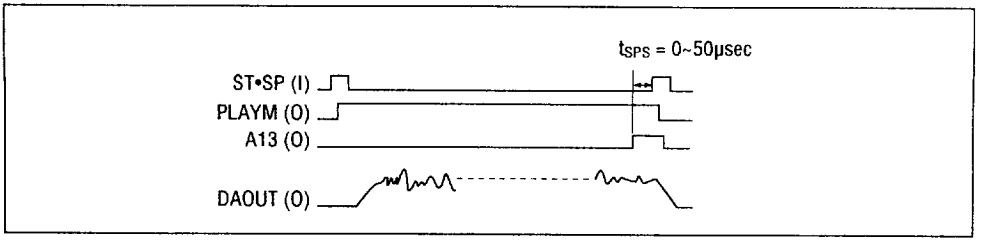


Figure 20 Stop Timing for Reproduction from ROM

Setting of other terminals
(D/$\overline{SRAM}$ = "L", CA1, 2, 3 = "L",
REC/$\overline{PLAY}$ = "L", RAMS1 = "L",
RAMS2 = "H")

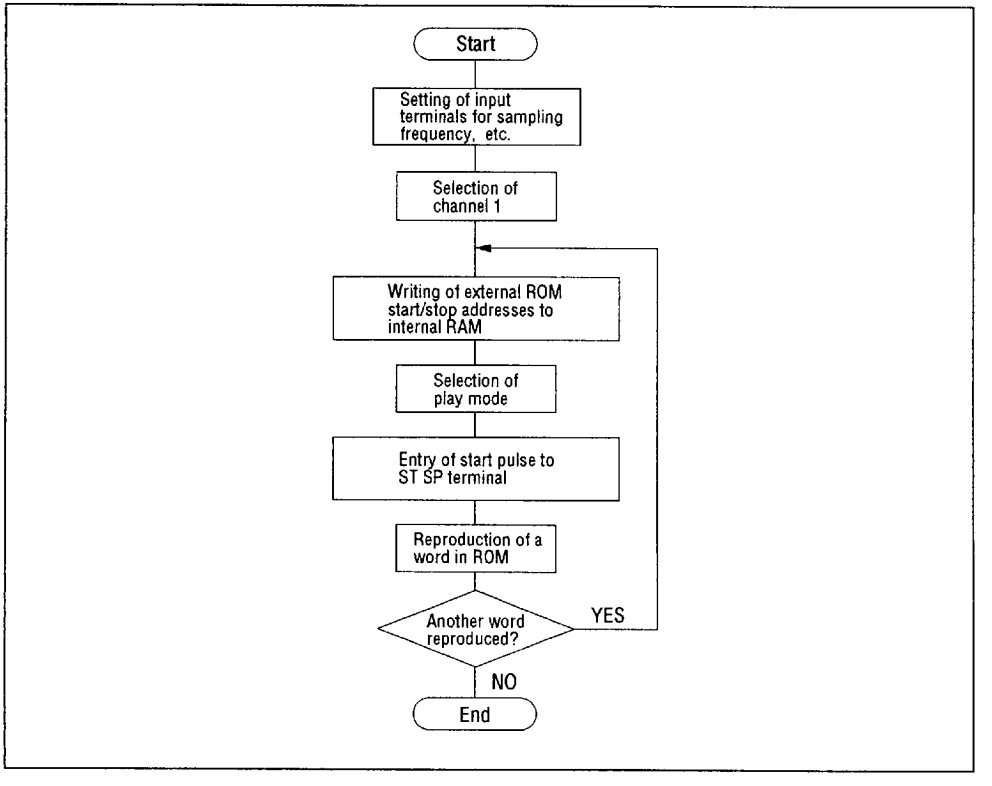


Figure 21 Flow Chart for Reproduction from ROM

14. Use

14.1 Recording of 7 or More Words

As stated earlier, seven words can be recorded in channel 1 through 7. If the internal RAM in MSM6258 is controlled using a microcomputer, more than seven words can be recorded. Operating procedure is similar to that described in 13.2, "Reproduction of Part of Contents of External ROM". Select channel 1, write start/stop addresses to the internal RAM, and record data to that address.

14.2 Use of both RAM and ROM

RAM and ROM may be connected to MSM6258 to record a variable message in RAM and a fixed message in ROM.

Examples of circuits are given in Figures 28 and 29.

15. Backup with Battery

When backing up SRAM storing ADPCM data with a battery, be sure to also back up MSM6258. MSM6258 has RAM to store start/stop addresses for each channel. Even if SRAM is backed up, its contents cannot be reproduced unless MSM6258 itself is backed up.

- **Operation with CPU Interface**

As stated earlier, CPU interface does not control external RAM addresses. Therefore, an external control circuit for RAM must be designed.

1. Connection of Data Bus

Insert a pull-up or pull-down resistor to the data bus bits D0~D7.

Table 5 Use of $\overline{CS}$, D/C, $\overline{RD}$, and $\overline{WR}$

CS	D/C	RD	WR	Operation
L	H	L	H	Output of ADPCM data (during recording)
L	H	H	L	Input of ADPCM data (during playing)
L	L	L	H	Output of status
L	L	H	L	Entry of command
H	x	x	x	Use of data bus is inhibited. (high impedance)

2. Use of Data Bus

The data bus can be controlled using the four pins of the D/C terminal by making a selection as to whether the CS, RD, and WR terminals, and data bus should be used for input/output of ADPCM data or for input/output of command/status.

Table 5 is a list of "H" and "L" combinations of these terminals. As shown in Table 2, ADPCM data for two samples are input and output at a time.

3. Entry of Commands

These are commands for start of recording, start of reproduction, stop of recording/reproduction, and setting of initial pointers.

Entering "H" level makes each of these commands valid.

However, "L" level should be entered for initial pointers P0 through P4. If "H" level is entered, the amplitude of the waveform for reproduction will be changed.

Table 6 shows the relationships between the data bus and command.

Table 6 Data Bus and Command

D0	D1	D2	D3	D4	D5	D6	D7
SP ST	PLAY ST	REC	P4	P3	P2	P1	P0

SP ..... Stop recording and playing
PLAY ST ..... Start playing
REC ST ..... Start recording
P0 ~ P4 ..... Setting of initial pointers (Always enter "L".)

4. Status Output

The status output tells which is currently performed, recording or playing.

The status output in standby mode is as follows:

D0 ~ D6: "L"level
D7: "H"level

Table 7 shows the relationships between the data bus and status.

Table 7 Relationships between Data Bus and Status

D0	D1	D2	D3	D4	D5	D6	D7
X	X	X	X	X	X	X	REC/PLAY

REC/PLAY ..... "H" during recording
"L" during playing

5. Read/Write Timing

Read/write timing of ADPCM DATA is synchronized to MCK.

6. Recording/Playback Method

To start recording, a recording start command is entered using the D/C, WR, and D0 ~ D7 terminals.

During recording, ADPCM data is written to the external RAM in synchronization with the MCK output.

To terminate recording, enter a stop command.

Playing is performed if a play start command is entered, and ADPCM data is read from the external RAM in synchronization with MCK.

Timing for recording and playing is shown in Figure 22. If recording or playing is stopped using a stop command, DAOUT retains the level at which recording or playing has been terminated, and its level is changed to 1/2VDD as soon as a start command is entered.

7. Voice-Triggered Starting

With the CPU interface, voice-triggered starting cannot be performed using the logic circuit in MSM6258. To perform voice-triggered starting, use an external analog circuit. An example of such a circuit is given in Figure 35.

8. Troubleshooting Check List

If normal playing is impossible even when the hardware and software for CPU interface are used, perform check up according to the following procedure:

(1) Check DAOUT output during recording:

The waveform of the output from the DAOUT terminal during recording is just the same as that during playing. Make sure that the waveform of the output from the DAOUT is normal.

(2) Recording and playing of muted voice:

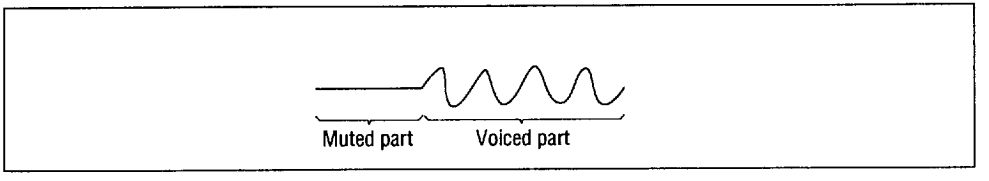
If the waveform of the output during recording is normal, use a muted voice waveform, or DC level waveform.

If the waveform of the output from DAOUT during playing rises or falls, ADPCM data read/write timing is wrong. Check read/write timing.

(3) Recording and playing of muted voice waveform and voice waveform:

To check read/write timing, perform recording and playing using a waveform consisting of muted voice and voice.

If the waveform of the output from DAOUT rises or falls during playing, or if its amplitude changes, check read/write timing again.



(4) Recording and playing of voice waveform:

For final checkup, perform recording and playing using a voice waveform.

If the amplitude of the waveform of the output from DAOUT during playing changes, the trouble may lie in the interface with the external RAM. More concretely, it is likely that ADPCM data for several samples are not stored in the external RAM before start of recording, or ADPCM data for several samples are not transferred from the external RAM to LSI before start of playing. To see whether the timing after start of playing is normal, enter the ADPCM data given below to the LSI, and check that a 1.5Vp-p sine wave is output from DAOUT.

If the waveform is 1.5Vp-p sine wave, the interface for playing is judged to be normal. Check the timing for start of recording again.

How to generate 1.5Vpp sine wave:

Enter the following ADPCM data:

0,3,3,7,F,7,F,4,C,4,C,4,0,9,C,8,1 repetitions of 4,0,9,C,8,1

This data will work with a M5205 but must be nibble swapped for the 6258.

<Example>

D7 ~ D0
(3 0)$_{HEX}$ Please refer to ADPCM data of P.29.
(7 3)$_{HEX}$
(7 F)$_{HEX}$
(4 F)$_{HEX}$

Waveform of output from DAOUT

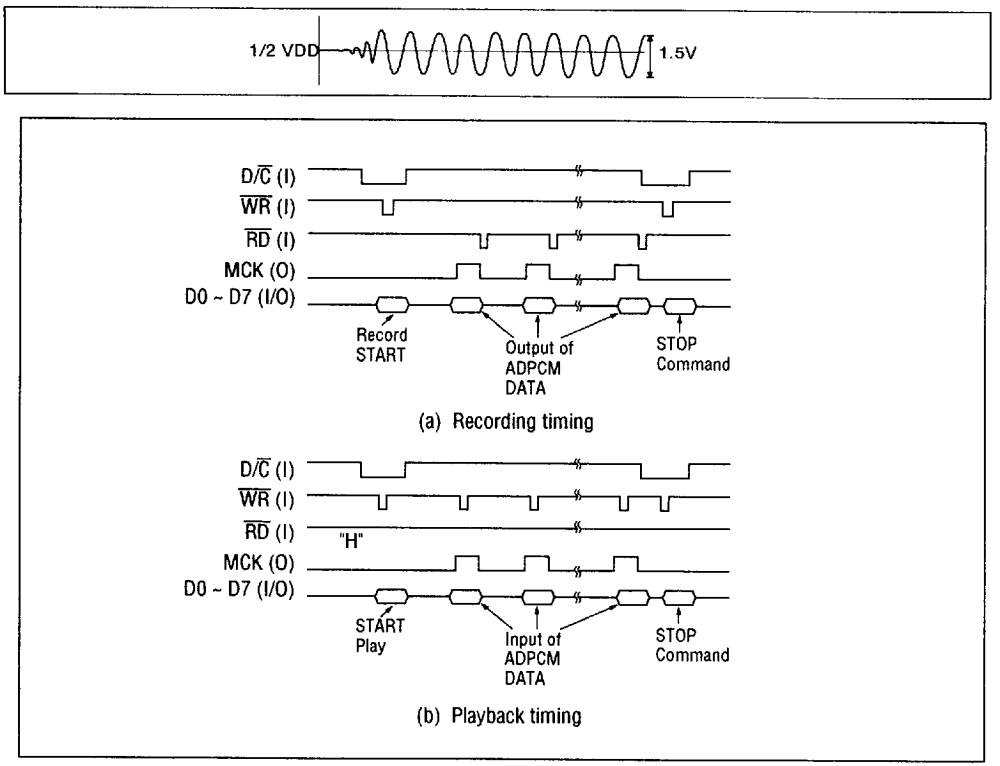


Figure 22

CIRCUIT EXAMPLES

- Figure 23 shows an example of interface with 64K SRAM.
- Figure 24 shows an example of interface with 256K SRAM.
- Figure 25 shows an example of interface with 256K SRAM.
- Figure 26 shows an example of interface with 256K DRAM.
- Figure 27 shows an example of interface with 1M DRAM.
- Figure 28 shows an example of interface with 256K EPROM.
- Figure 29 shows an example of interface with 512K EPROM.
- Figure 30 shows an example of interface with MSM5840A when MSM6258, masked ROM, and SRAM used for fixed and variable messages.
- Figure 31 shows an example of a circuit when MSM6258, masked ROM, and DRAM, and SRAM are used for fixed and variable messages.
- Figure 32 shows an example of interface with MSM80C85 when MSM6258, is used in CPU interface.
- Figure 33 shows an example of a mute circuit used for recording with MSM6258.
- Figure 34 shows an example of a voice-triggered starting circuit for the CPU interface with MSM6258.

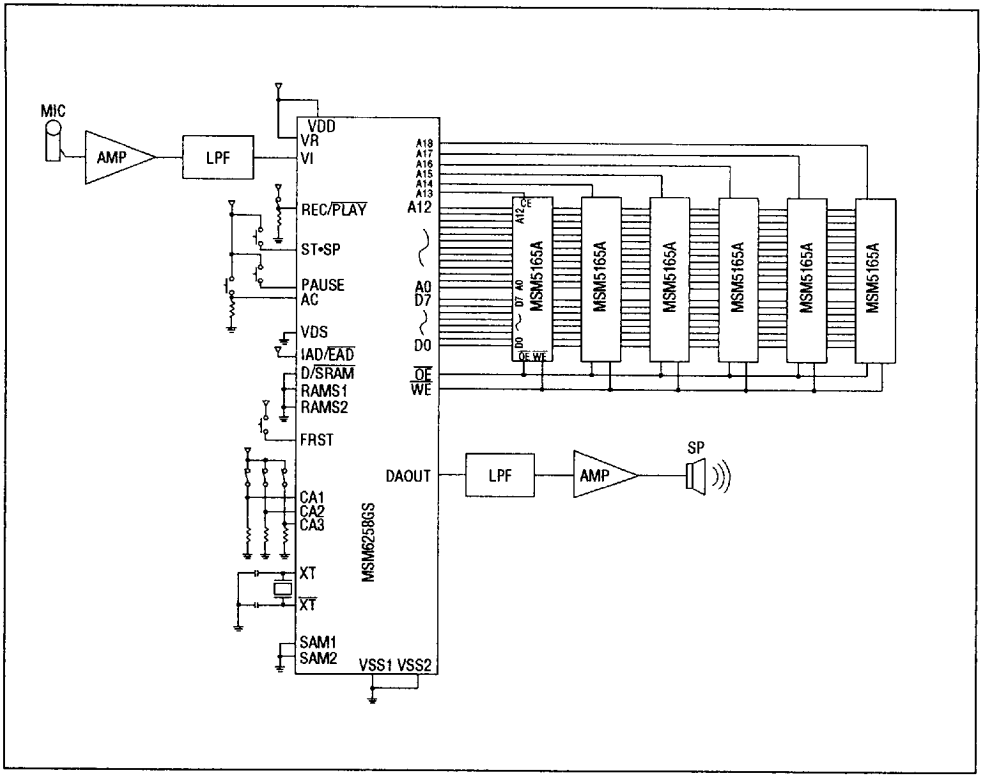


Figure 23 Application Note for 64K SRAM

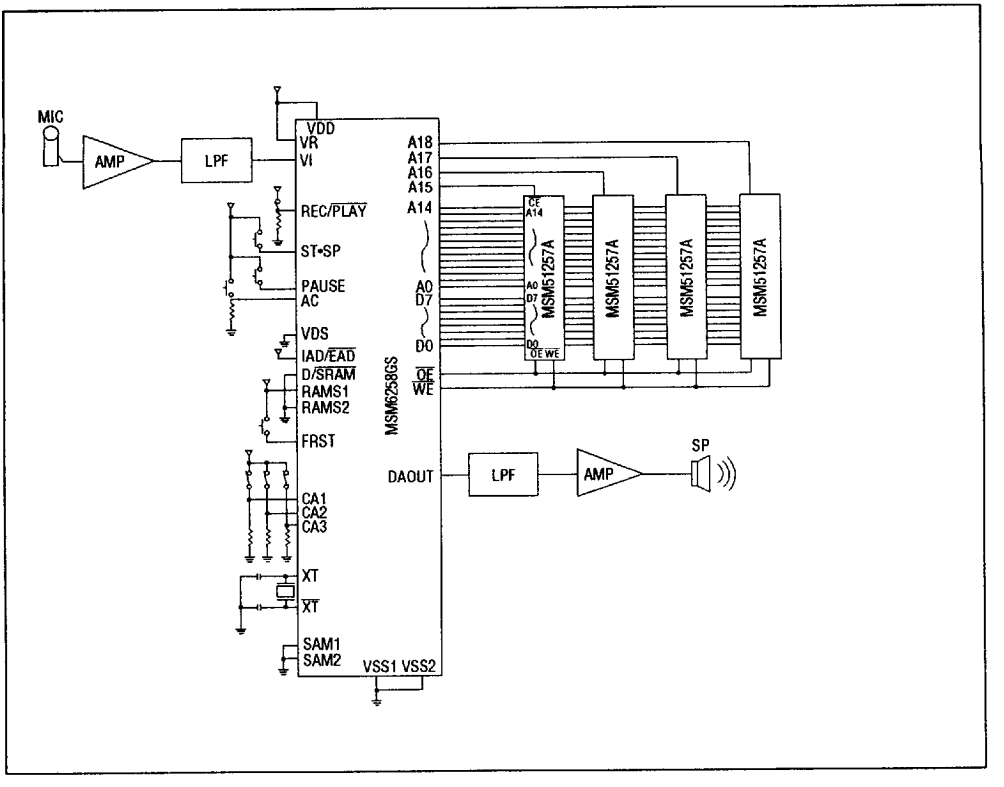


Figure 24 Application Note for 256K SRAM

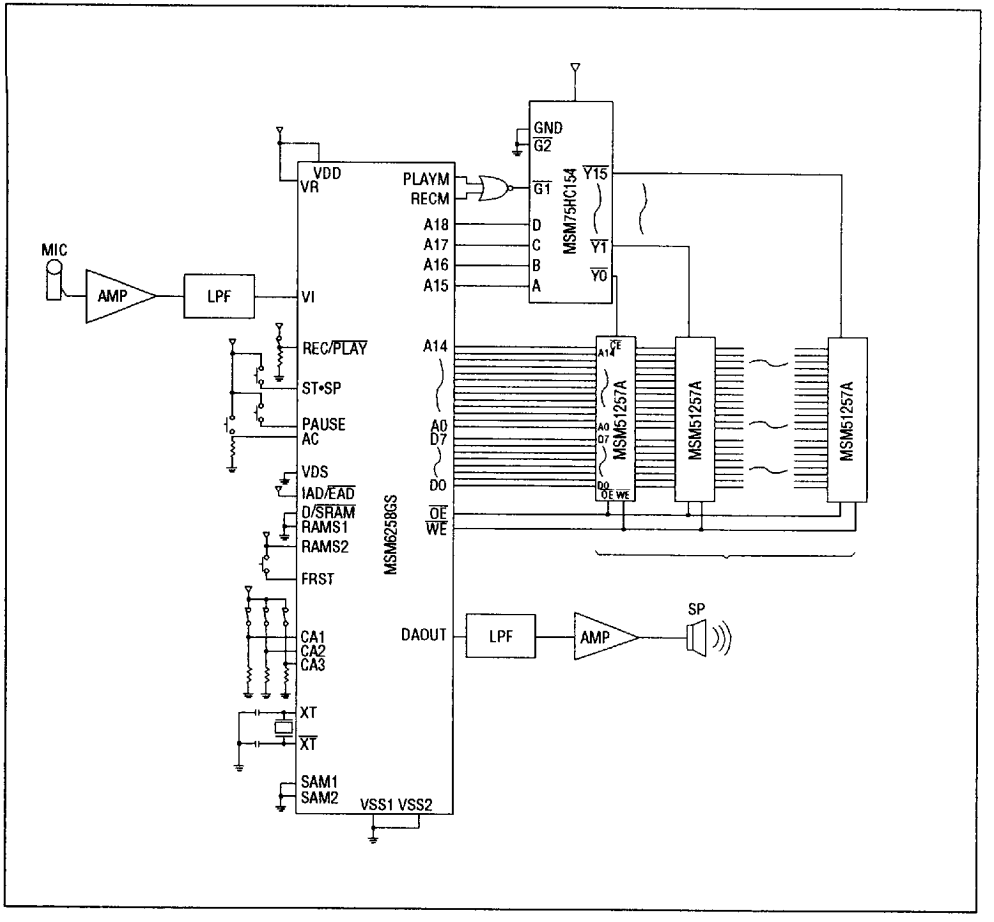


Figure 25 Application Note for 256K SRAM (Use 16 pcs)

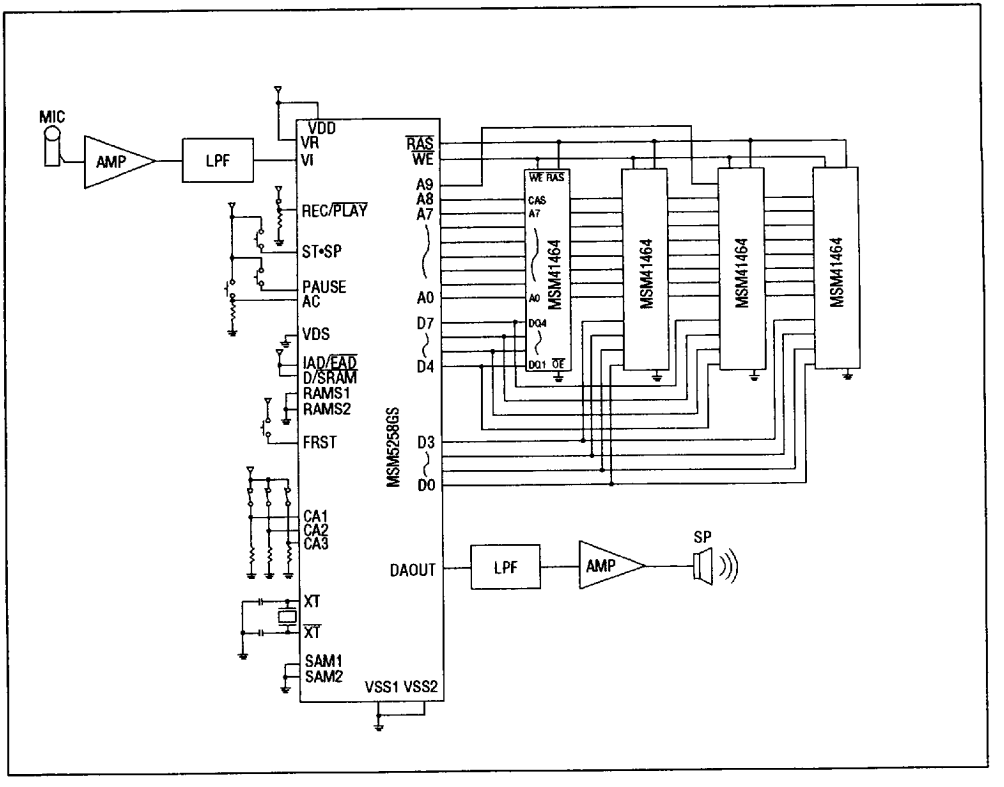


Figure 26 Application Note for 256K DRAM

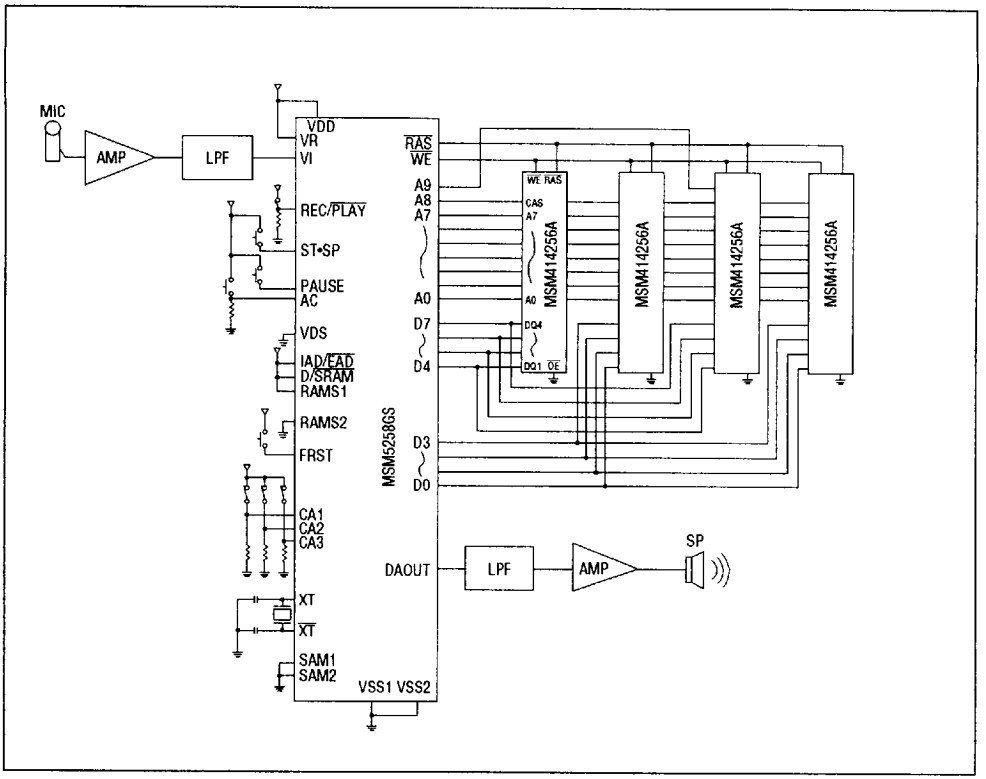


Figure 27 Application Note for 1M-bit DRAM

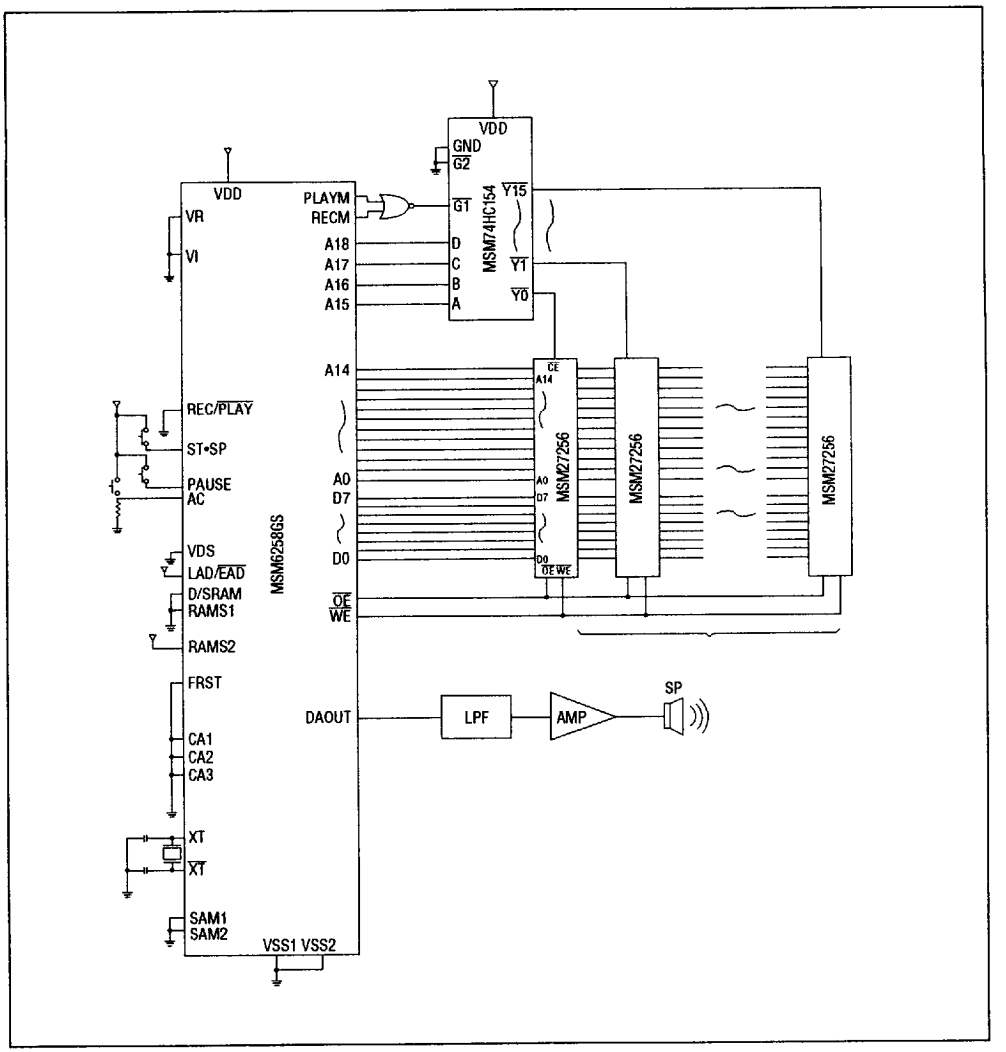


Figure 28 Application Note for 256K EPROM (Use 16 pcs)

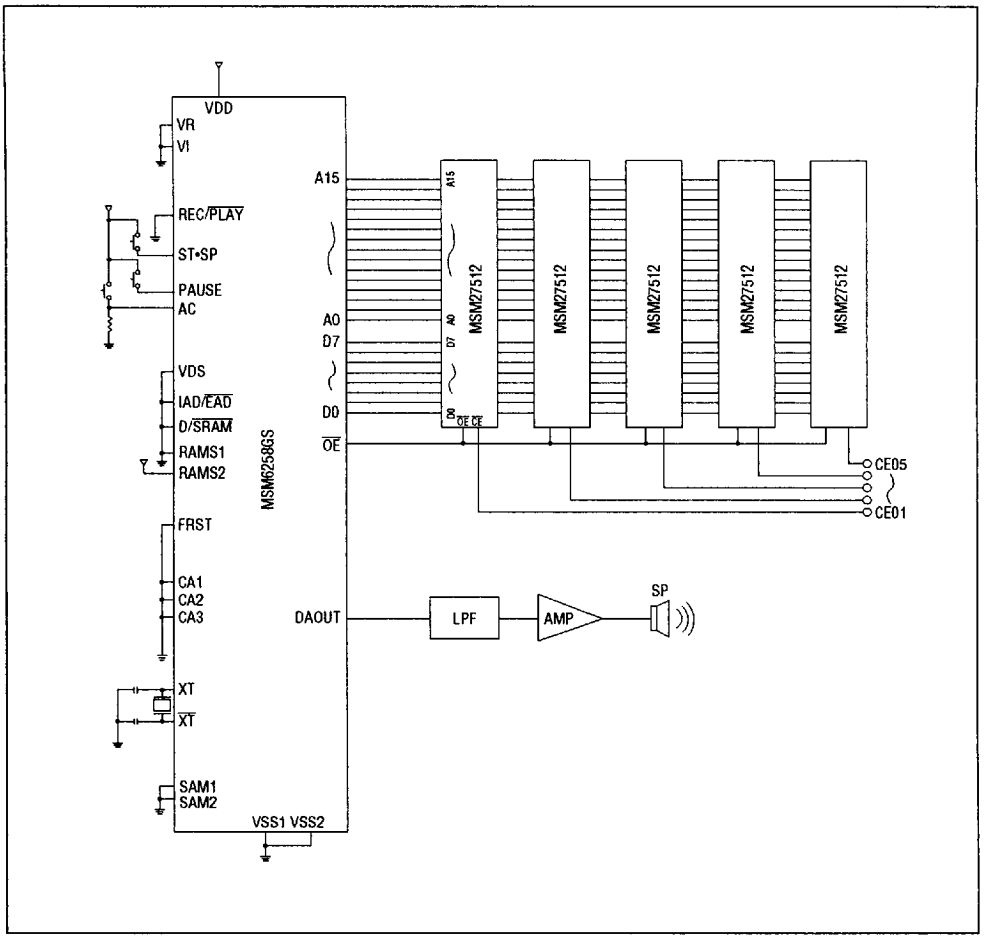


Figure 29 Application Note for 512K EPROM (Address is binary output)

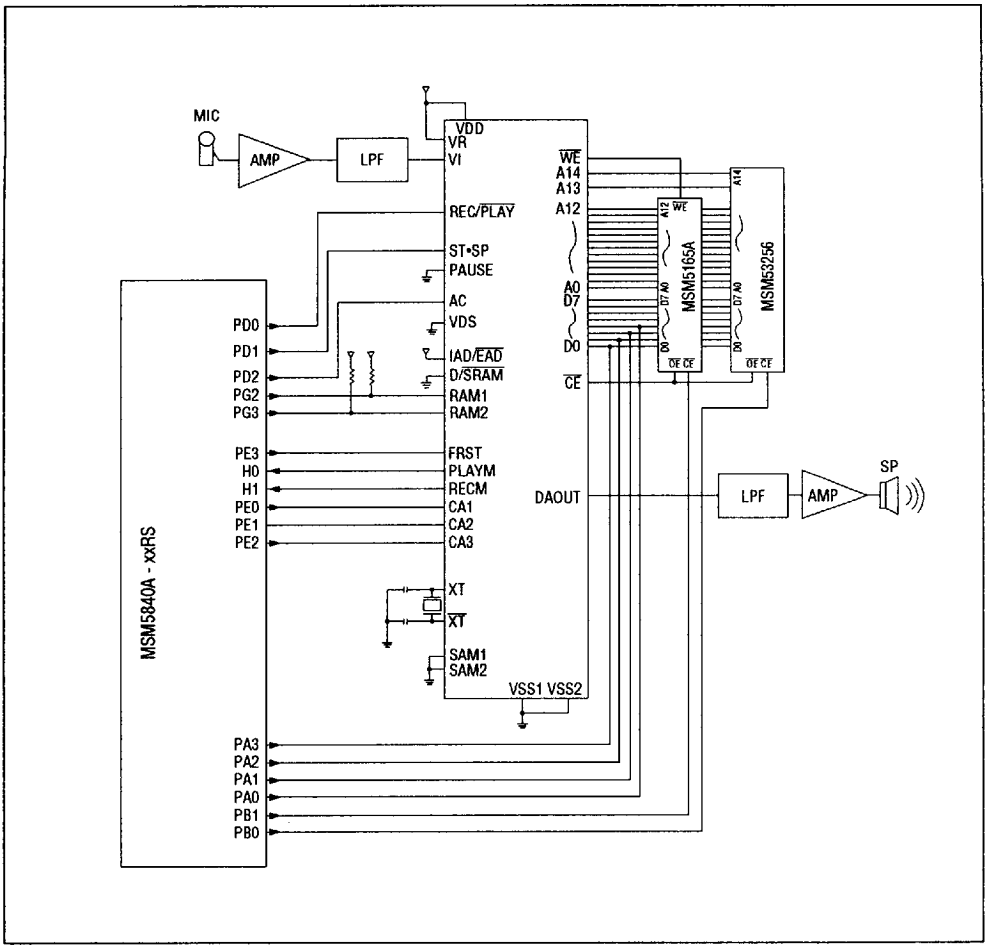
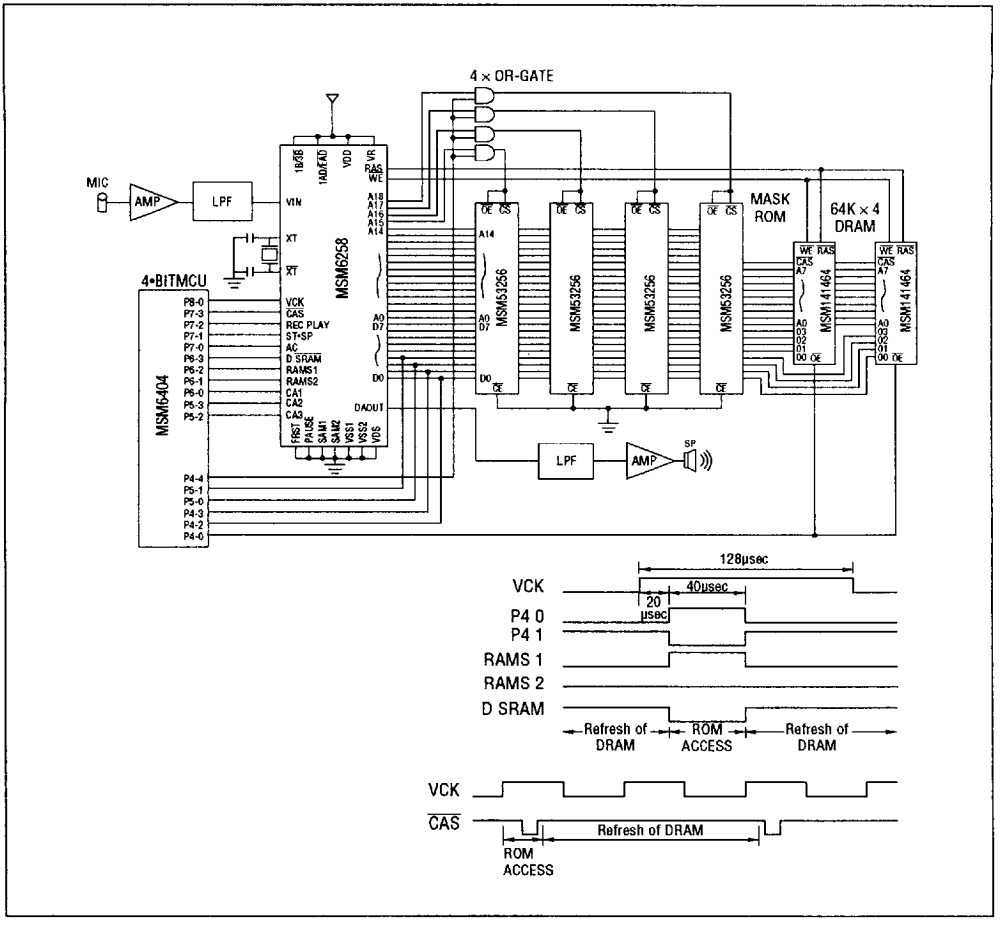


Figure 30 Example of Interface with 64K SRAM & 256K Mask ROM



In case both DRAM and masked ROM are used, it is necessary to refresh DRAM except when data is being read from the masked ROM.
The figure on the right shows the timing when fs is 3.9kHz. Read data from ROM during the ROM access time shown in the figure.

Figure 31 Example of Interface for 256K DRAM and Masked ROM

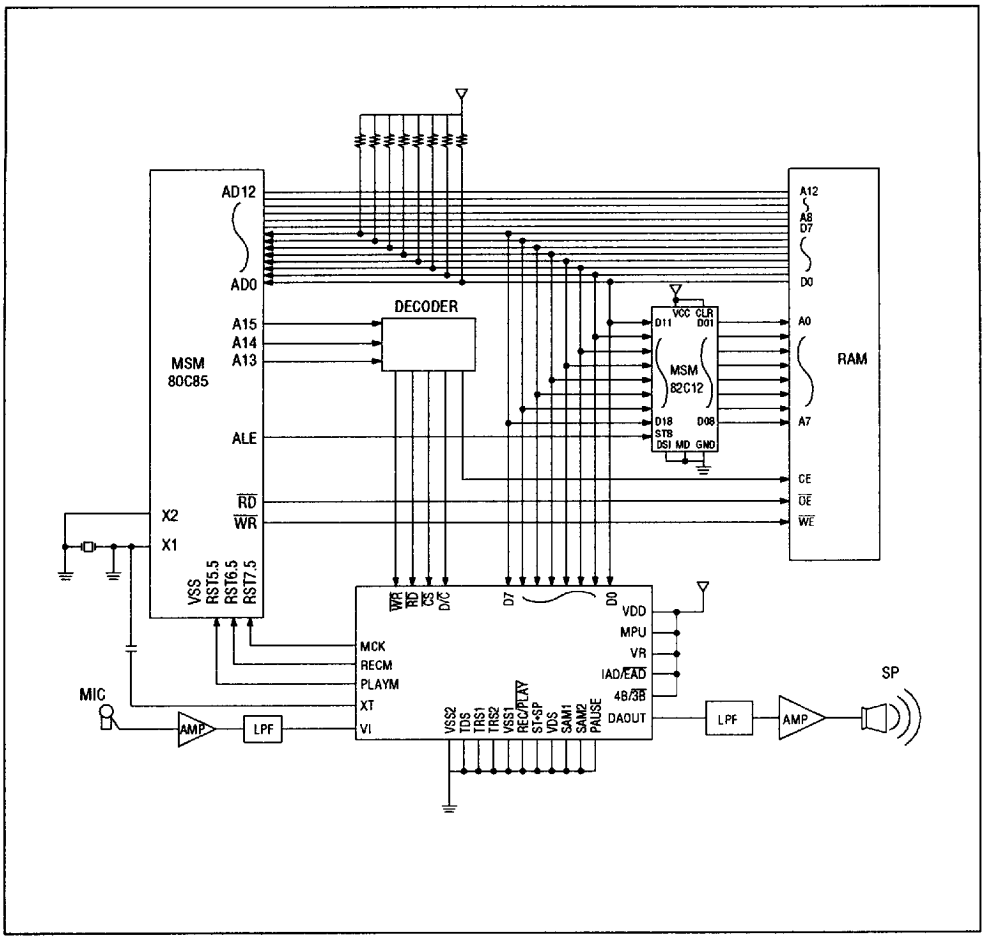


Figure 32 Example of Interface with MSM80C85

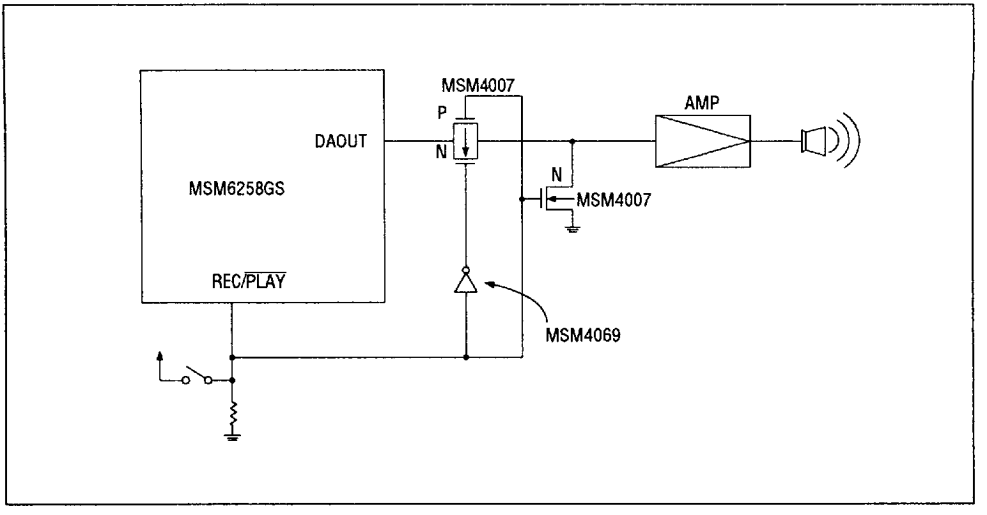


Figure 33 Example of Mute Circuit for Recording

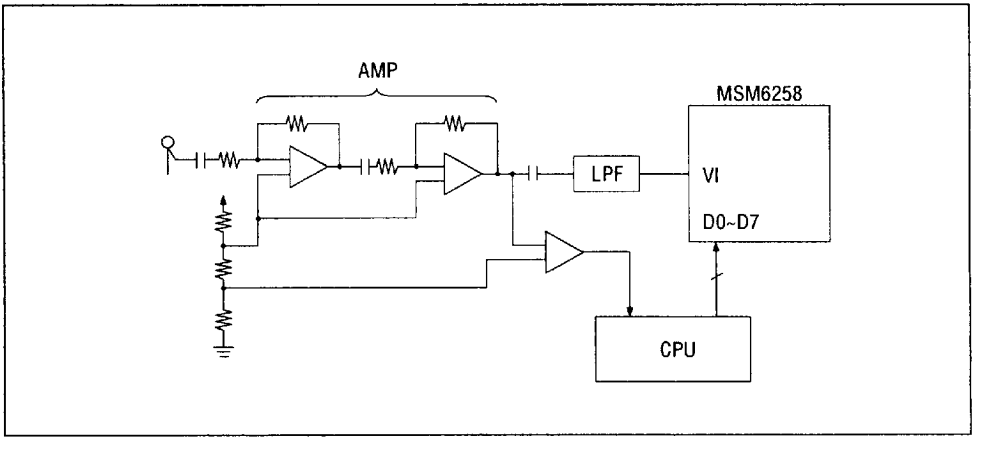


Figure 34 Voice-Triggered Starting Circuit for CPU Interface