

APPLICATION NOTE

Bi-directional level shifter for I²C-bus and other systems.

AN97055

Abstract

With a single MOS-FET a bi-directional level shifter circuit can be realised to connect devices with different supply voltages of e.g. 5 Volt and 3.3 Volt to one I²C-bus system. The level shifter can also isolate a bus section of powered-down devices from the I²C-bus, allowing the powered part of the I²C-bus to operate in a normal way.

The level shifter can also be used in other bus systems or point to point connections for level shifting and/or isolation.



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APPLICATION NOTE

Bi-directional level shifter for I²C-bus and other systems.

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Summary

Present technologies for integrated circuit with clearances of 0.5 μm and less, limit the maximum supply voltage and consequently the logic levels for the digital I/O signals. To interface these lower voltage circuits with existing 5 Volt devices a level shifter is needed. For bi-directional bus systems as e.g. the I²C-bus, such a level shifter must be bi-directional, without the need of a direction control signal. With only one appropriate MOS-FET for each bus line the desired level shifting with automatic direction control can be done. The levels may have a vast range, depending on the used MOS-FET, e.g. down to 2 Volt at the "Lower voltage" side and up to 10 Volt or more at the "Higher voltage" side of the level shifter.

An additional function of the level shifter is that it can isolate a powered-down section in a bus system, without obstructing the powered part. Another feature is the protection of the "Lower voltage" section against high voltage spikes at the "Higher voltage" section, as long as the MOS-FET can withstand this spikes.

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1. INTRODUCTION

The I²C-bus has been introduced in 1980 by Philips, and has become a de-facto world standard. More than 1000 different IC devices have been provided with an I²C-bus interface, most of them having a 5 Volt supply voltage and corresponding logic I/O levels. These 5 Volt devices can be interconnected to an I²C-bus system without any glue logic.

Present technology processes for integrated circuits with clearances of 0.5 μm and less, limit the maximum supply voltage to 3.3 Volt and in the near future to 2 Volt and less. Also the I/O signals have this limitation, so there is a problem to interconnect them with existing 5 Volt devices. The same problem will exist in the future to interconnect e.g. 3.3 Volt devices and 2 Volt devices.

One solution for this problem is the use of 5 Volt tolerant I/O's. Most present IC technology processes have a high voltage option to make I/O signals 5V tolerant. This gives the possibility to connect lower voltage devices to 5 Volt devices or to 5 Volt bus systems. The disadvantage of this 5 Volt option is that it requires more masks and process steps in the IC manufacturing, which makes the IC devices significantly more expensive.

Another solution is the use of external level shifters. In the different logic families level shifters are available, most of them for one direction, which cannot be used in a bi-directional bus system. The bi-directional level shifters in these families require a direction control signal, which is not available in a serial bus system, so these level shifters are not applicable.

The bi-directional level shifter circuit described in this application note consists of one discrete MOS-FET for each bus line. In spite of its surprising simplicity, it not only fulfils the requirement of bi-directional level shifting without a direction control signal, but it also has the next additional features:

- isolating of a powered-down bus section from the rest of the bus system,
- protection of the "Lower voltage" side against high voltage spikes at the 'Higher voltage' side.

The bi-directional level shifter can be used in standard mode (0 to 100 kbit/s) or in fast mode (0 to 400 kbit/s) I²C-bus systems, without any change. The following description apply for both modes.

1.1 References.

Useful references for I²C-bus related documentation:

ordering inf.

- | | |
|---|----------------|
| • The I ² C-bus and how to use it. (including specification) | 9398 393 40011 |
| • I ² C Peripherals, DATA HANDBOOK IC12 (includes I ² C-bus spec.) | 9397 750 00306 |
| • Application Notes and Development Tools for 80C51 Microcontrollers (includes I ² C-bus application notes, articles and I ² C-bus spec.) | 9397 750 00963 |

1.2 World Wide Web.

Internet access for Philips Semiconductors:

<http://www.semiconductors.philips.com>

2. INTERCONNECTION OF DEVICES WITH DIFFERENT LOGIC LEVELS.**2.1 Logic levels of the I²C-bus.**

An overview of the different logic levels, used in I²C-bus systems, is given below.

The I²C-bus specifies two types of logic levels:

- a) fixed levels,
- b) supply voltage related levels.

a) The fixed levels are intended for non-CMOS devices and/or devices with higher supply voltages than 5 Volt, e.g. 12 Volt. The I/O levels for fixed level devices are:

LOW level input voltage V_{IL}	min. -0.5V	max. 1.5V
HIGH level input voltage V_{IH}	min. 3.0V	max. $V_{DDmax}+0.5V$
LOW level output voltage V_{OL1}	min. 0V	max. 0.4V
HIGH level output voltage V_{OH}	open drain output, determined by V_{DD} via an external pull-up resistor.	

b) The supply voltage related levels are intended for CMOS devices and/or devices with supply voltages of 5V or lower. Their I/O levels are:

LOW level input voltage V_{IL}	min. -0.5V	max. $0.3V_{DD}$
HIGH level input voltage V_{IH}	min. $0.7V_{DD}$	max. $V_{DDmax}+0.5V$
LOW level output voltage V_{OL1}	min. 0V	max. 0.4V
HIGH level output voltage V_{OH}	open drain output, determined by V_{DD} via an external pull-up resistor.	

The logic levels of the bus lines depends on the pull-up resistors to V_{DD} , leakage current and, if present, series resistors to the I/O pins of the devices. Their values must be chosen in such a way that during the LOW level a minimum noise margin of $0.1 V_{DD}$ is present and $0.2 V_{DD}$ during the HIGH level.

2.2 I²C-bus devices with different supply voltages and 5V tolerant I/O's.

From the listed values in 2.1 can be concluded that fixed level devices and 5V supply voltage related devices can be connected directly to the same bus lines, without additional components. Also 3.3V supply voltage related devices can be connected directly to these bus lines as long as they have 5V tolerant I/O pins, because the pull-up resistors have to be connected to the 5V supply voltage (see Figure 1).

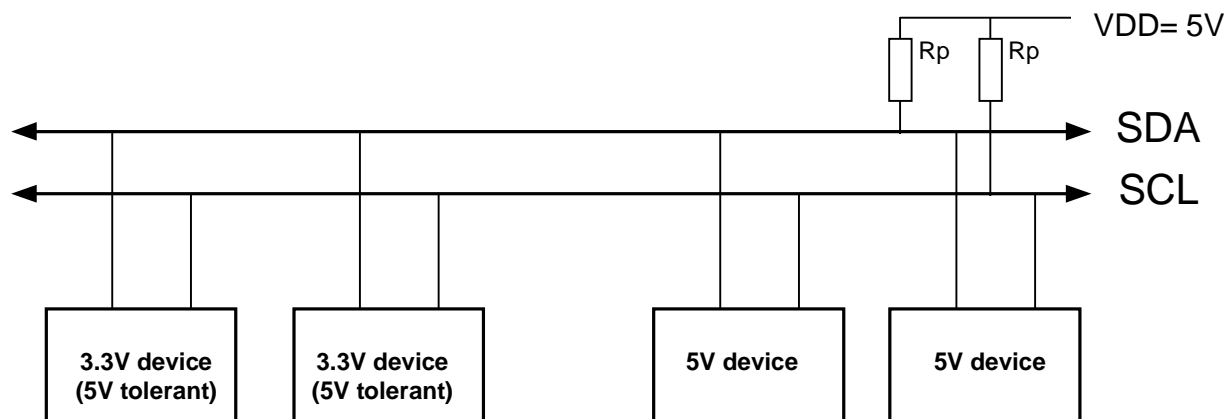


Figure 1. I²C-bus system with 3.3V devices (5V tolerant) and 5V devices, all connected to the same bus lines.

This is the most simple solution, but the lower voltage devices must be 5 Volt tolerant, which may make them more expensive to manufacture. Lower voltage devices with a supply voltage as low as 2 Volt still meet the I²C-bus specification and can be connected to the bus system of Figure 1.

If devices with a supply voltage lower than 2.7 Volt are connected via series resistors to the bus lines, then attention must be paid to meet the $0.1 V_{DD}$ noise margin during the LOW level, required by the I²C-bus specification. The required $0.2 V_{DD}$ noise margin during the HIGH level does not depend on the supply voltage.

Devices with a supply voltage lower than 2 Volt do not meet the noise margin requirement of $0.1 V_{DD}$ because the LOW level on the bus lines is 0.4V and their input level of $0.3 V_{DD}$ is less than 0.6V. This will be solved in the next update of the I²C-bus specification.

2.3 Devices with different logic levels connected via the bi-directional level shifter.

The bi-directional level shifter is used to interconnect two sections of an I²C-bus system, each section with a different supply voltage and different logic levels. In the bus system of Figure 2 the left section has pull-up resistors and devices connected to a 3.3 Volt supply voltage, the right section has pull-up resistors and devices connected to a 5 Volt supply voltage. The devices of each section have I/O's with supply voltage related logic input levels and an open drain output configuration.

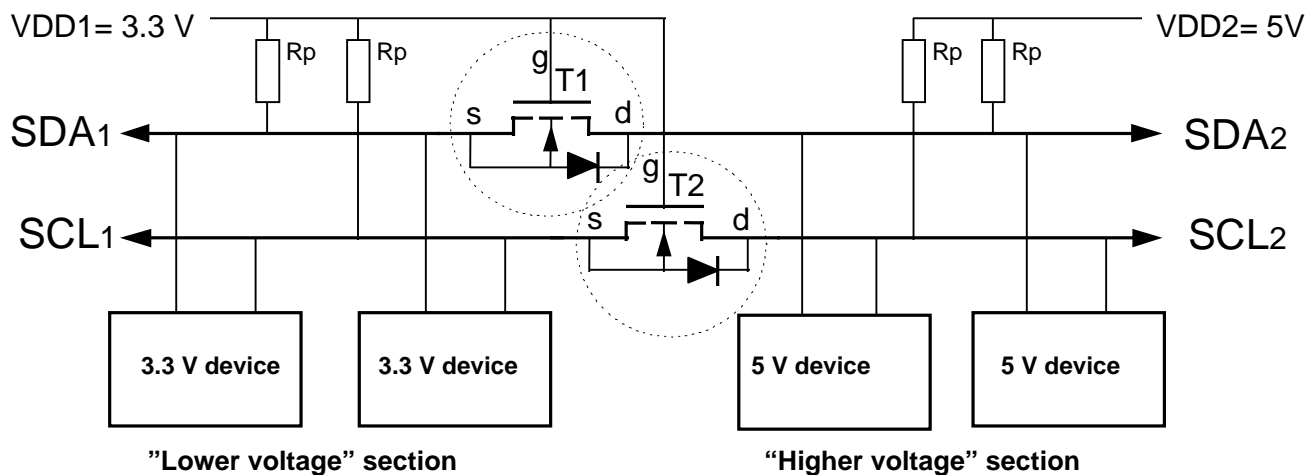


Figure 2. Bi-directional level shifter circuit connects two different voltage sections of an I²C-bus system.

The level shifter for each bus line is identical and consists of one discrete N-channel enhancement MOS-FET, T1 for the serial data line SDA and T2 for the serial clock line SCL. The gates (g) has to be connected to the lowest supply voltage VDD1, the sources (s) to the bus lines of the "Lower voltage" section, and the drains (d) to the bus lines of the "Higher voltage" section. Many MOS-FET's have the substrate internally already connected with its source, otherwise it should be done externally. The diode between the drain (d) and substrate is inside the MOS-FET present as n-p junction of drain and substrate.

2.3.1 Description of the level shift operation.

For the level shift operation three states has to be considered:

- State 1. No device is pulling down the bus line and the bus line of the "Lower voltage" section is pulled up by its pull-up resistors Rp to 3.3 V. The gate and the source of the MOS-FET are both at 3.3 V, so its V_{GS} is below the threshold voltage and the MOS-FET is not conducting. This allows that the bus line at the "Higher voltage" section is pulled up by its pull-up resistor Rp to 5V. So the bus lines of both sections are HIGH, but at a different voltage level.
- State 2. A 3.3 V device pulls down the bus line to a LOW level. The source of the MOS-FET becomes also LOW, while the gate stay at 3.3 V. The V_{GS} rises above the threshold and the MOS-FET becomes conducting. Now the bus line of the "Higher voltage" section is also pulled down to a LOW level by the 3.3 V device via the conducting MOS-FET. So the bus lines of both sections become LOW at the same voltage level.

- State 3. A 5 V device pulls down the bus line to a LOW level. Via the drain-substrate diode of the MOS-FET the “Lower voltage” section is in first instance pulled down until V_{GS} passes the threshold and the MOS-FET becomes conducting. Now the bus line of the “Lower voltage” section is further pulled down to a LOW level by the 5 V device via the conducting MOS-FET. So the bus lines of both sections become LOW at the same voltage level.

The three states show that the logic levels are transferred in both directions of the bus system, independent of the driving section. State 2 and state 3 perform the “wired AND” function between the bus lines of both sections as required by the I²C-bus specification.

Other supply voltages than 3.3V for VDD1 and 5V for VDD2 can be applied, e.g. 2V for VDD1 and 10V for VDD2 is feasible. In normal operation VDD2 must be equal to or higher than VDD1.

The MOS-FET's allow that VDD2 is lower than VDD1 during switching power on/off, of course the bus system is not operational during that time.

The maximum VDD2 is not critical as long as the drain of the MOS-FET can withstand this voltage. At a higher VDD2 a slower falling edge for both bus sections has to be taken in account, both in state 2 and state 3, because it takes more discharge time of the bus line.

The lowest possible supply voltage VDD1 depends on the threshold voltage $V_{GS(th)}$ of the MOS-FET's. With a threshold voltage of about 1 Volt below the lowest VDD1, the level shifter circuit will operate properly. If for example the lowest VDD1 is 3 Volt, a threshold voltage $V_{GS(th)}$ of maximum 2 Volt is allowed.

2.3.2 Protection of the “Lower voltage” section against high voltage spikes.

If an I²C-bus system has to be connected with e.g. external bus lines on which high voltage spikes can be expected, the level shifter circuit may be used as protection circuit as long as the drain of the MOS-FET can withstand these high voltage spikes. The “Lower voltage” section is the protected side, the “Higher voltage” section the is the side of the external bus lines (see Figure 2). If in this application no level shifting is required, VDD1 and VDD2 can be interconnected.

2.3.3 The level shifter used in point to point connections.

The circuit of figure 2 can also be used as a one-directional level shifter between an output signal and one or more inputs, which have higher or lower logic levels than that output signal.

If the output signal is generated by a push-pull stage, then the Rp at the output circuit side, (“Lower voltage” or “Higher voltage” section) can be omitted. The Rp at the input circuit(s) side remains needed.

The protection and isolation features, described in 2.3.2 and 2.3.4 also apply here.

2.3.4 Isolation of the powered-down “Lower voltage” section.

An additional feature of the level shifter circuit in figure 2 is the isolation of the “Lower voltage” section when VDD1 is switched off. In that case VDD1 is about 0 Volt and the MOS-FET's are switched off because V_{GS} is below the threshold voltage. The “Higher voltage” section is not hindered and stays operational. To assure a noise margin, the MOS-FET's should have a minimum threshold voltage $V_{GS(th)}$ of e.g. 0.4V and VDD1 must stay below this value. The isolation feature can also be applied if no level shifting is required, VDD1 and VDD2 may have the same value, e.g. both 3.3V or both 5V.

2.3.5 Extended circuit for isolation of the powered-down “higher voltage” section.

If it is necessary to isolate also the “Higher voltage” section when it is powered off, then the level shifter circuit can be extended as shown in figure 3.

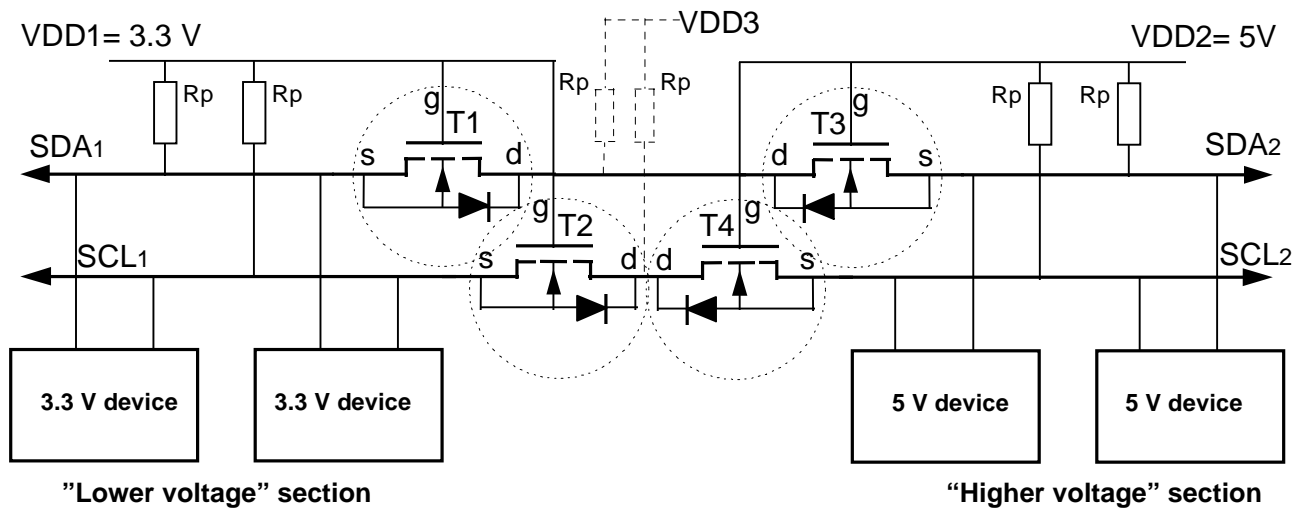


Figure 3. I²C-bus system in which the “Higher voltage” section is isolated at power-off.

If VDD2 is switched-off then T3 and T4 becomes not conducting and the “Higher voltage” section is isolated from the other part of the bus system. The pull-up resistors Rp to VDD3 are not necessary for the proper operation and may have a high resistance value, they can be added to prevent the MOS-FET drains become floating at a HIGH level. VDD3 is preferably connected to the highest supply voltage. If VDD3 has a lower value, then care must be taken that the logic HIGH levels of the bus lines are not decreased too much.

The “Lower voltage” section is isolated if VDD1 is switched off, in the same way as in Figure 2 and described in 2.3.4, but now independent of the value of VDD2.

Because this level shifter circuit is symmetrical, the “Lower voltage” section and “Higher voltage” section can be chosen arbitrary at the left or right side in figure 3. Even more sections with a higher, a lower or a same supply voltage value can be added by connecting these sections via additional MOS-FET's to the common drain terminals (d) in the same way as the other sections in Figure 3. Every section is isolated from the rest of the bus system when its supply voltage is switched off, while level shifting between all other sections remain operational.

3. CHARACTERISTICS OF THE MOS-FET'S.

The requirements for the most important characteristics of the MOS-FET's, used as bi-directional level shifter in an I²C-bus system with max. 6V and min. 2.7V levels, are listed below. The values are intended as an indication and may be adapted for other supply voltages, other logic levels and/or other applications.

Type :	N-channel enhancement mode MOS-FET.		
Gate threshold voltage :	$V_{GS(th)}$	min. 0.1V	max. 2V
On resistance :	$R_{DS(on)}$	max. 100 Ohm @ $I_D = 3mA$, $V_{GS} = 2.5V$	
Input capacitance :	C_{iss}	max. 100 pF @ $V_{DS} = 1V$, $V_{GS} = 0V$	
Switching times :	t_{on} t_{off}	max. 50 ns.	
Allowed drain current :	I_D	10 mA or higher.	

Values of pull-up resistors and series resistors are not given here, they depend on the worst case values of the supply voltages and logic levels, length and load of the bus lines, and the requirements for rise and fall times. These resistors have to be calculated for each bus system separately. A good approach for the calculation is to keep the RC values for the different sections about the same, it gives the best timing tolerances for set-up and hold times.

MOS-FET's in table 1 are suitable to be used as level shifter. See Philips Data Handbook SC07 for their full specification. BSN10 or BSN20 are low cost devices and have good properties for 3V/5V level shifting, isolation and protection.

TABLE 1

TYPE	$V_{GS(th)}$	$R_{DS(on)}$	C_{iss}	Package
BSN10	min. 0.4V max. 1.8V	25 Ohm (typ)	15 pF	TO-92
BSN20	min. 0.4V max. 1.8V	25 Ohm (typ)	15 pF	SOT23
BSS83	min. 0.1V max. 2.0V	70 Ohm (typ)	1.5 pF (typ)	SOT143
BSS88	min. 0.4V max. 1.2V	15 Ohm	50 pF (typ)	TO-92

4. WAVE FORMS OF THE LOGIC LEVELS.

Figures 4, 5, 6, 7 and 8 show the wave forms of the logic levels of an implementation according Figure 2. Figure 9 shows the wave forms of the implementation according figure 3. T1, T2, T3 and T4 are MOS-FET's type BSN10. The "Lower voltage" section has an Rp of 3k3 Ω and a bus line capacitance of 50 pF. The "Higher voltage" section 4K7 Ω and 30 pF. Only the wave forms of the SCL lines are shown. The driving devices have slope controlled outputs for the falling edges with a fall time of 50 ns.

4.1 Shifting from a 3V to a 5V level.

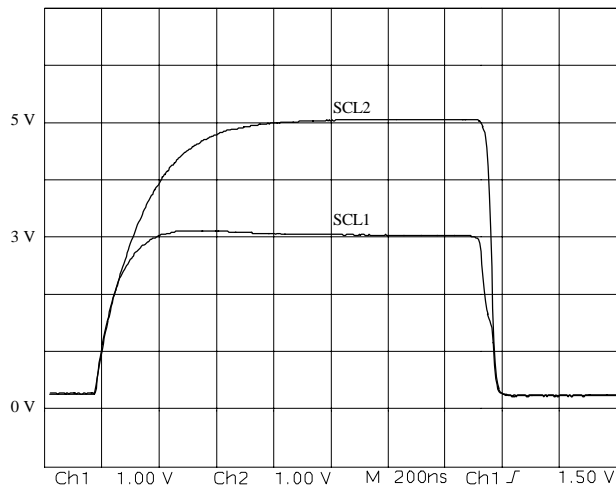


Figure 4.

Shifting from a 3V to a 5V level (200 ns/div).

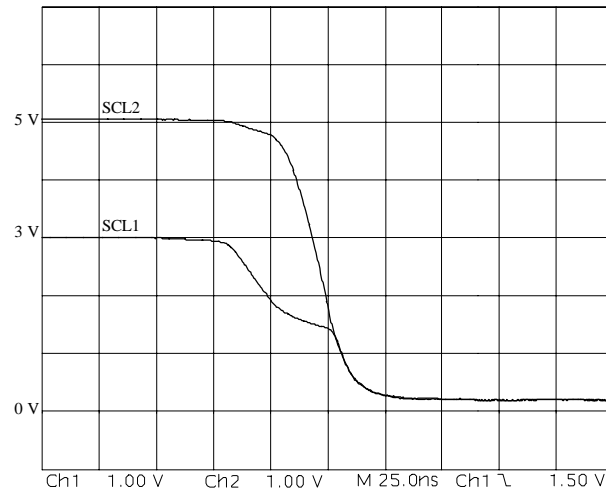


Figure 5.

Enlarged falling edge of fig. 4 (25 ns/div).

Figure 4 shows the level shifting from a "Lower level" to a "Higher level" section at 200 ns/div. time scale. A 3V device drives the SCL1 line and this wave form is shifted upwards to a 5 Volt wave form at SCL2. At about 2 Volt on the rising edge, the MOS-FET is switched off and each section rises smoothly with its own curve to its end value. Figure 5 gives an enlarged view of the falling edges at 25 ns/div. time scale. At about 2 Volt on the falling edge of SCL1, the MOS-FET becomes conducting and interconnects both bus line sections. It takes about 25 ns (between 100 and 125 ns of the time scale) to discharge SCL2 to the same voltage level of SCL1, showing an increase of the fall time of SCL1, but far within the 300 ns requirement of the I²C-bus specification. Afterwards both lines SCL1 and SCL2 are pulled LOW together smoothly.

Capacitive coupling via the MOS-FET between SCL1 and SCL2 shows some minor effect on the curves:

- a small overshoot of SCL1 during the rising edge of SCL2 (Figure 4),
- the first slow part of the falling edge of SCL2 due to the falling edge of SCL1 (Figure 5).

4.2 Shifting from a 5V to a 3V level.

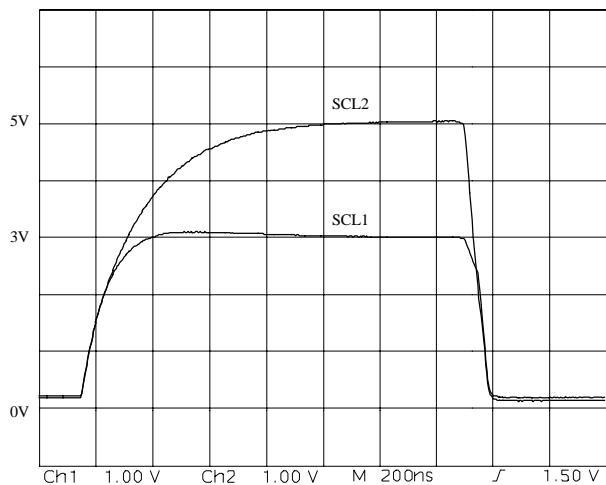


Figure 6.
Shifting from 5V to a 3V level (200 ns/div).

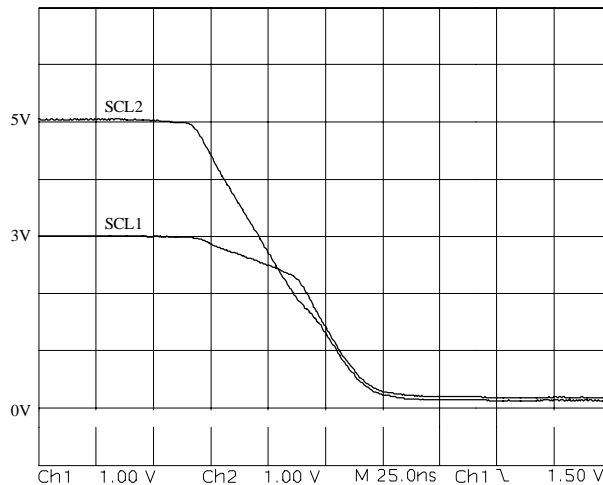


Figure 7.
Enlarged falling edge of fig. 6 (25 ns/div).

Figure 6 shows the level shifting from a “Higher level” to a “Lower level” at 200 ns/div. time scale. A 5V device drives the SCL2 line and this wave form is shifted downwards to a 3 Volt wave form at SCL1. At about 2 Volt on the rising edge, the MOS-FET is switched off and each section rises smoothly with its own curve to its end value. Figure 7 gives an enlarged view of the falling edges at 25 ns/div. time scale. At about 2 Volt on the falling edge of SCL2, the MOS-FET becomes conducting and interconnects both bus line sections. SCL2 and SCL1 are then about at the same voltage level, and both lines are pulled LOW together smoothly. Capacitive coupling via the MOS-FET between SCL1 and SCL2 shows some minor effect on the curves:

- a small overshoot of SCL1 during the rising edge of SCL2 (Figure 6),
- the first slow part of the falling edge of SCL1 due to the falling edge of SCL2 (Figure 7).

4.3 Wave forms when a bus section is powered-down.

Figure 8 and 9 show the wave forms of the logic levels if a section is powered-down in the bus systems of figure 2 and figure 3 respectively.

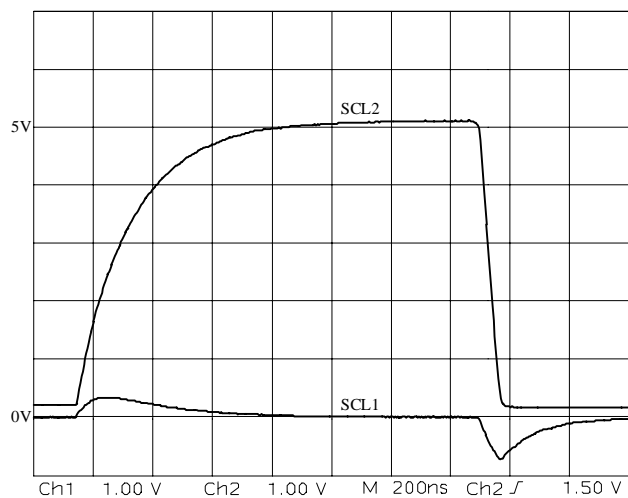


Figure 8.

“Lower voltage” section in fig.2 is powered-down.

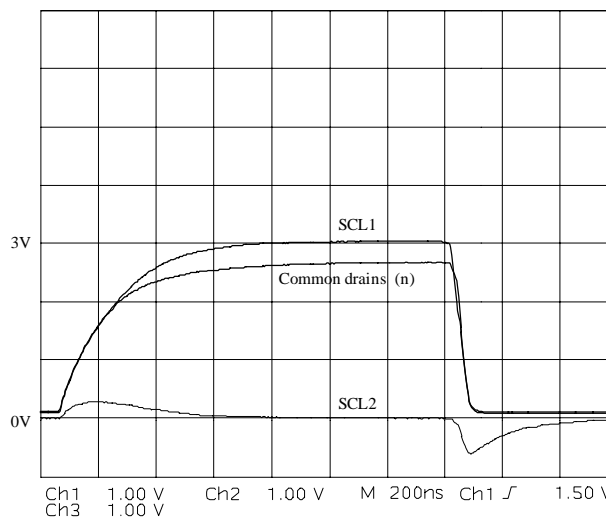


Figure 9.

“Higher voltage” section in fig.3 is powered-down

Figure 8 shows the situation when VDD1 is 0 Volt, so the “Lower voltage” section is powered-down in the bus system of fig.2. The “Higher voltage” section stays operational and a clock pulse is present on the SCL2 line. The SCL1 line stays at a LOW level with some positive and negative cross-talk effects via the drain-source capacitance of the not conducting MOS-FET T2.

Figure 9 shows the situation when VDD2 is 0 Volt and the “High voltage” section is powered-down in the bus system of fig.3. The “Lower voltage” section stays operational and a clock pulse is present on the SCL1 line. The SCL2 line stays at a LOW level with some positive and negative capacitive cross-talk effects via the drain-source capacitance of the not conducting MOS-FET T4. The pull-up resistors to VDD3 are not present, and the common drains follow the SCL1 HIGH level minus the voltage drop of the internal drain-substrate diode of T2. During the LOW level T2 is conducting and the common drains (d) have the same level as SCL1.

If pull-up resistors to VDD3 are present, then the HIGH level of the common drains (d) will be pulled up to the VDD3 level when SCL1 line is HIGH (equal as SCL2 in fig.4). In this case it is also possible to connect “Higher voltage” devices direct to the common drains (d). These devices have VDD3 as supply voltage, which is not switched off.

The use of the above level shift circuits gives extensive possibilities to I²C-bus systems to connect, power-down and protect I²C-bus devices with different supply voltages and logic levels.
