



YAC523

EVR2

Electric Variable Resistance 2

■ Outline

YAC523 (EVR2) is a 7ch high grade digital volume LSI for high-end audio systems.

Owing to its built-in high-quality sound operational amplifier, output with wide dynamic range and low distortion factor can be obtained.

YAC523 is able to control each channel through a serial data interface in 255 steps at 0.5dB per step, and can allow configuration of a system with 8 channels or more by using a daisy chain connection.

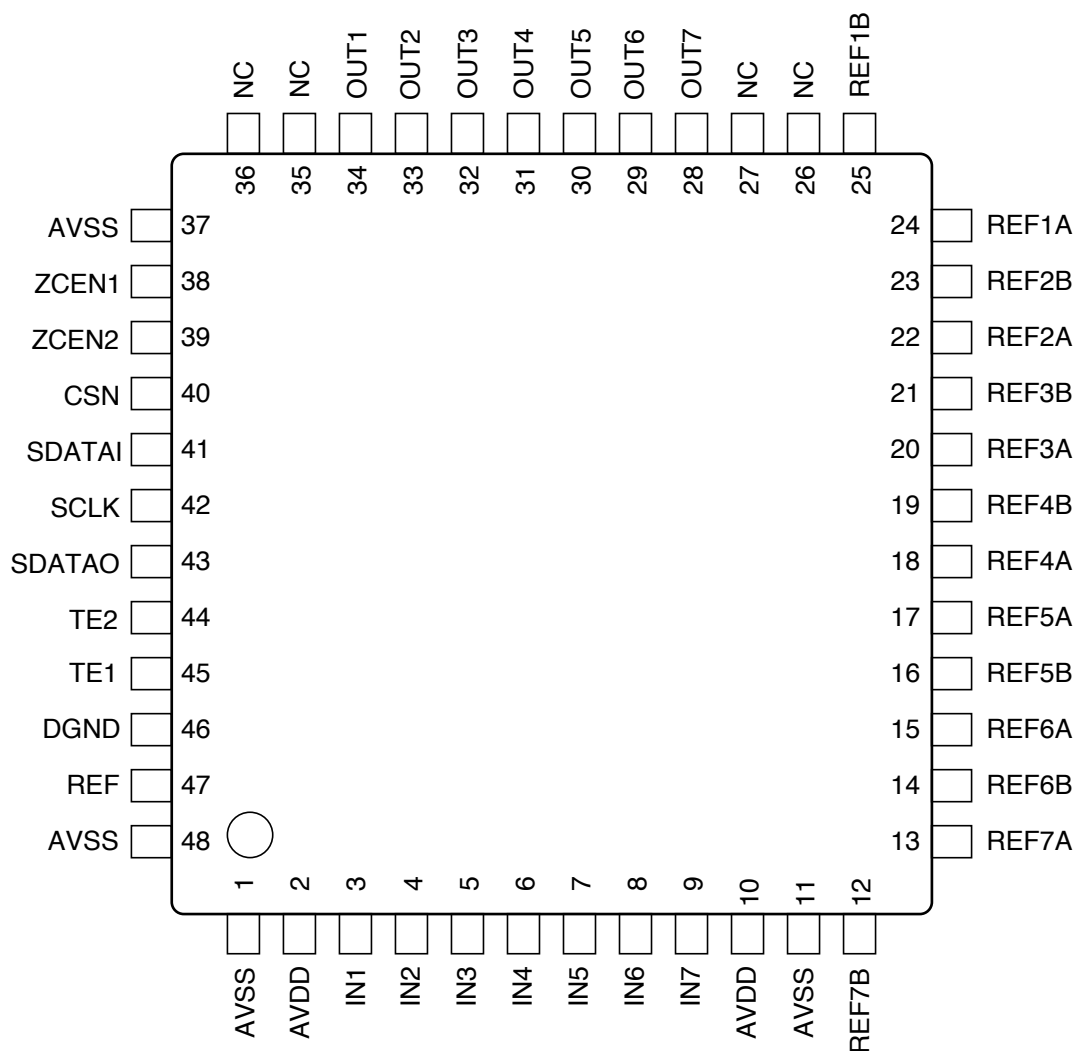
Owing to its zero-cross detection function, the device is able to suppress audible noise that may occur at a quick volume change.

■ Features

- Built-in 7channel high sound quality operational amplifier.
- Wide volume range.
+ 31.5dB ~ - 95.0dB, MUTE (0.5dB/step, 255 steps)
- Maximum input signal amplitude
4.2Vrms ($\pm 6V$ power supply)
- Low distortion (THD)
0.0004% typ. (Input=1Vrms@1kHz, Gain=0dB)
- Low residual noise
1.2 μ Vrms typ. (Gain=MUTE, IHF-A)
- Power supply voltage
 $\pm 4.75V \sim \pm 6.6V$
- Silicon gate CMOS process.
- 48-pin plastic LQFP (YAC523-VZ)

■ Terminal configuration

YAC523-VZ



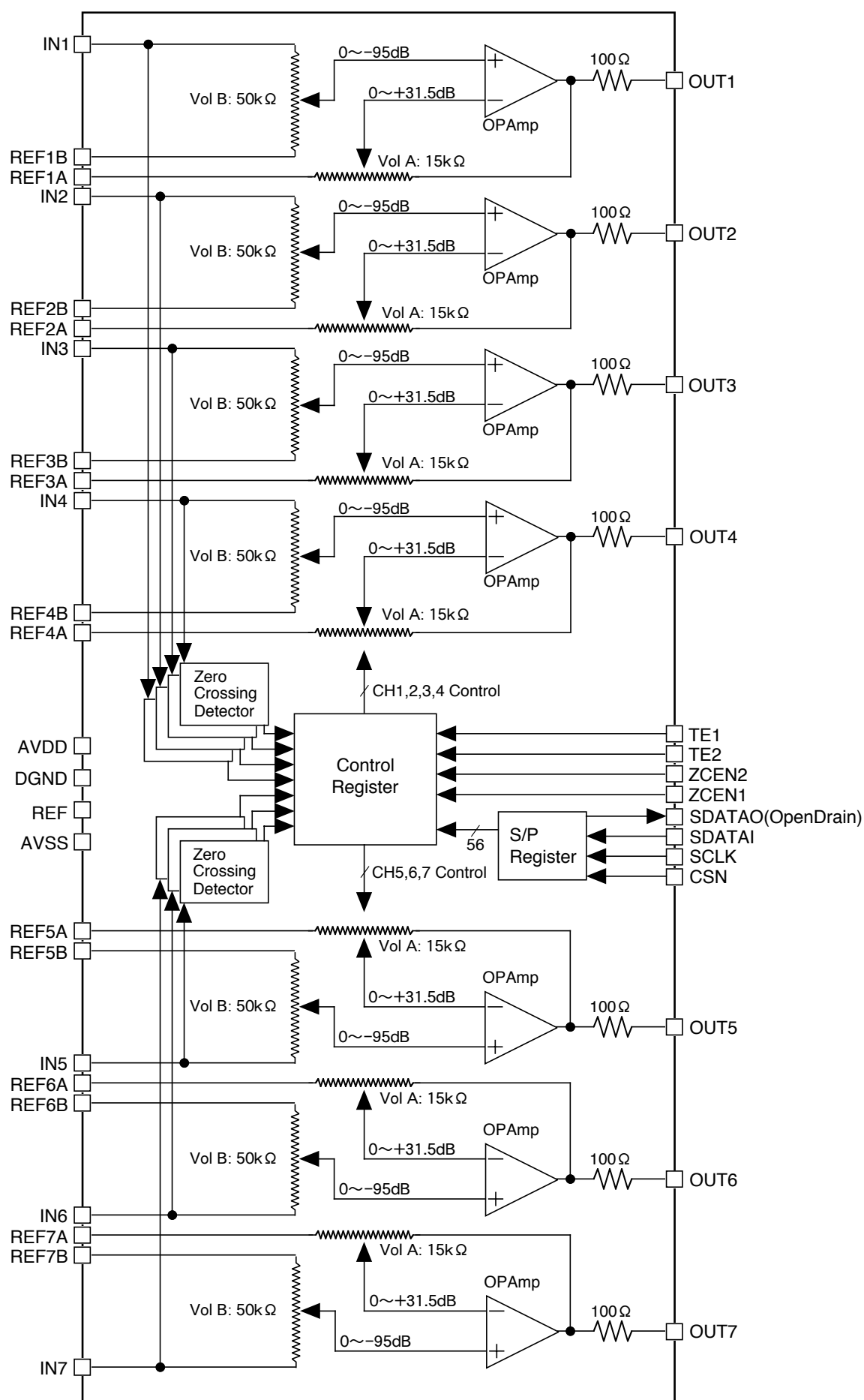
<48 pin LQFP TopView>

■ Terminal function

No.	Name	I/O	Function
1	AVSS	—	Minus power supply for analog (-6.0V Typ.)
2	AVDD	—	Plus power supply for analog (+6.0V Typ.)
3	IN1	AI	ch1 analog input
4	IN2	AI	ch2 analog input
5	IN3	AI	ch3 analog input
6	IN4	AI	ch4 analog input
7	IN5	AI	ch5 analog input
8	IN6	AI	ch6 analog input
9	IN7	AI	ch7 analog input
When avoid the use of this terminal, connect to ground. And please use the output impedance of the source of input signal less than 2.2k Ω .			
10	AVDD	—	Plus power supply for analog (+6.0V Typ.)
11	AVSS	—	Minus power supply for analog (-6.0V Typ.)
12	REF7B	AI	ch7 analog reference voltage input 7B Connect to ground directly.
13	REF7A	AI	ch7 analog reference voltage input 7A Connect to ground through 33 μ F.
14	REF6B	AI	ch6 analog reference voltage input 6B Connect to ground directly.
15	REF6A	AI	ch6 analog reference voltage input 6A Connect to ground through 33 μ F.
16	REF5B	AI	ch5 analog reference voltage input 5B Connect to ground directly.
17	REF5A	AI	ch5 analog reference voltage input 5A Connect to ground through 33 μ F.
18	REF4A	AI	ch4 analog reference voltage input 4A Connect to ground through 33 μ F.
19	REF4B	AI	ch4 analog reference voltage input 4B Connect to ground directly.
20	REF3A	AI	ch3 analog reference voltage input 3A Connect to ground through 33 μ F.
21	REF3B	AI	ch3 analog reference voltage input 3B Connect to ground directly.
22	REF2A	AI	ch2 analog reference voltage input 2A Connect to ground through 33 μ F.
23	REF2B	AI	ch2 analog reference voltage input 2B Connect to ground directly.
24	REF1A	AI	ch1 analog reference voltage input 1A Connect to ground through 33 μ F.
25	REF1B	AI	ch1 analog reference voltage input 1B Connect to ground directly.
26	NC	—	Non connection or connect to ground.
27	NC	—	Non connection or connect to ground.
28	OUT7	AO	ch7 analog output
29	OUT6	AO	ch6 analog output
30	OUT5	AO	ch5 analog output
31	OUT4	AO	ch4 analog output
32	OUT3	AO	ch3 analog output
33	OUT2	AO	ch2 analog output
34	OUT1	AO	ch1 analog output
35	NC	—	Non connection or connect to ground.
36	NC	—	Non connection or connect to ground.
37	AVSS	—	Minus power supply for analog (-6.0V Typ.)
38	ZCEN1	I	Zero-cross control input 1. Select one from four types of zero-cross modes including non-zero-cross mode. When changing zero-cross modes during operation, set the system so that it changes at 1 second or more after the rise of CSN signal.
39	ZCEN2	I	Zero-cross control input 2. Select one from four types of zero-cross modes including non-zero-cross mode. When changing zero-cross modes during operation, set the system so that it changes at 1 second or more after the rise of CSN signal.
40	CSN	I	Chip select input
41	SDATAI	I	Serial data input
42	SCLK	I	Serial clock input
43	SDATAO	OD	Serial data output Serial data are outputted from this terminal when CSN pin is "L" level. This terminal becomes high-impedance state when CSN pin is "H". Since it is an open drain output pin, pull it up through a resistor to the power supply voltage (to be AVDD or less) of a device to be connected. Do not allow output current of 1.5mA or over.
44	TE2	I	Test terminal Non connection or connect to DGND terminal.
45	TE1	I	Test terminal Non connection or connect to DGND terminal.
46	DGND	—	Digital ground
47	REF	O	Reference voltage output for digital For attaining stabilization, connect this terminal to AVSS terminal through a capacitance of 10 μ F or higher (CREF). And please do not use this terminal output for the drive purpose of an external circuit.
48	AVSS	—	Minus power supply for analog (-6.0V Typ.)

Note A: analog terminal, OD: Open drain output terminal, "L" level means V_{IL} , "H" level means V_{IH} .

Internal block diagram



■Description of functions

●Analog functions

- Maximum input voltage

The maximum amplitude of the input signal that is inputted to the analog input pin of YAC523 is 4.2Vrms when power supply voltage is $\pm 6V$.

For a system to which a signal exceeding the power supply voltage (AVDD/AVSS) may be applied, use external diodes to suppress the signal to the maximum rating or less.

- Maximum output voltage

The maximum output voltage(THD<1%) of the signal that is outputted from the analog output pin of YAC523 is 4.2Vrms when power supply voltage is $\pm 6V$ and no load is connected. The output impedance is 100 Ω (typ.).

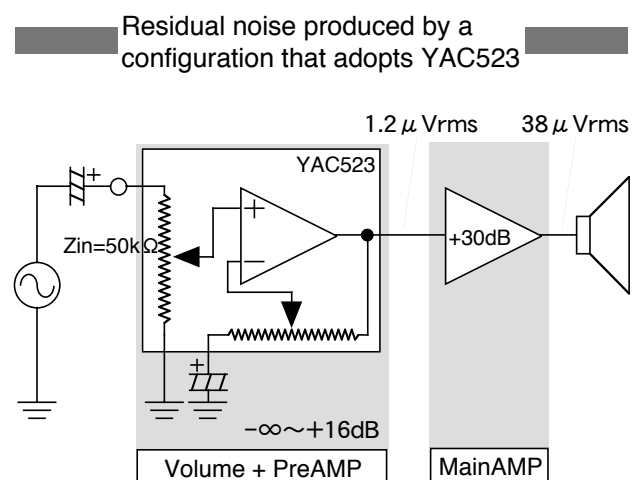
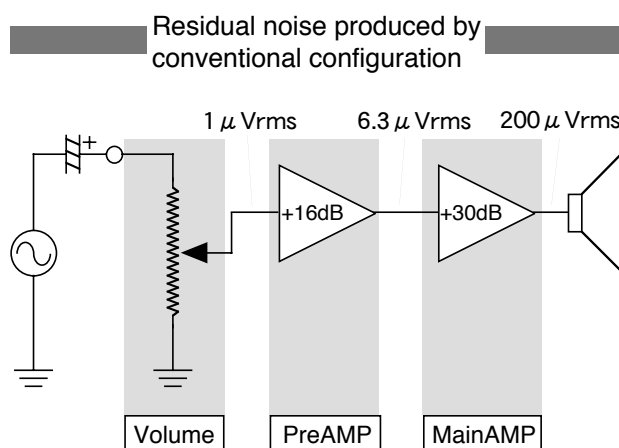
●Realization of low residual noise system

General audio amplifiers are designed to have input sensitivity of approximately 150mV, and have a gain of approximately 16dB at the preamplifier (PreAMP) section and approximately 30dB at the main amplifier section (MainAMP).

The residual noise of YAC523 (Gain= $-\infty$) is 1.2 μV rms (typ.) which is very small, and the device has positive side gain (max: 31.5dB). Therefore, by using YAC523 also as "PreAMP", systems with a very small residual noise and amplification of volume control noise can be configured.

For conventional configurations that need a "PreAMP", even if the residual noise of the volume control itself is zero, the noise that is produced at the "PreAMP" is amplified by the gain, the noise becomes very high when it is heard at the speakers.

When the input converted noise of "PreAMP" is 1 μV , the conventional configuration produces noise of approximately 200 μV at the speakers. For the configuration that uses YAC523, the noise is 38 μV which is very small.

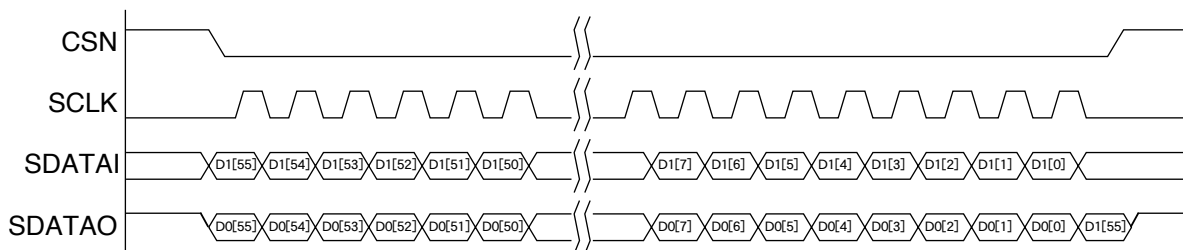


● Digital functions

• Serial data interface

Writing of volume control data into YAC523 is performed through a serial interface. SDATAI is a serial data input pin, SCLK is a clock input pin, and CSN is a chip select pin for writing the value of volume. The serial data that is inputted from SDATAI (MSB first) is taken into YAC523 at the rising edge of SCLK when CSN terminal is at "L" level. The serial data is latched at the rising edge of CSN, and volume value of each channel is set into the register. The present volume value is outputted from SDATAO pin as serial data. With this data, the control by using daisy chain connection and verification of the present volume value can be performed easily.

Note that the register value after turning the power supply on is ALL "0" (muted state) and the interface is enabled after a predetermined period (tPUP) has elapsed. (Serial access is prohibited in tPUP period.)



Assignment of volume control data

D[55:48]	: Channel1 Volume data
D[47:40]	: Channel2 Volume data
D[39:32]	: Channel3 Volume data
D[31:24]	: Channel4 Volume data
D[23:16]	: Channel5 Volume data
D[15: 8]	: Channel6 Volume data
D[7: 0]	: Channel7 Volume data

D1[55:0] is volume data value to change.

D0[55:0] is present volume data value.

• Daisy chain

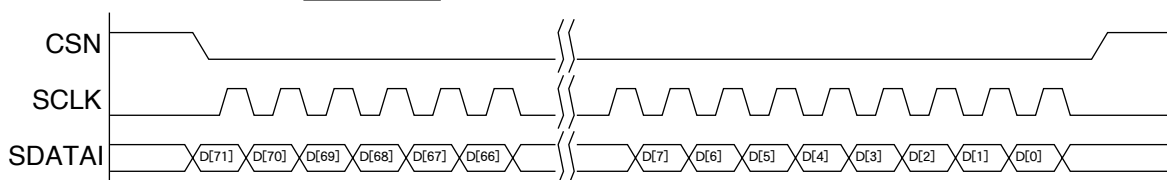
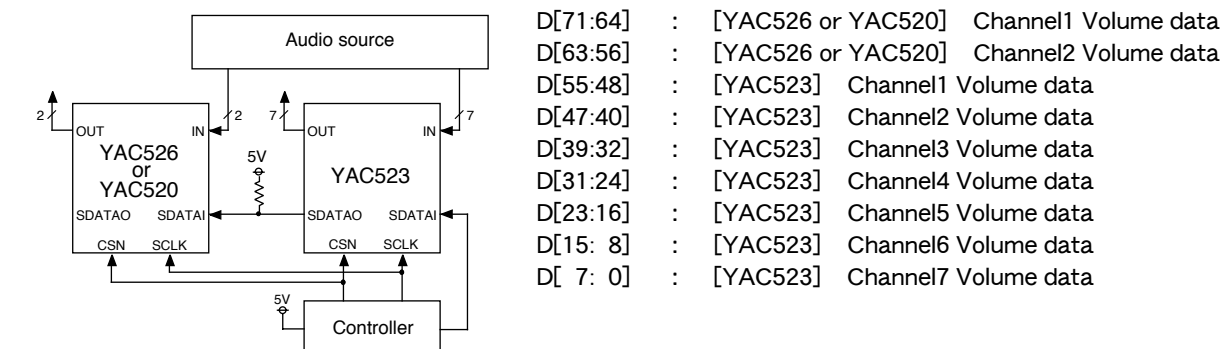
Since multiple YAC523 devices can be connected by using the daisy chain connection, systems with 8 channels or more can be attained.

For example, by connecting the device with YAC526 (2ch digital volume) through daisy chain, 8.1ch system can be attained. By connecting SDATAO pin of YAC523 (or YAC526) to SDATAI pin of YAC526 (YAC523), YAC523 and YAC526 can be controlled simultaneously without need of a complex addressing.

(It is also possible to connect multiple YAC523, or to connect the device with YAC520 through daisy chain.)

The volume data is taken into S/P (serial / parallel) registers of each LSI by setting CSN pin to "L" for 8 clock period on all channels that are connected with daisy chain. And, by setting CSN pin to "H" after the elapse of 8 clock period on all channels, the data is written from S/P registers of all YAC523 (or YAC526) that are connected with daisy chain into the control registers simultaneously to change the volume value.

Example: Assignment of volume control data when a combination of YAC523 and YAC526 (or YAC520) as described below is used.



• Volume setting

The relationship between input code and volume value is as shown in the following table.

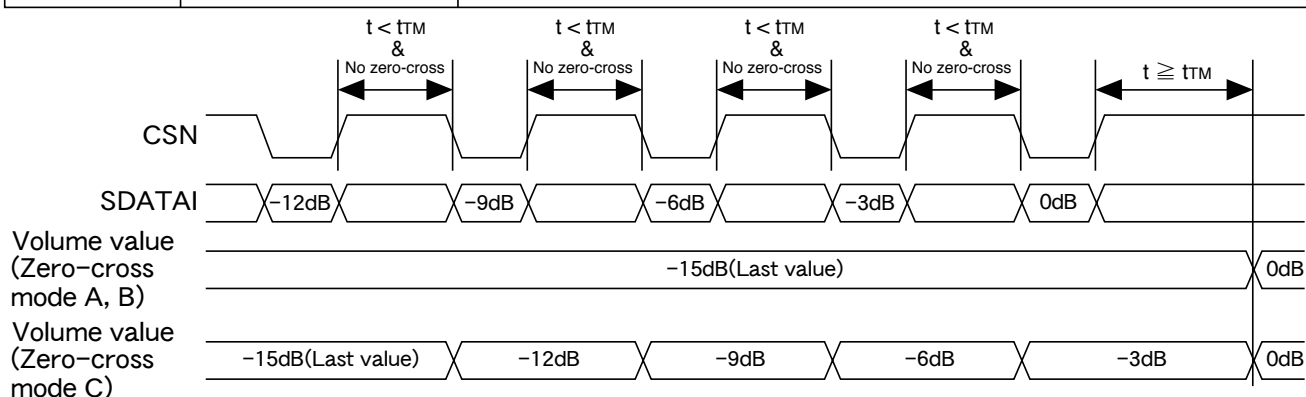
Input code	Gain or attenuate(dB)
11111111	MUTE
11111110	+31.5
⋮	⋮
11011111	+16.0
⋮	⋮
10111111	0
⋮	⋮
00000010	-94.5
00000001	-95.0
00000000	MUTE

The input codes ALL"0" and ALL"1" are set for mute.

• Zero-cross mode

YAC523 incorporates the zero-cross detection function to suppress audible noise when the volume is changed quickly. A mode is selected from the following four modes by setting ZCEN1 and 2 pins.

ZCEN[2:1]	Mode	Operation
00	Normal	Zero-cross is not detected, and the volume value is changed immediately after the rising of CSN.
01	Zero-cross mode A	Zero-cross is detected after the rising of CSN, or after t_{TM1} (20ms) passes, volume value is changed.
10	Zero-cross mode B	Zero-cross is detected after the rising of CSN, or after t_{TM2} (10ms) passes, volume value is changed.
11	Zero-cross mode C	When the next data is written within t_{TM1} (20ms) for zero-cross mode A, the changed is performed at the falling of CSN by using the volume value immediately before.



Operation in each zero-cross mode when zero-cross is not detected

Be careful not to change the zero-cross mode during the operation of the device, or an erroneous operation may be caused. Perform change of zero-cross mode after the elapse of 1 second or more from the rising of CSN signal.

• Power on reset

YAC523 builds in the power on reset function that resets the volume value when the power is turned on. Since a system that perform the reset by detecting the power supply voltage level, when turning on the power supply again, do it after the power supply voltage AVDD and AVSS has reduced sufficiently (to +1.0V/ -1.0V or less). Moreover, although a volume register is reset at the time of a power supply injection, since shocking sound occurs in the case of power supply ON/OFF, please apply mute to the whole set.

Power on reset is started when AVSS is 90%. At the time, AVDD should rise +1V or more. Since power-on reset may be unable to be completed when conditions cannot be fulfilled, please perform a re-setup of a volume register before canceling MUTE by the side of a set.

■ Electrical characteristics

1. Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
Power supply voltage	AVDD-AVSS		14.0	V
Analog input terminal voltage	VINA	AVSS -0.6	AVDD+0.6 and VINA-AVSS < 14.0V	V
Digital input terminal voltage	VIND	AVSS -0.3	AVDD+0.3	V
Storage temperature	TSTG	-50	125	°C

Note : DGND=0V

2. Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Analog power supply voltage(Positive)	AVDD	4.75	6.00	6.60	V
Analog power supply voltage(Negative)	AVSS	-6.60	-6.00	-4.75	V
Operating ambient temperature	TOP	-40		85	°C

Note : DGND=0V

3. Analog characteristics (Ta=25°C, AVDD=+6.0V, AVSS=-6.0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Gain range	Gain	-95.0		+31.5	dB
Step size			0.5		dB
Gain matching between channel (0~-40dB, 1kHz)			±0.1		dB
Gain matching between channel (@-80dB, 1kHz)			±0.2		dB
Step error (≥-80dB)			±0.1		dB
Input resistance	RI		50		kΩ
Output resistance	RO		100		Ω
Load capacitance	RL	5			kΩ
Input capacitance	CI			10	pF
Load capacitance	CL			100	pF
Maximum input voltage (THD<1%, RL=∞)	VI			4.2	Vrms
Maximum output voltage (THD<1%, RL=∞)	VO			4.2	Vrms
Output noise voltage1 (In=GND, Vol=+16dB) *1	Vn1		10.0		μVrms
Output noise voltage2 (In=GND, Vol=0dB) *1	Vn2		2.5		μVrms
Output noise voltage3 (In=GND, Vol=Mute) *1	Vn3		1.2		μVrms
Total harmonic distortion (In=1Vrms, Vol=0dB, 1kHz) *2	THD1		0.0004		%
Total harmonic distortion (In=1Vrms, Vol=0dB, 20kHz) *3	THD2		0.0055		%
Inter channel isolation (Vol=0dB, 1kHz)	Cs		-115		dB

Note : *1 : Input of other channels are analog ground, Band Width=IHF-A

*2 : Input of other channels are analog ground, Band Width=400Hz~30kHz

*3 : Input of other channels are analog ground, Band Width=400Hz~

4. Power consumption

Item	Symbol	Min.	Typ.	Max.	Unit
Power consumption(AVDD=+6V, AVSS=-6V, CSN="H")	PD		360		mW

5. DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH		2.2			V
Low level input voltage	VIL				0.8	V
Low level output voltage	VOL	IO= 1.5mA			0.4	V
Input leakage current	ILI				10	μA

6. AC characteristics (CL=20pF)

Item	Symbol	Min.	Typ.	Max.	Unit
Serial clock frequency	SCLK	0		1.0	MHz
Serial clock pulse width high	t _{PH}	500			ns
Serial clock pulse width Low	t _{PL}	500			ns
SDATAI set up time	t _{SDVS}	200			ns
SDATAI hold time	t _{SDH}	200			ns
CSN pulse width High	t _{CSPH}	1000			ns
CSN set up time	t _{CSVS}	500			ns
CSN hold time	t _{LTH}	200			ns
SDATAO data output set up time	t _{CSH}			300	ns
SDATAO output delay time	t _{SSD}			300	ns
SDATAO output data hold time (data output stop)	t _{CSDH}			200	ns
CSN, SCLK rise time	t _R			100	ns
CSN, SCLK fall time	t _F			100	ns
Zero-cross time out (Zero-cross MODE=A, C)	t _{TM1}		20		ms
Zero-cross time out (Zero-cross MODE=B)	t _{TM2}		10		ms
Regulation time until the data writing from a power supply injection (more than AVSS=90%) to LSI becomes effective. (C _{REF} =10 μ F)	t _{PUP}		20	50	ms

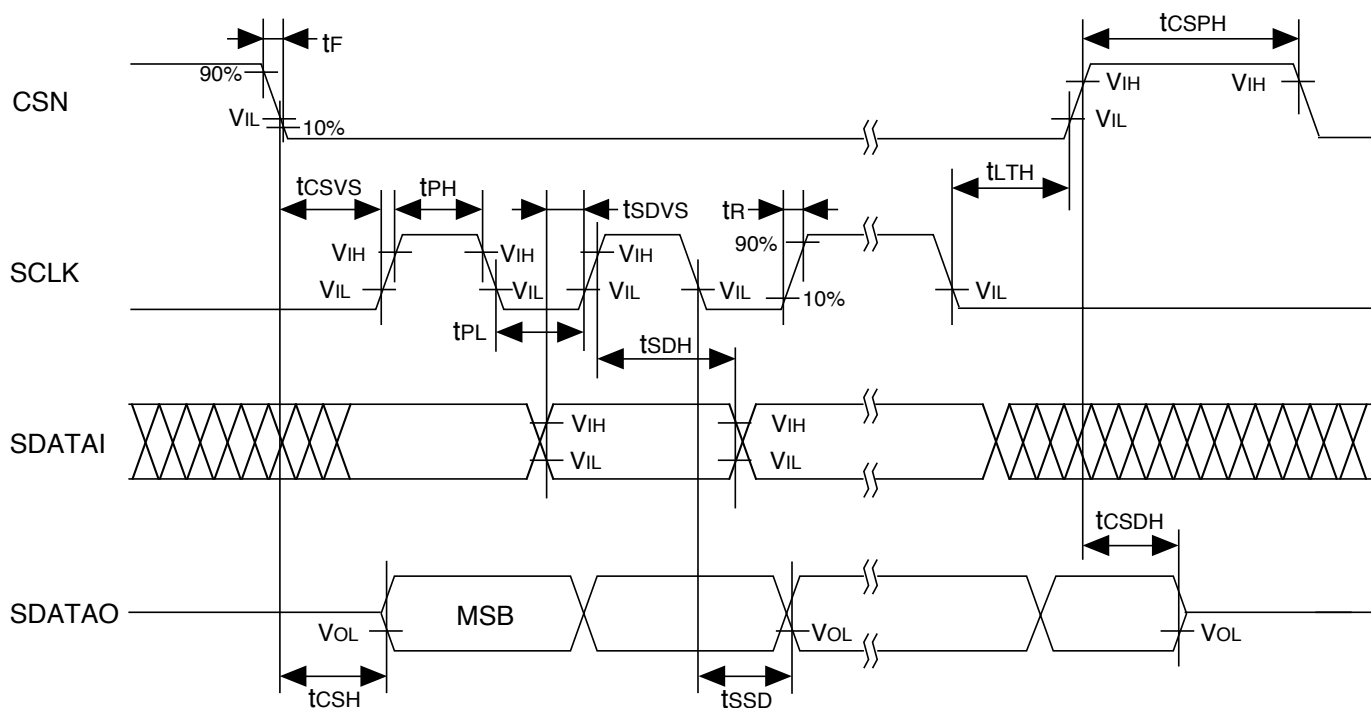
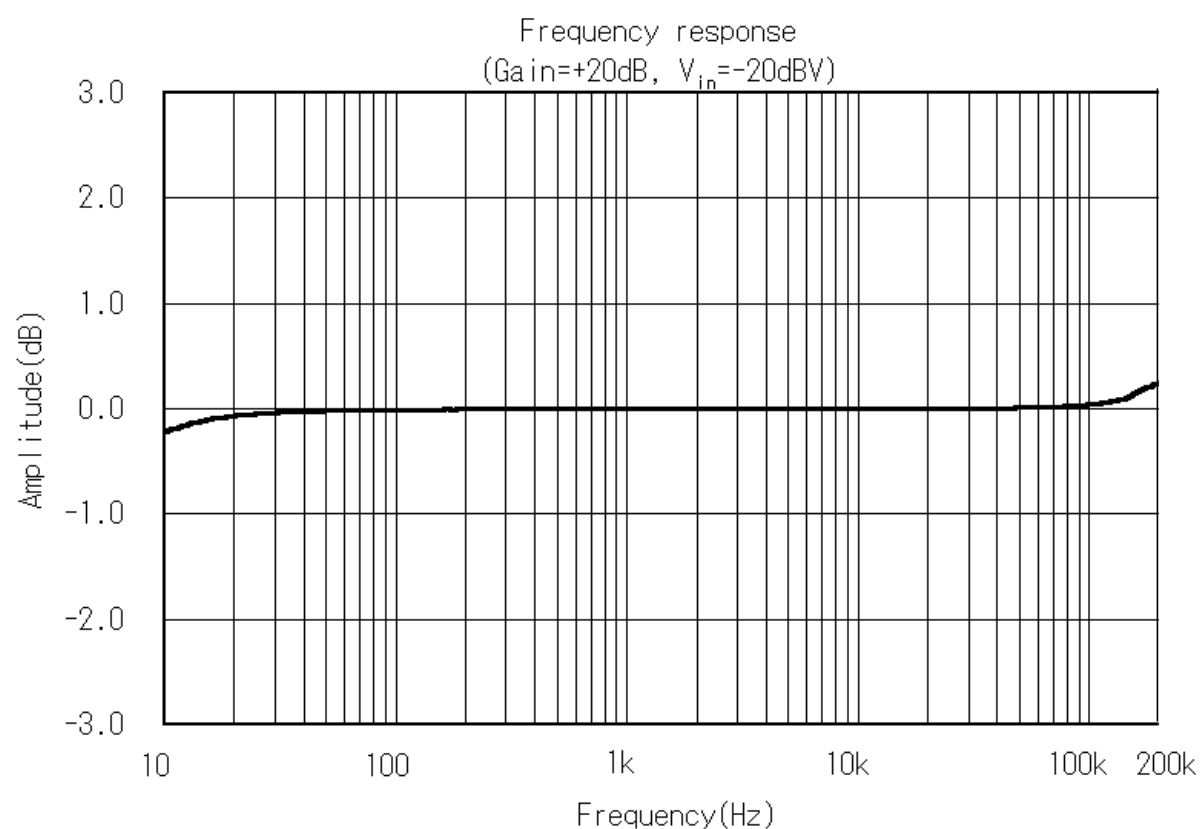
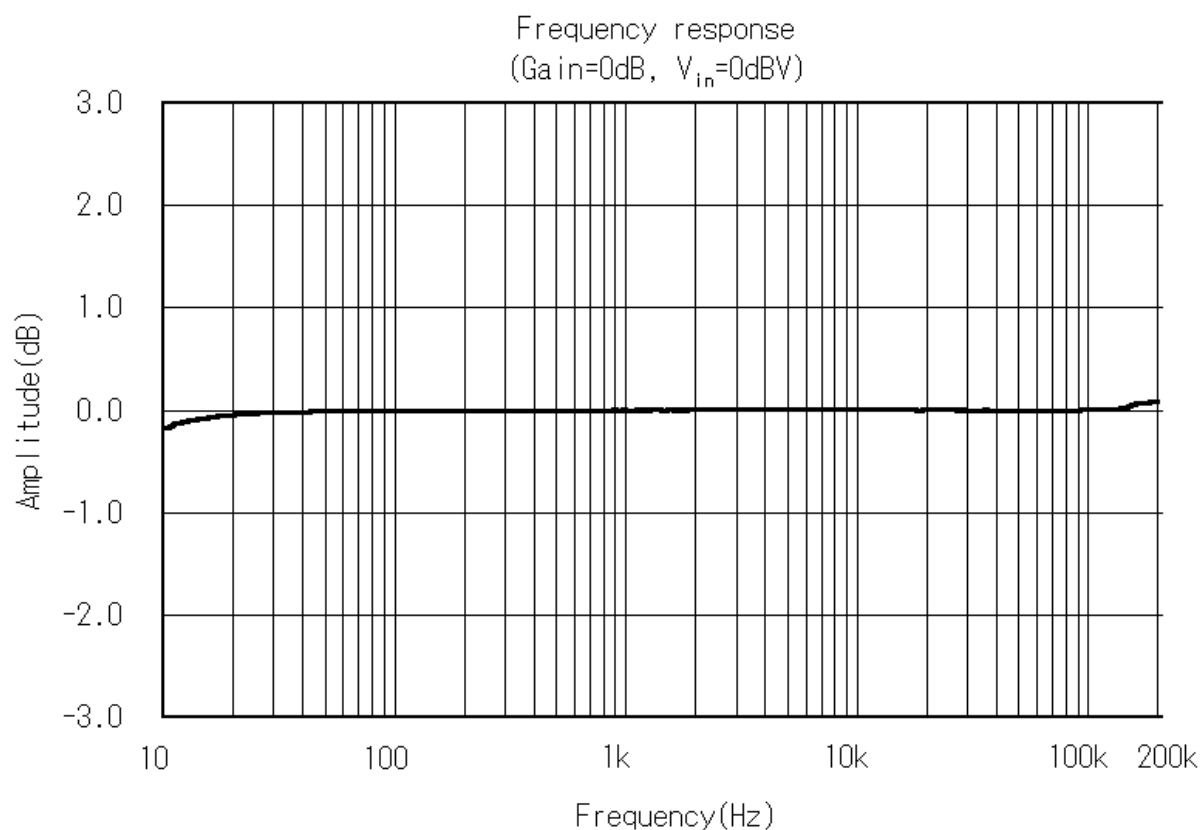
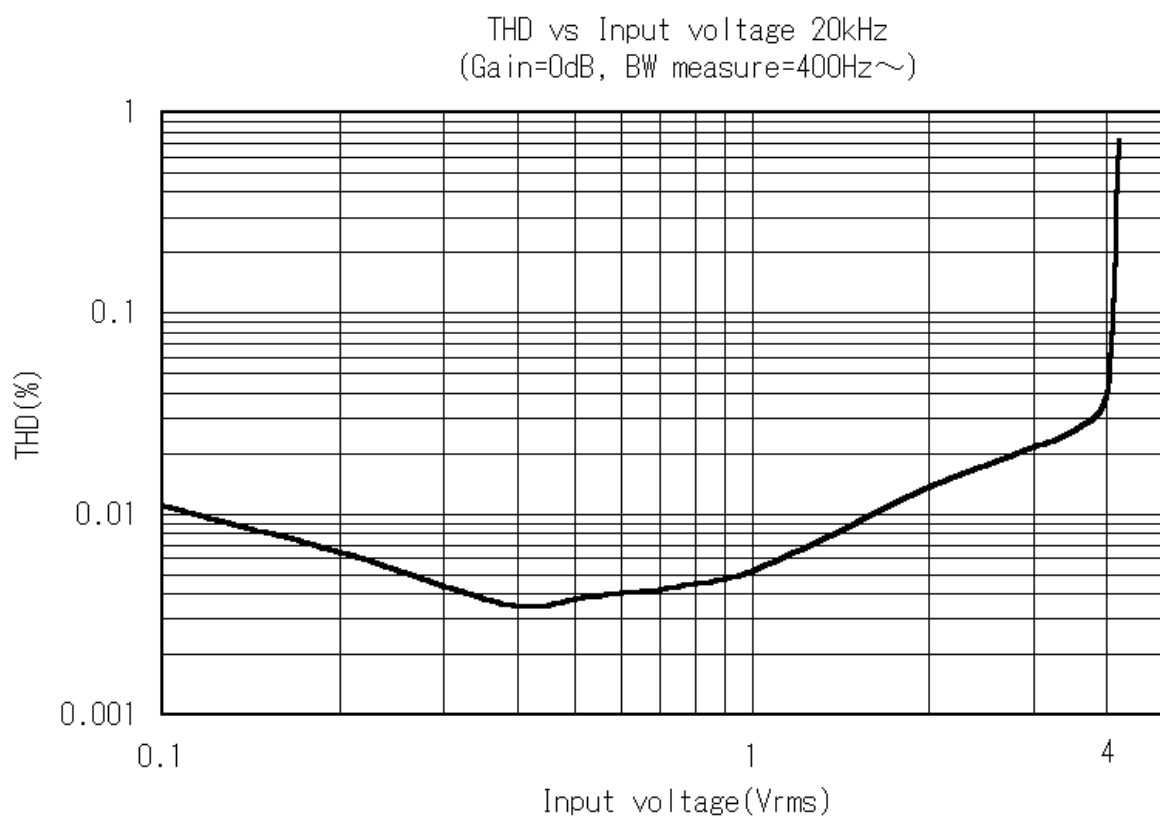
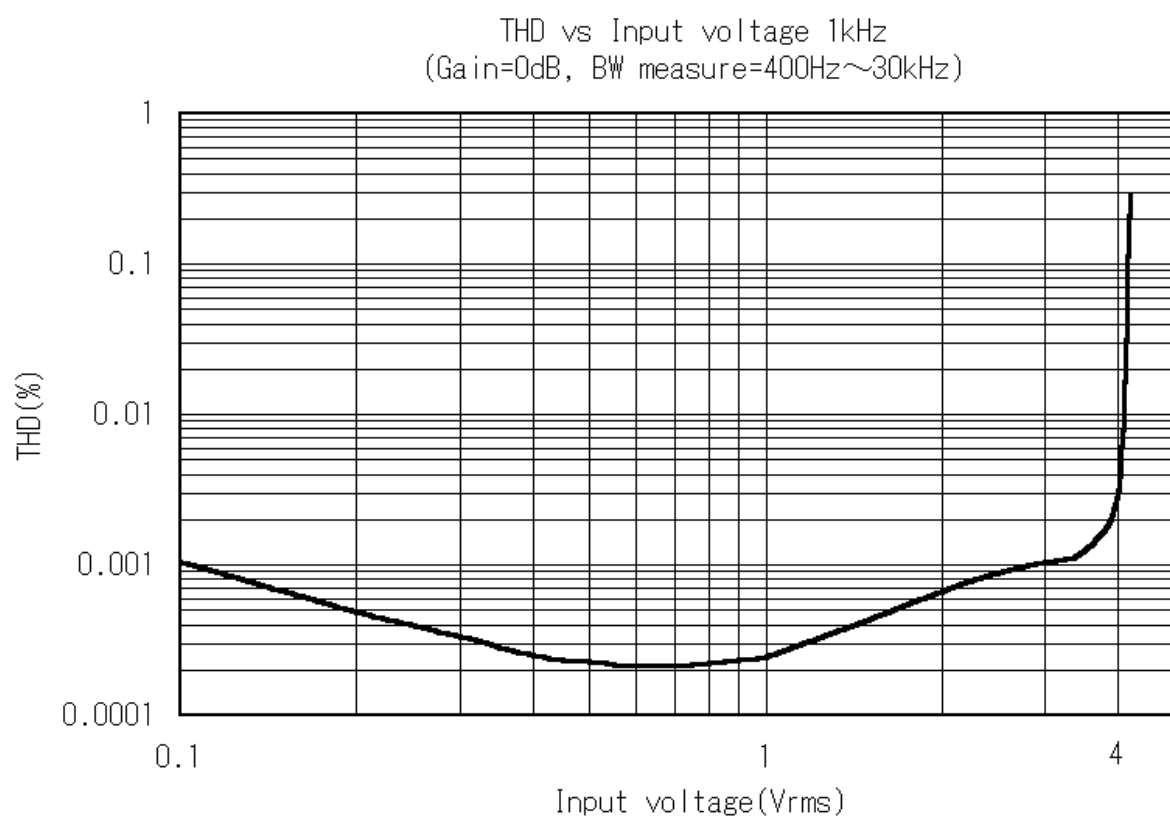


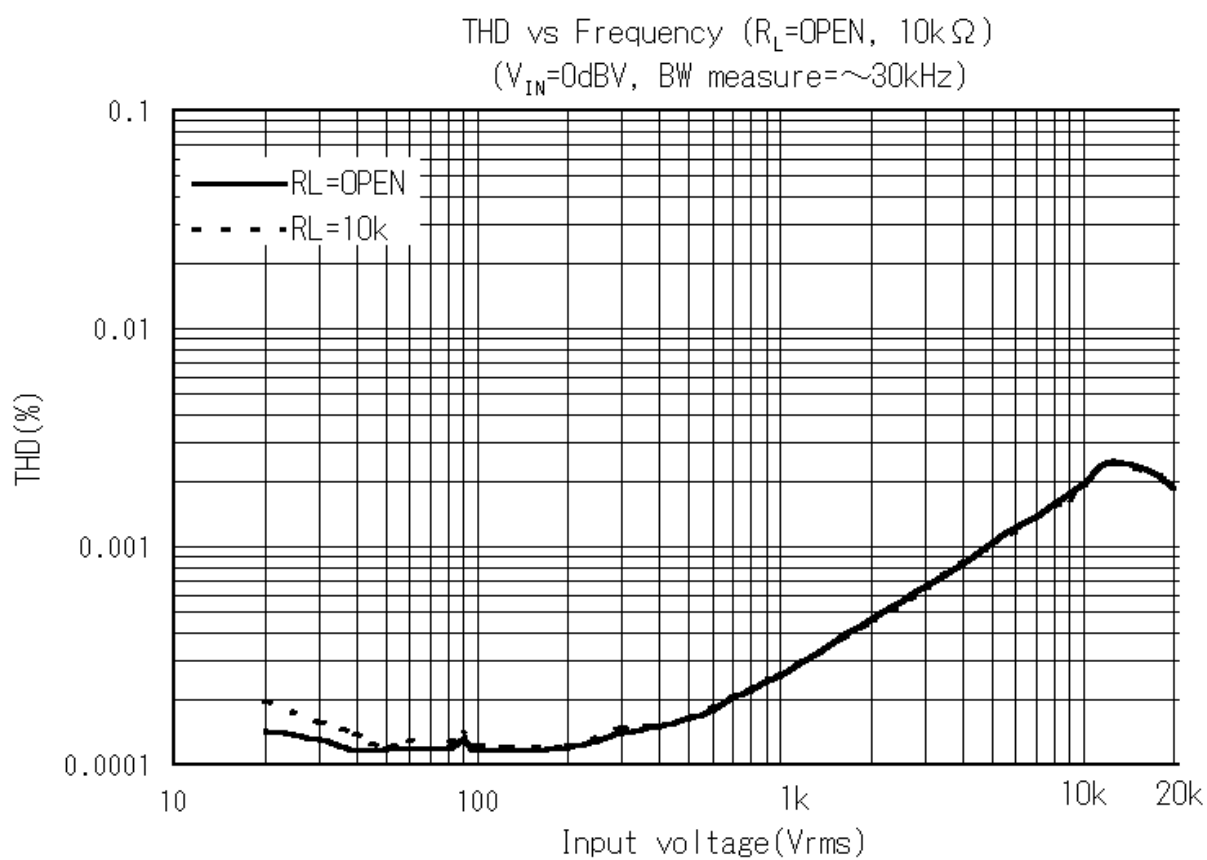
Fig 1 Serial port timing

■ Typical analog characteristic

As long as there is no description especially, it is $T_a=+25$ 、 $AVDD=+6V$ 、 $AVSS=-6V$ 、 $R_L=10k\Omega$ 、 $C_L=100pF$.







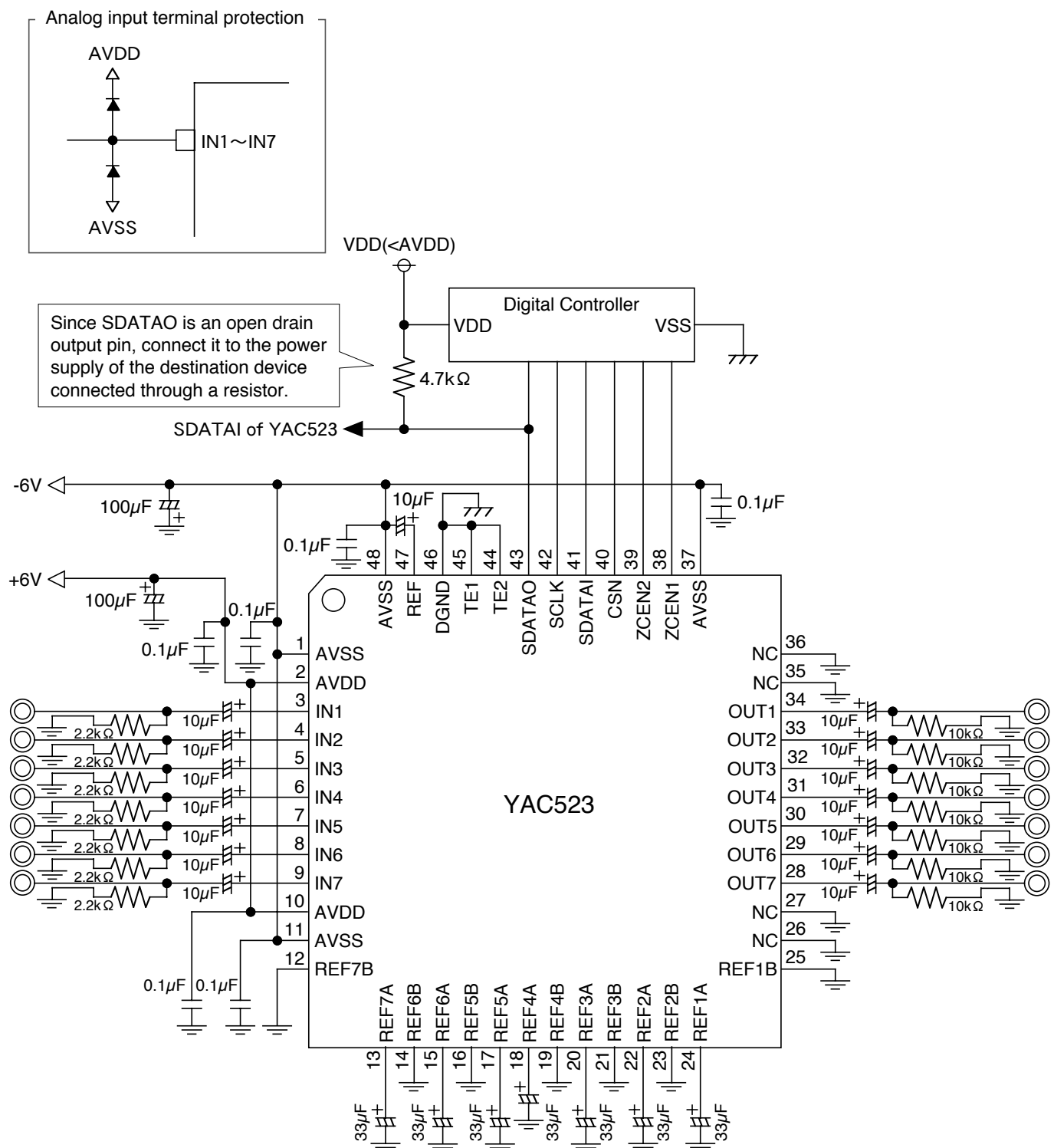
■ Example of system configuration

When there is a fear that voltage exceeding the maximum rating is applied to the analog input pins (IN1 to IN7) of YAC523, connect diodes between AVDD and AVSS as shown below to prevent application of voltage exceeding the maximum rating to the input pins.

Please make an analog domain and a digital domain into the ground side separated, respectively, and arrange YAC523 to an analog domain and the impedance to an AVSS pin should become small as much as possible.

And please secure an area large enough, and a radiation noise should fully be stopped and an analog ground and a digital ground also make it.

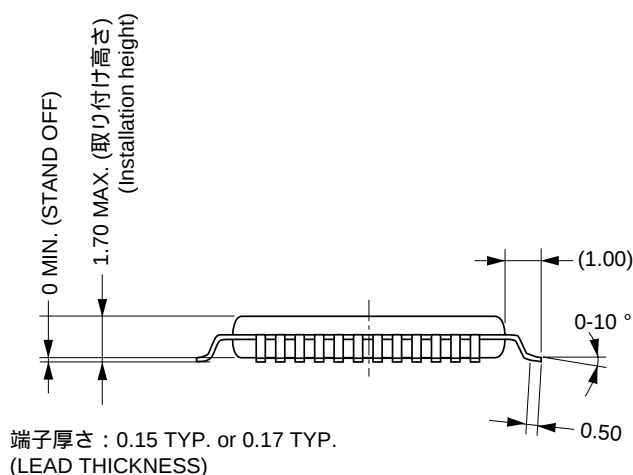
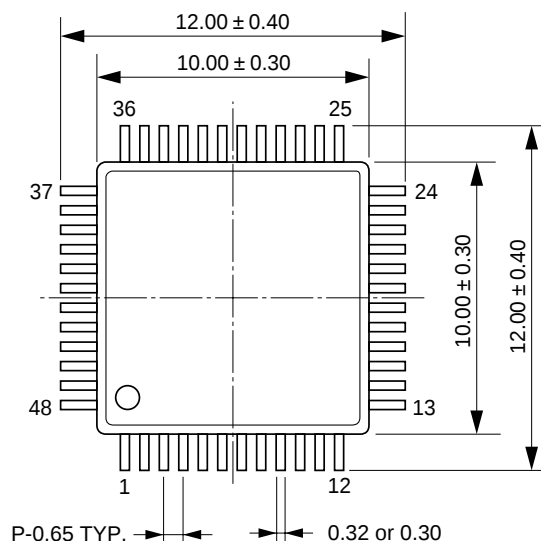
Control signals, such as serial interface, should wire a digital ground side collectively. In order to prevent interference with a control signal and an analog signal, be careful for an analog signal and a digital signal not to cross or not to adjoin.



■ External dimensions of package

YAC523-VZ

C-PK48VP-0



モールドコーナー形状は、本図面と若干異なるタイプもあります。カッコ内の寸法値は参考値とする。モールド外形寸法はバリを含まない。単位(UNIT) : mm(millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis () should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装 LSI は保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, please contact your nearest Yamaha agent.

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YAMAHA CORPORATION

Semiconductor Sales & Marketing Department

- Head Office 203, Matsunokijima, Toyooka-mura,
Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054
- Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088
- Osaka Office 3-12-12, Minami Senba, Chuo-ku
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229