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SED2800FVA CMOS VFD DRIVER

■ Description

The SED2800FVA is a CMOS LSI dot-matrix vacuum fluorescent display anode and grid driver. It has 40 high-voltage anode outputs and 40 high-voltage grid outputs in 2 × 20 blocks.

The SED2800FVA has independent serial inputs and outputs for each 20–element block which feature data transfer rates of up to 4 Mbits/s. The daisy-chain serial data transfer system simplifies controller requirements. An automatic shutdown circuit turns off output drivers when power is removed from the logic circuits, simplifying power supply design.

The SED2800FVA uses a 5V logic supply and a 30 to 70V display supply, and is available in 100-pin plastic flatpacks.

■ Features

- 40 anode and 40 grid output drivers
- 70V, 10 mA grid drive capability
- 70V, 2 mA anode drive capability
- Automatic shutdown circuit
- Up to 4 Mbits/s serial data transfer rate
- Daisy-chain data transfer system for cascaded operation
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 100-pin plastic flatpack (QFP5-100pin)

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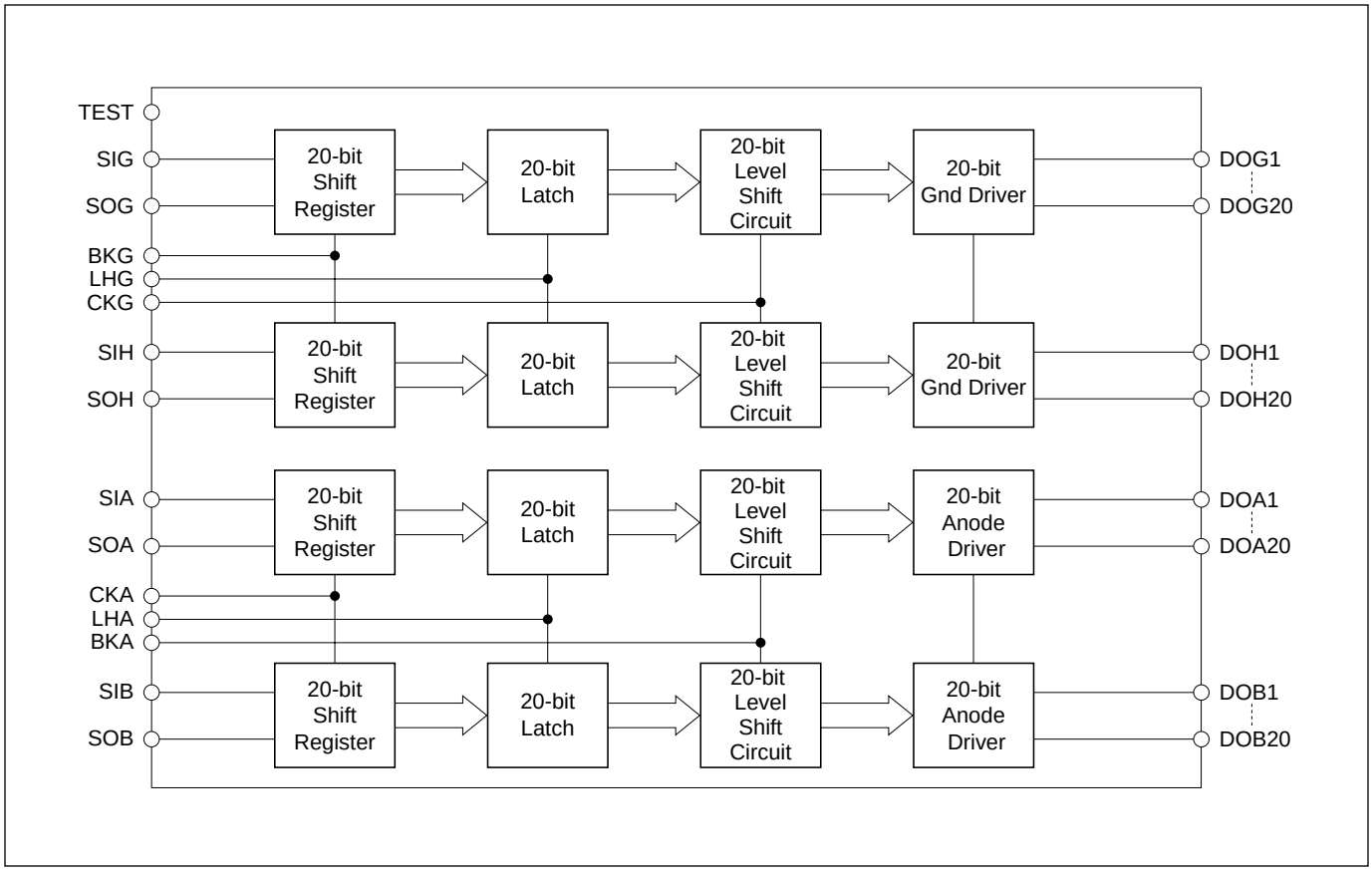
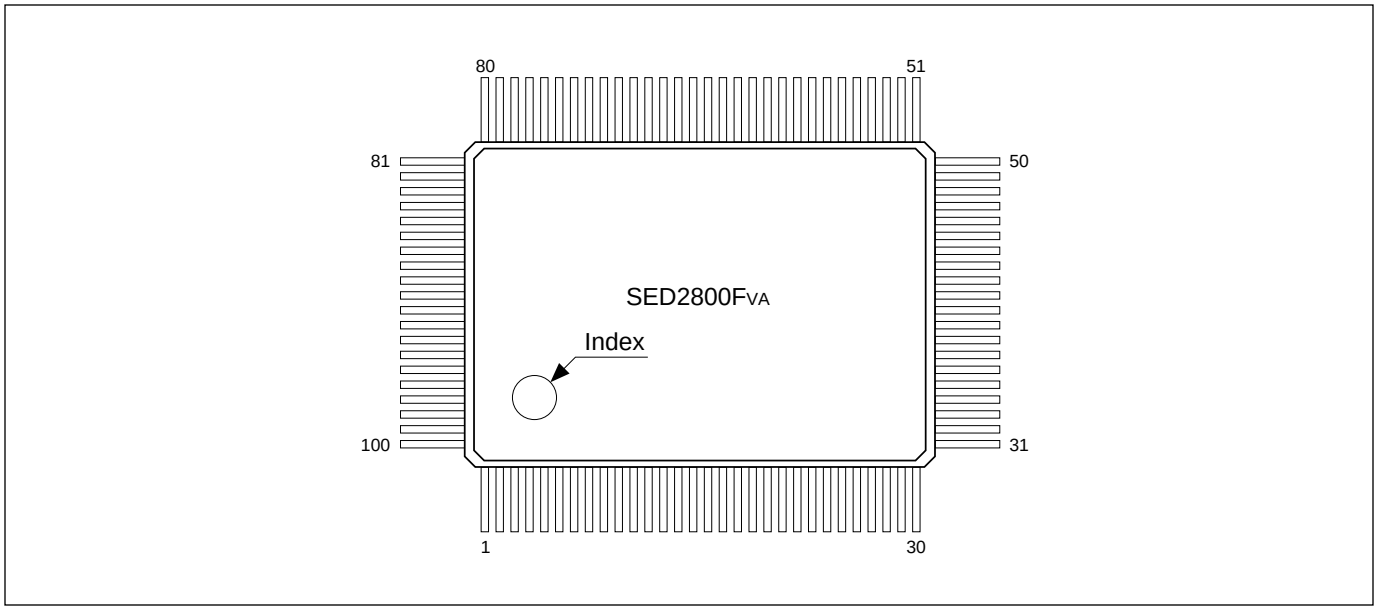
■ Block Diagram



■ Pinout



■ Pin Description

Pin		Pin		Pin		Pin	
Number	Name	Number	Name	Number	Name	Number	Name
1	DOB20	26	DOA15	51	DOH10	76	DOG5
2	DOB19	27	DOA14	52	DOH9	77	DOG4
3	DOB18	28	DOA13	53	DOG8	78	DOG3
4	DOB17	29	DOA12	54	DOH7	79	DOG2
5	DOB16	30	DOA11	55	DOH6	80	DOG1
6	DOB15	31	DOA10	56	DOH5	81	VDDH
7	DOB14	32	DOA9	57	DOH4	82	VSS
8	DOB13	33	DOA8	58	DOH3	83	TEST
9	DOB12	34	DOA7	59	DOH2	84	SIG
10	DOB11	35	DOA6	60	DOH1	85	CKG
11	DOB10	36	DOA5	61	DOG20	86	LHG
12	DOB9	37	DOA4	62	DOG19	87	BKG
13	DOB8	38	DOA3	63	DOG18	88	SOG
14	DOB7	39	DOA2	64	DOG17	89	SIH
15	DOB6	40	DOA1	65	DOG16	90	SOH
16	DOB5	41	DOH20	66	DOG15	91	SIA
17	DOB4	42	DOH19	67	DOG14	92	CKA
18	DOB3	43	DOH18	68	DOG13	93	LHA
19	DOB2	44	DOH17	69	DOG12	94	BKA
20	DOB1	45	DOH16	70	DOG11	95	SOA
21	DOA20	46	DOH15	71	DOG10	96	SIB
22	DOA19	47	DOH14	72	DOG9	97	SOB
23	DOA18	48	DOH13	73	DOG8	98	VDDL
24	DOA17	49	DOH12	74	DOG7	99	VSS
25	DOA16	50	DOH11	75	DOG6	100	VDDH

■ Pin Description

Number	Name	Description
1 to 20	DOB20 to DOB1	Parallel anode driver B outputs
21 to 40	DOA20 to DOA1	Parallel anode driver A outputs
41 to 60	DOH20 to DOH1	Parallel grid driver H outputs
61 to 80	DOG20 to DOG1	Parallel grid driver G outputs
81	VDDH	30 to 70V output driver supply input
82	VSS	Ground
83	TEST	Test input. Tied LOW for normal operation
84	SIG	Serial grid data input G
85	CKG	Serial grid data input clock
86	LHG	Active-HIGH grid data latch input
87	BKG	Active-HIGH grid driver blanking input. Used to disable output circuitry while parallel data is being latched
88	SOG	Serial grid data output G
89	SIH	Serial grid data input H
90	SOH	Serial grid data output H
91	SIA	Serial anode data input A
92	CKA	Serial anode data input clock
93	LHA	Active-HIGH anode grid data latch input
94	BKA	Active-HIGH anode driver blanking input. Used to disable output circuitry while parallel data is being latched
95	SOA	Serial anode data output A
96	SIB	Serial anode data input B
97	SOB	Serial anode data output B
98	VDDL	5V logic supply input
99	VSS	Ground
100	VDDH	30 to 70V output driver supply input. Referenced to VSS

■ Electrical Characteristics

● Absolute Maximum Ratings

V_{SS} = 0V

Parameter		Symbol	Rating	Unit
Driver supply voltage range		V_{DDH}	–0.3 to 70	V
Logic supply voltage range		V_{DDL}	–0.3 to 7	V
Driver output voltage range		V_{DO}	V_{SS} – 0.3 to V_{DDH} + 0.3	V
Input voltage range		V_{IN}	V_{SS} – 0.3 to V_{DDL} + 0.3	V
Logic output voltage range		V_{OUT}	V_{SS} – 0.3 to V_{DDL} + 0.3	V
HIGH-level driver output current range	Anode	I_{OHDO}	–5 to 0	mA
	Grid		–15 to 0	mA
LOW-level driver output current range	Anode	I_{OLDO}	0 to 1	mA
	Grid			
Power dissipation		P_D	120 at T_a = 85 °C	mW
			300 at T_a = 70 °C	
Operating temperature range		T_{opr}	–40 to 85	°C
Storage temperature range		T_{stg}	–65 to 150	°C

● Thermal Characteristics

Parameter	Symbol	Rating	Unit
Package thermal resistance	RØ˜$_{\mu A}$	80	°C/W
Package derating coefficient		12.5	mW/°C

● Recommended Operating Conditions

T_a = 25°C, V_{SS} = 0V

Parameter		Symbol	Condition	Rating			Unit
				Min	Typ	Max	
Driver supply voltage		V_{DDH}		30	60	70	V
Logic supply voltage		V_{DDL}		4.5	5.0	5.5	V
Input voltage		V_{IN}		0	—	5.5	V
Input threshold level		V_{LL}		—	1.55	—	V
HIGH-level driver output current	Anode	I_{OHDO}		—	–0.5	—	mA
	Grid			—	–10	—	mA
Clock frequency		f_{clock}		—	—	4	MHz
Clock pulsewidth		t_{wclock}		125	—	—	ns
Setup time		t_{setup}		70	—	—	ns
Hold time		t_{hold}		0	—	—	ns
Latch clock pulsewidth		t_{wlatch}		250	—	—	ns

● DC Characteristics

V_{DDL} = 5V, V_{DDH} = 60V, V_{SS} = 0V, T_a = 25°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level input voltage	V_{IH}		2.4	—	5	V
LOW-level input voltage	V_{IL}		0	—	0.7	V
HIGH-level input current	I_{IH}	V_{IH} = 5.0V	—	—	0.1	µA
LOW-level input current	I_{IL}	V_{IL} = 0V	–100	–33	–10	µA
HIGH-level output current	I_{OHSO}	V_{OH} = 4.6V	—	–1.4	–0.44	mA
LOW-level output current	I_{OLSO}	V_{OL} = 0.4V	0.5	1.5	—	mA
Logic supply current	I_{DDL}	f_{clock} = 4 MHz	—	—	7	mA
Driver supply current	I_{DDH}	All outputs disabled	—	—	0.2	mA
HIGH-level anode driver output current	I_{OHDOA}	V_{OHDO} = 55V	—	—	–2	mA
HIGH-level grid driver output current	I_{OHDOG}		—	—	–10	mA
LOW-level grid and anode driver output current	I_{OLDOA}, I_{OLDOG}	V_{OLDO} = 5V	0.5	1	—	mA
Supply undervoltage detection threshold	V_{LV}		2.0	—	4.0	V

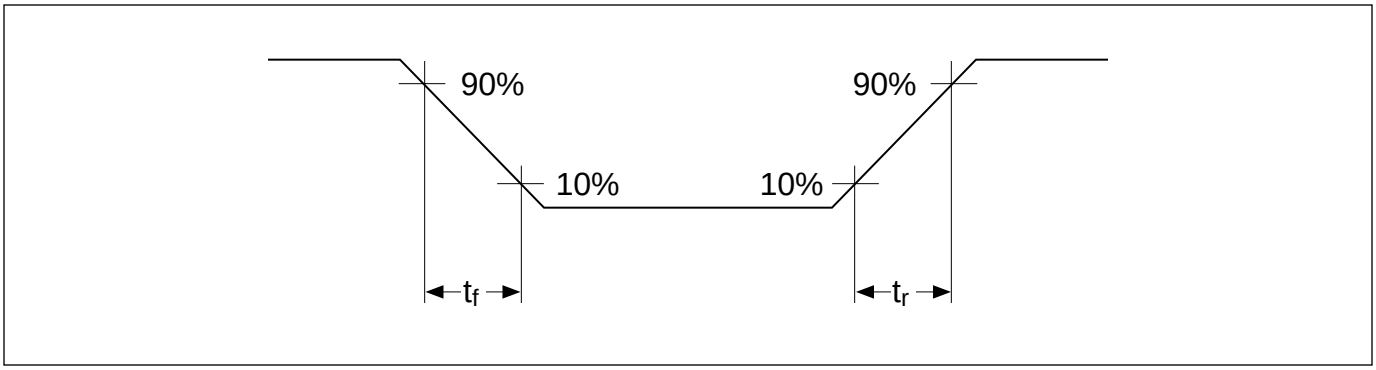
● AC Characteristics

V_{DDL} = 5V, V_{DDH} = 60V, V_{SS} = 0V, Ta = 25°C

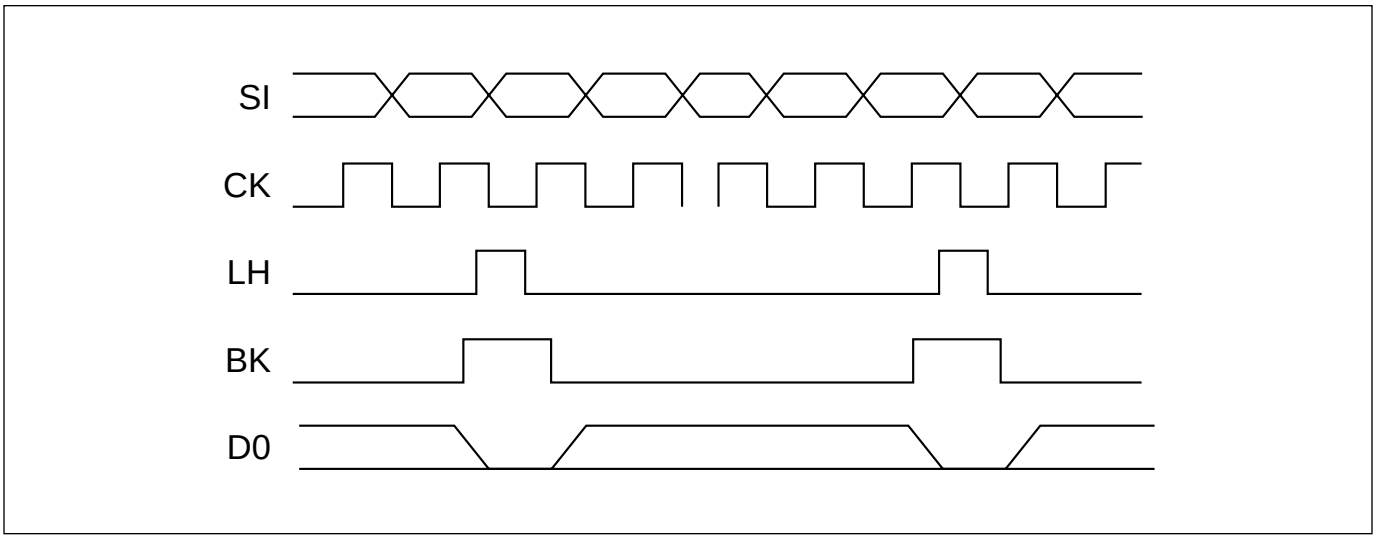
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Latch setup time	t_{CL}		125	—	—	ns
Latch hold time	t_{LC}		0	—	—	ns
Serial output (SO) rise time	t_{rso}		—	—	50	ns
Serial output (SO) fall time	t_{fso}		—	—	50	ns
Logic output clock delay time	t_{pso}		—	—	125	ns
Driver output (DO) rise time	t_{rdo}		—	—	0.5	µs
Driver output (DO) fall time	t_{fdo}		—	—	1	µs
Blanking-to-output propagation delay	t_{pdo}		—	—	2	µs

■ Timing Diagrams

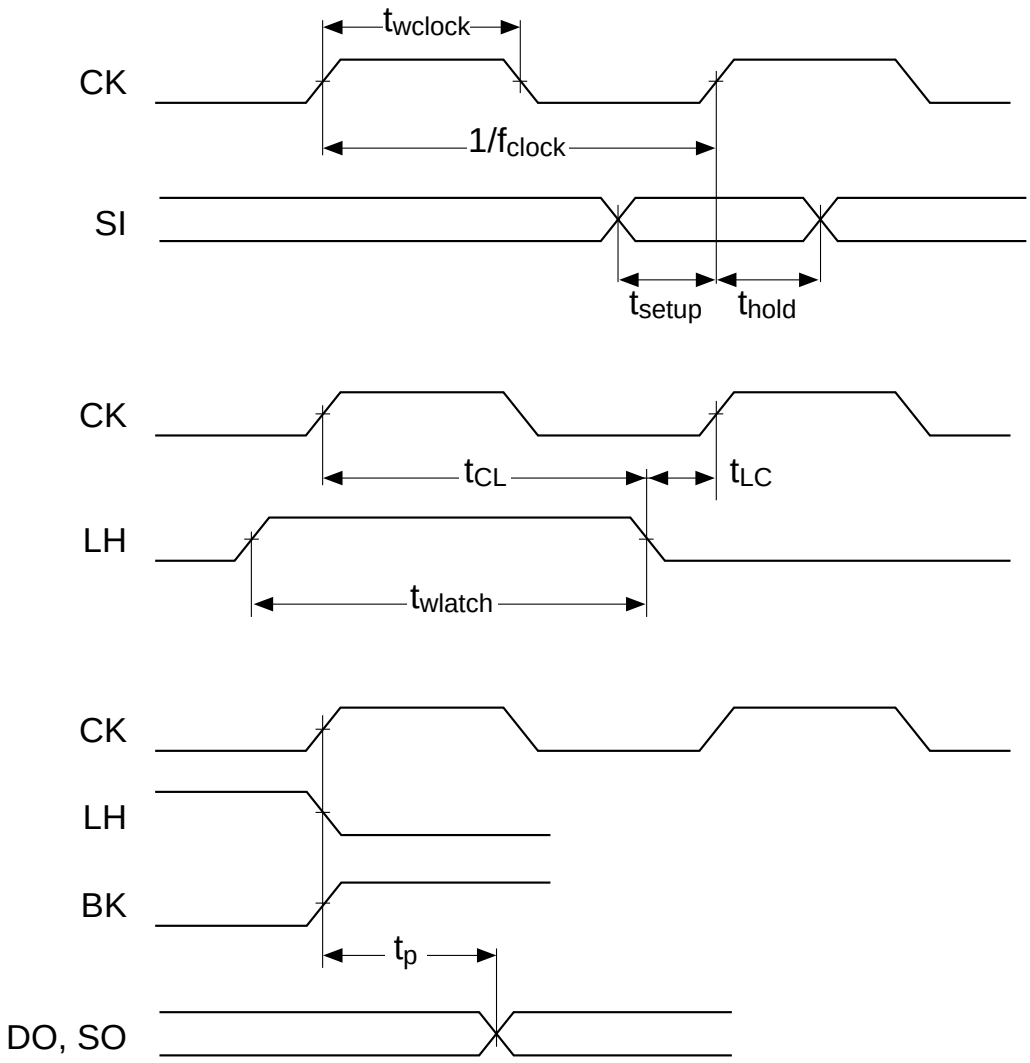
● Rising and Falling Edges



● Input/Output Waveform



● Input/Output Timing



■ Measurement Conditions

- **Inputs**
  - 0 to 5V signal levels
  - 15 ns or less rise and fall times
  - Measured between half logic level intervals
- **Outputs**
  - Standard 13 pF, 10 MΩ load
- **Measured between half logic level intervals**

■ Driver Characteristics

● Anode Driver

Output Current I_{OHDOA} (mA)	Output Voltage Drop V_{OHDOA} (V)
0.25	0.5
0.50	1.0
1.0	1.5
1.5	2.0
2.0	2.5

● Grid Driver

Output Current I_{OHDOG} (mA)	Output Voltage Drop V_{OHDOG} (V)
5	2.5
10	5.0
15	7.5

● Supply Current vs. Clock Frequency

Clock Frequency (MHz)	Supply Current I_{DDL} (mA)
4	7.0
3	5.5
2	4.0

Note: Current consumption can be reduced by disabling the driver outputs using the blanking control input BK, while data is being latched. Latching occurs on the active edge of the clock, while LH is HIGH.

■ Breakdown Testing

● Latchup Immunity

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input trigger current	I_{tIN}	V_{DDL} = 5.0V	±40	—	—	mA
Serial output (SO) trigger current	I_{tSO}	V_{DDL} = 5.0V	±40	—	—	mA
Driver output (DO) trigger current	I_{tDO}	V_{DDL} = 5.0V, V_{DDH} = 60V	–40	—	—	mA

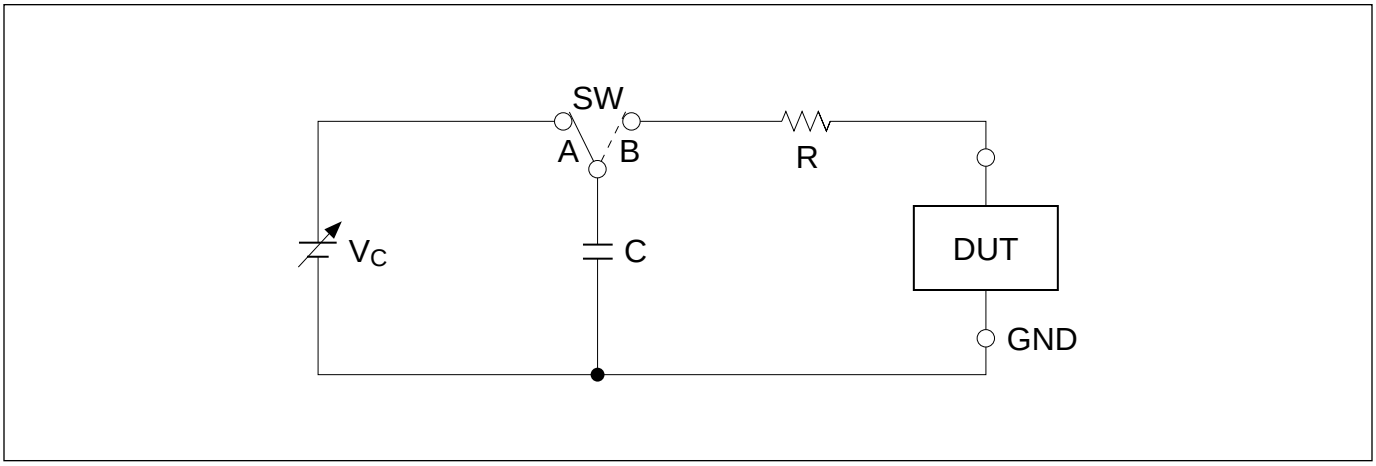
Note: Current should not flow into the driver outputs.

● Static Breakdown Voltage

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input static breakdown voltage	V_{SIN}	C = 100 pF, R = 0 Ω	±300	—	—	V
Serial output (SO) static breakdown voltage	V_{SOUT}	C = 100 pF, R = 0 Ω	±300	—	—	V
Driver output (DO) static breakdown voltage	V_{SDO}	C = 100 pF, R = 0 Ω	±300	—	—	V

■ Measurement Procedure

● Measurement Circuit



● Surge Voltage Application

Set switch SW to position A. After capacitor C has been charged by the Vc supply, set the switch to position B to discharge the capacitor and apply a surge to the device-under-test (DUT).

Increase Vc in steps of 50V, starting from 50V, up to a maximum of 1 kV or until the device fails.

● Static Breakdown Testing

Apply the voltage specified in the absolute maximum ratings to the pin being tested. Measure the leakage current between the pin being tested and VSS or VDDL. If it increases by 10 μA or more, the device has failed.

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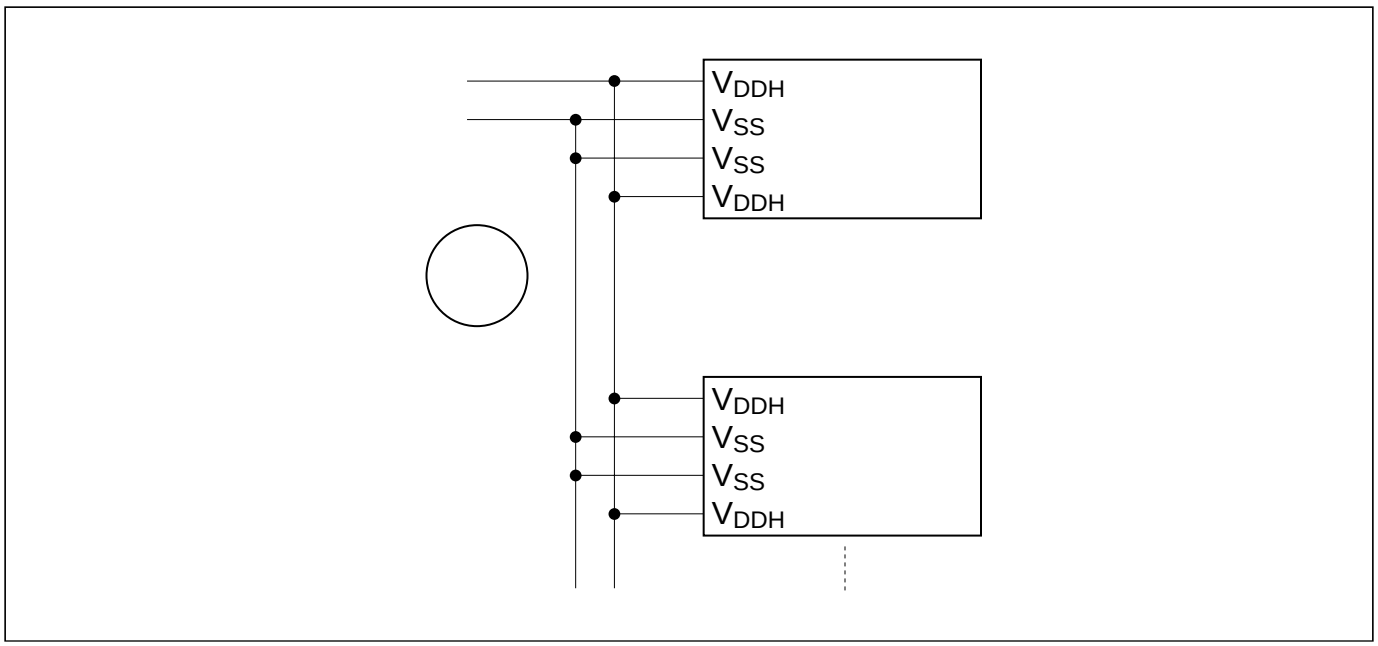
■ Design Notes

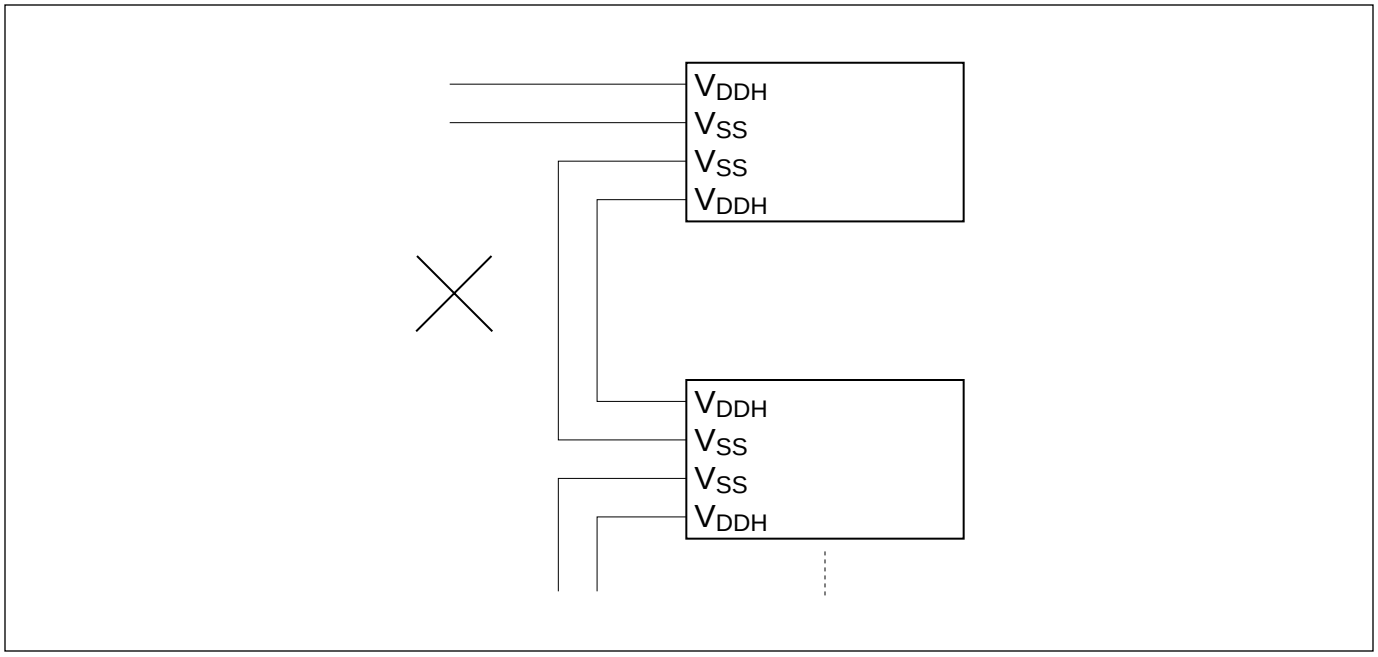
● Supply Connection

The following figures show correct and incorrect supply connections to cascaded devices.

● Correct Supply Connection



● Incorrect Supply Connection



● Power Dissipation Calculation

S-MOS's high-efficiency output driver circuitry ensures low power dissipation. Quiescent current drain is insignificant.

Power dissipation is calculated using the following equation.

$Pd = (V_{DDL} \times I_{DDL}) + (V_{OHDOA} \times I_{OHDOA} \times NA) + (V_{OHDOG} \times I_{OHDOG} \times NG)$

where

- V_{DDL} is the logic supply voltage
- I_{DDL} is the logic supply current
- V_{OHDOA} is the voltage drop across the anode driver output devices
- I_{OHDOA} is the anode driver output current
- NA is the number of anode drivers turned ON
- V_{OHDOG} is the voltage drop across the grid driver output devices
- I_{OHDOG} is the grid driver output current
- NG is the number of grid drivers turned ON

For example, consider a device operating under the following conditions:

$V_{DDL} = 5.5V$, $I_{DDL} = 7$ mA, $f_{CK} = 4$ MHz

$V_{OHDOA} = 1.0V$, $I_{OHDOA} = 0.5$ mA, NA = 40

$V_{OHDOG} = 5.0V$, $I_{OHDOG} = 10$ mA, NG = 1

The power dissipation would be

$Pd = (5.5 \times 7) + (1.0 \times 0.5 \times 40) + (5.0 \times 10 \times 1) = 109$ mW

which is less than the rated value.

(120 mW when Ta = 85°C or 300 mW when Tap = 70°C)

■ Package Dimensions

Unit: inches (mm)