### September 1997

V850 family

#### **Product Letter**



Description	The V851 and V852 are single chip micro- controllers in the 32-bit RISC V850 family from NEC. They integrate CPU, ROM, RAM and peripheral functions on chip. While	the internal bus width is 32-bit, the external bus is 16-bit wide. Different memory options of the controllers are available, see Table 1.
Applications	The applications for V851 / V852 devices are in the field of realtime control, like servo motor control in computer peripherals and machine tool, engine management control,	consumer electronics and multimedia. Low power consumption and power saving modes also make the V851 and V852 perfectly suitable for portable applications.
Features	<ul> <li>Small, 32-bit RISC CPU core</li> <li>16 Mbyte linear address space</li> <li>Min. instruction execution time 30 ns (max. clock 33 MHz)</li> <li>32 general purpose registers</li> <li>74 instructions optimised for embedded control</li> <li>up to 3 Kbyte internal RAM</li> </ul>	<ul> <li>DSP functionality with HW multiplier and saturation logic operating in a single clock cycle</li> <li>Interrupt controller</li> <li>Real-time puls unit/timers</li> <li>Serial interface with baud rate generator</li> <li>Clock generator</li> <li>Power save functions</li> <li>POMers Mark POM OTR versions</li> </ul>

ROMless, Mask-ROM, OTP versions

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RISC by NEC: Know-how<sup>2</sup>

• 100 pin QFP

## Block Diagram V852



# **Functional Block Description**

CPU	The internal CPU is a very compact 32-bit RISC engine. Most instructions are executed in a single clock cycle under control of a 5-stage pipeline. It also includes a hardware multiplier for 16x16-bit with 32-bit and saturation logic to detect and handle overflow/underflow conditions. A 32-bit barrel shifter and bit manipulation instructions accelerate complex bit manipulation to high speed.
Bus Control Unit (BCU)	The BCU initiates the necessary bus cycles based on the physical addresses given by the CPU.
RAM	The internal RAM, with a capacity of 1 Kbyte (V851) or 3 Kbyte (V852), is mapped from address FFFFE000H. The CPU can access any data in one clock cycle.
ROM	The internal ROM / OTP-ROM, with a capacity of 32 Kbyte (V851) or 90 Kbyte (V852), is mapped from address 00000000H. Access to the ROM/PROM is controlled with MODE0 and MODE1 pins. The CPU can access any instruction of the ROM/PROM in one clock cycle.
PROM Programming	The PROMs can be written electrically. To program them, the VPP, MODE0 and MODE1 pins are used. The PROM programming characteristics are compatible with the $\mu$ PD27C1001A products.
Ports	The V851 is equipped with a total of 68 input/output port pins, divided into ports 0 to 10. Alternatively they can be used as control pins.
Interrupt Controller	The interrupt controller handles the various interrupt requests (NMI, INTP00-INTP03, and INTP10-INTP13) issued by internal peripheral hardware or external devices. Up to 8 levels of interrupt priority can be individually specified for each interrupt request.
Clock Generator	The clock generator produces the CPU operating clock. The internal frequency can be selected to be 5x or 1x the crystal frequency by using the internal PLL or 1/2x the crystal frequency without PLL. Instead of using the clock generator, an external clock signal can also be used. A clock-out signal is available.
Real-time Pulse Unit (RPU)/Timers	The RPU includes a 16-bit timer/event counter and a 16-bit interval timer. It can be used to measure puls widths and signal frequencies and to output programmable pulses.
Serial Interface	The serial interface includes one UART (asynchronous serial interface) and one CSI (Clocked Serial Interface) in the V851. The UART transfers the data with TXD and RXD pins at up to 781 kBaud. The on-chip dedicated baud rate generator delivers its baud rate. The CSI transfers data with SO, SI and SCK pins. The baud rate can be determined by the internal dedicated baud rate generator or by an external clock. The V852 offers two additional CSI channels with an additional baud rate generator on chip.

# Differences between V851 and V852

Table 1	Product	Max. freq (MHz)	CSI channels	BRG	RAM	ROM	ROM- less
	V851	33	1	1	1K	32K	yes
	V852	25	3	2	3K	90K	no



## **Ordering Information**

Devices	Part Number		Product Name	Max. freq (MHz)		Internal ROM (Kbyte)	
	μPD703000GC-25-xxx-7EA		V851	25		32 Mask	
	μPD703000GC-33-xxx-7EA		V851	33		32 Mask	
	μPD70P3000GC-25-7EA		V851	25		32 OTP	
	μPD70P3000GC-33-7EA		V851	33		32 OTP	
	μPD703001GC-25-7EA		V851	25		no	
	µPD703001GC-33-7EA		V851	33		no	
	µPD703002GC-25-xxx-7EA		V852	25		90 Mask	
	μPD70P300GC-25-7EA		V852	25 90 OTH		90 OTP	
	Note: "xxx" is ROM code number						
Documentation	Doc Number	Device	Device		Туре		
	U10988E	μPD70	)P3000 Data		a Sheet		
	U10987E	μPD70	D3000 Data Sheet		Sheet	et	
	U10935E	V851	U		Jser's Manual		
	U11826E	µPD7(	03002 E		Data Sheet		
	U10038E	V852	User's Manual		d		
	U10243E	V850	Family Architecture Manual		Manual		
SW Tools	Order Number		Description		Platform		
	CPDHP-ODAT-V800		C/C++Compiler		HP		
	CPDW95/NT-ICDR-V800		and Tools Win95/Win		Win NT		
	Note: Tools include Linker, Librarian, Assembler, Debugger, Simulator,						
	ICE interface software, and MULTI environment.						
			1				
HW Tools	Order Number		Description				
	EB-V853STARTER		Starter Kit for all V850 controllers				
	IE-703002-MC		Emulator				
	IE-70000-MC-PS-B		Power Supply				
	IE-70000-PC-IF-B		PC Interface Card				
	IE-70000-MC-SV3		Ethernet Adapter				
	SC100SD		Emulation Probe				
	PA-70P3000GC		Programming Adapter				



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