Embedded Computing for
Business-Critical Continuity™

MITX-CORE-820

Installation and Use

P/N: 6806800M10D

August 2011

EMERSON
Network Power

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices.

- *Introduction* describes the features of the MITX-CORE-820 processors, standard compliances, mechanical data and ordering information.
- *Hardware Preparation and Installation* describes the environmental and power requirements, installation prerequisites, processor cooler and memory module installation and removal procedures.
- *Controls, LEDs and Connectors* describes the LEDs and connectors used on the motherboard.
- *Functional Description* describes the functionalities provided on the motherboard.
- *Firmware* describes the motherboard's firmware.
- *Replacing the Battery* contains the procedures for replacing the battery.
- *Related Documentation* provides a listing of related product documentation, manufacturer's documents, and industry standard specifications.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
A	Amps
A/D	Analog/Digital
AMT	Active Management Technology
ANSI	American National Standard Institute
BGA	Ball Grid Array
COM	Communications
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
oC	Degrees Celsius

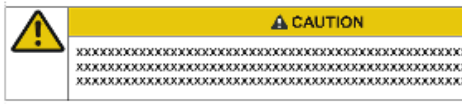
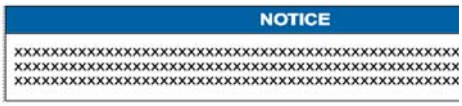
Abbreviation	Definition
DMA	Direct Memory Access
DMC	Display Mini Card
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPROM	Erasable Programmable Read-Only Memory
FCC	Federal Communications Commission
F/W	Firmware
FPBGA	Flip Chip Plastic Ball Grid Array
GB	GigaBytes
GbE	Gigabit Ethernet
Gbit	Gigabit
Gbps	Gigabits Per Second
GLCI	Gigabit LAN Connect Interface
H/W	Hardware
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
I2C	Inter IC
JTAG	Joint Test Access Group
KB	Kilo Bytes
KBAUD	Kilo Baud
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signaling
MB	MegaBytes
Mbit	Megabit
Mbps	Megabits Per Second

Abbreviation	Definition
MHz	Megahertz
MTBF	Mean Time Between Failure
OS	Operating System
PBGA	Plastic Ball Grid Array
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
POR	Power-On Reset
PRD	Product Requirements Document
RAM	Random Access Memory
Rcv	Receive
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial AT Attachment
SDRAM	Synchronous Dynamic Random Access Memory
SMT	Surface Mount Technology
SODIMM	Small-Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
S/W	Software
USB	Universal Serial Bus
V	Volts
VIO	Input/Output Voltage
W	Watts
XDP	Extended Debug Port

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR

Notation	Description
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800M10D	August 2011	• Updated marketing name to MITX-CORE-820 • Updated Table "MITX-CORE-820 Features Summary" on page 17 • Updated Table "Environmental Requirements" on page 25 • Updated Table "Power Dissipation of Critical Components" on page 26 • Updated Figure "MITX-CORE-820 Module Component" on page 33 • Updated Table "DC-IN Jack Pin Definitions" on page 48 • Updated Table "ATX Power Supply Connector (J12)" on page 48 • Updated Table "Board MAX Power Consumption Estimation" on page 49
6806800M10C	July 2011	Updated Figure "MITX-CORE-820 Module Component" on page 33. Added information on the board CPU specs.
6806800M10B	May 2011	Changed marketing name to MITX-CORE-810/820. Implemented editorial changes.
6806800M10A	May 2011	First edition

Introduction

1.1 Overview

MITX-CORE-820 is an Emerson designed Mini-ITX motherboard based on Intel® 6 Series Chipset supporting Intel® Sandy Bridge Mobile rPGA Quad/Dual core processors.

1.2 Features

The following table lists the features of the MITX-CORE-820 motherboard.

Table 1-1 MITX-CORE-820 Features Summary

Function	Features
CPU (rPGA988B Socket)	● Supports one 45 W 4-core Core i7 Intel Sandy Bridge-Mobile rPGA 988B embedded processor. ● Intel AMT 7.0, Turbo Boost ● Also provides the option to support one 35 W 2-core Core i5 Celeron Intel Sandy Bridge-Mobile PGA embedded processor.
Chipset	Intel 6 Series PCH
Memory Feature	● Supports up to 16GB dual-channel, non-ECC, unbuffered DDR3 SO-DIMM ● Up to 1600 MT/s
Embedded Controller	Nuvoton NPCE791C
Audio	● Audio on board (ALC888S-VC) ● Rear Panel: 5 audio jacks + 1 SPDIF output, Front Panel: 2 re-tasking audio jacks, 2nd SPDIF output header (optional)
LAN	Intel WG82579LM, Intel WG82574L
USB	High-speed Enhanced Host Controller interfaces (EHCI) that supports 12 ports(4 rear/6 on header (one header can be used as eUSB connector) /1 PCIe Mini Card/1 Display Mini PCIe Card)
Expansion slots	1x PCIe 16x Slot Supports Gen 2
Rear panel ports	4 USB2.0 ports, 2 Display Port, Audio Jack, DC-In Jack, 2 RJ-45 Ports (one for MITX-CORE-810), VGA/COM Port
Power Connectors	12 V or 14.4-19.5 V DC-IN Jack / 4-pin ATX_12V connector. Only one can be plugged at a time

Table 1-1 MITX-CORE-820 Features Summary (continued)

Function	Features
Board size	• Mini-ITX 170 mm x 170 mm form factor • 10 Layers PCB
Serial ATA	2 SATA 6G ports and 2 SATA 3G ports
EC/Thermal Sensor	Voltage, temperature and fan speed control
Trusted Platform Module	Connector Reserved
PCIe Mini Card/Display Mini Card	Dual head-to-head sockets, one full card or one half card/ one half card or one half card/ one DMC card supported
eUSB	Standard eUSB header on board
Graphics	Internal graphics: CRT, Dual-Mode display port, embedded DP, single/dual channel 24-bit/18bit LVDS, DMC External graphics: PEG 16X supports Gen 2
Smart Charger/Battery Interface	7-pin header interface for Smart Charger/Battery. Battery must have enough power capacity. Output voltage is higher than 11.4 V.
PS/2 - PS/2 Keyboard and Mouse Connector	

Table 1-1 MITX-CORE-820 Features Summary (continued)

Function	Features
Industrial Standard	● ACPI 4.0a ● PCI Express Gen2 ● SMbus Version2.0 ● Universal Host Controller Interface Revision1.1(UHCI) ● Enhanced host Controller Interface specification for Universal Serial bus Revision1.0(EHCI) ● Serial ATA specification revision 3.0 ● Serial ATA II: extensions to SATA1.0 revision1.0 ● Serial ATA 6G specification ● VESA Specification ● SMBIOS 2.3 ● ACPI Wake-up event: – Power Button: S0, S3, S4, S5, Deep Sx – KB: S0, S3 – Mouse: S0, S3 – PME: S0, S3, S4, S5, Deep Sx – USB: S0, S3 – RTC: S0, S3, S4, S5 ● Wake on LAN support ● DMI support

1.3 Standard Compliances

This product is designed to meet the following standards.

Table 1-2 Board Standard Compliances

Standard	Description
IEC 60950-1	General requirements of Safety-Part 1 of Information Technology Equipment.
EN55024 (EU)	Limits and methods of measurements of immunity characteristics of Information Technology Equipment.

Table 1-2 Board Standard Compliances

Standard	Description
FCC 47 CFR Part 15 Subpart B (US), Class B	Federal Communications Commission Radio Frequency Devices class B level requirements.
EN55022 Class B (EU)	Limits and methods of measurements of radio disturbance characteristics of Information Technology Equipment.
AS/NZS CISPR 22 Class B (Australia/New Zealand)	Limits and methods of measurement of radio disturbance characteristics of Information Technology Equipment.
VCCI Class B (Japan)	Voluntary Control Council for Interference by Information Technology Equipment.

1.4 Mechanical Specifications

Figure 1-1 MITX-CORE-820 Mechanical Data (Top View)

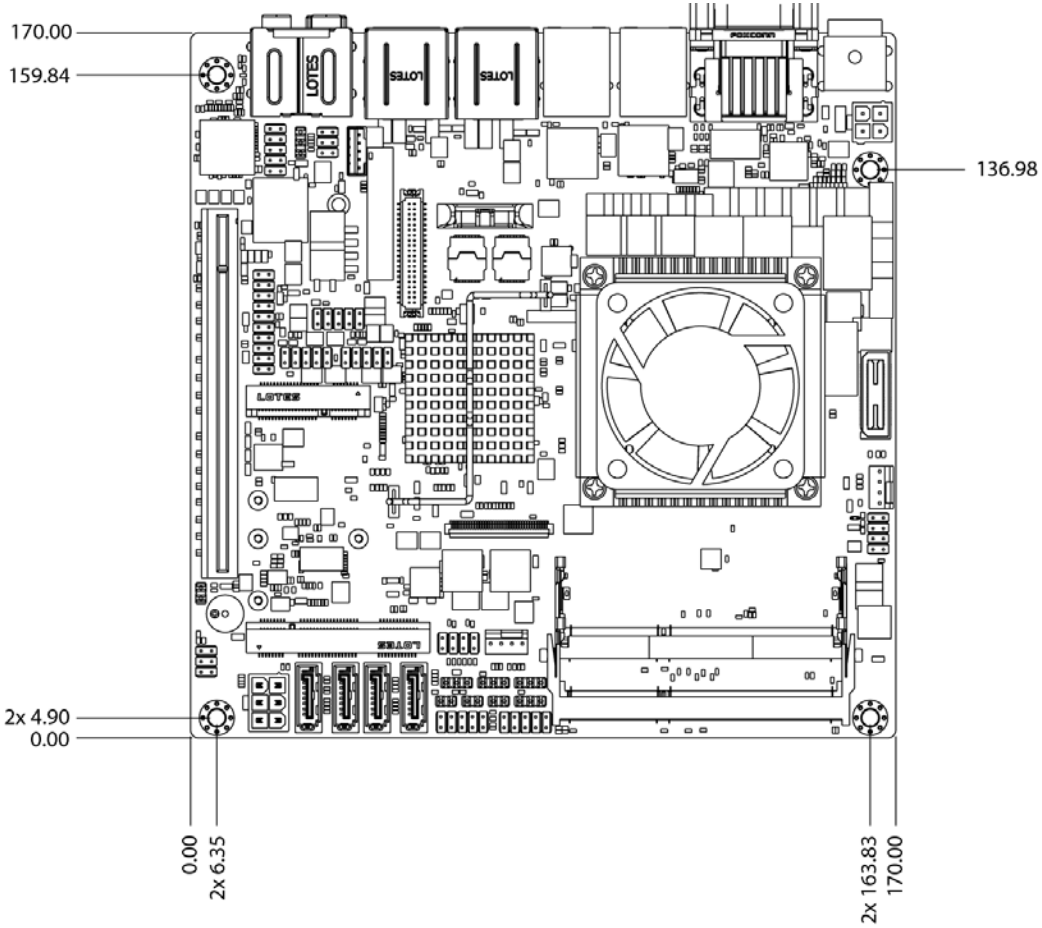
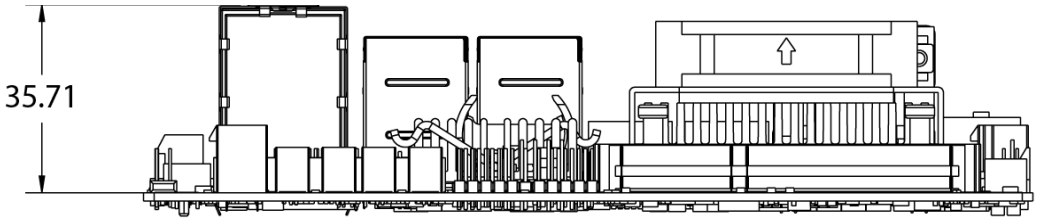


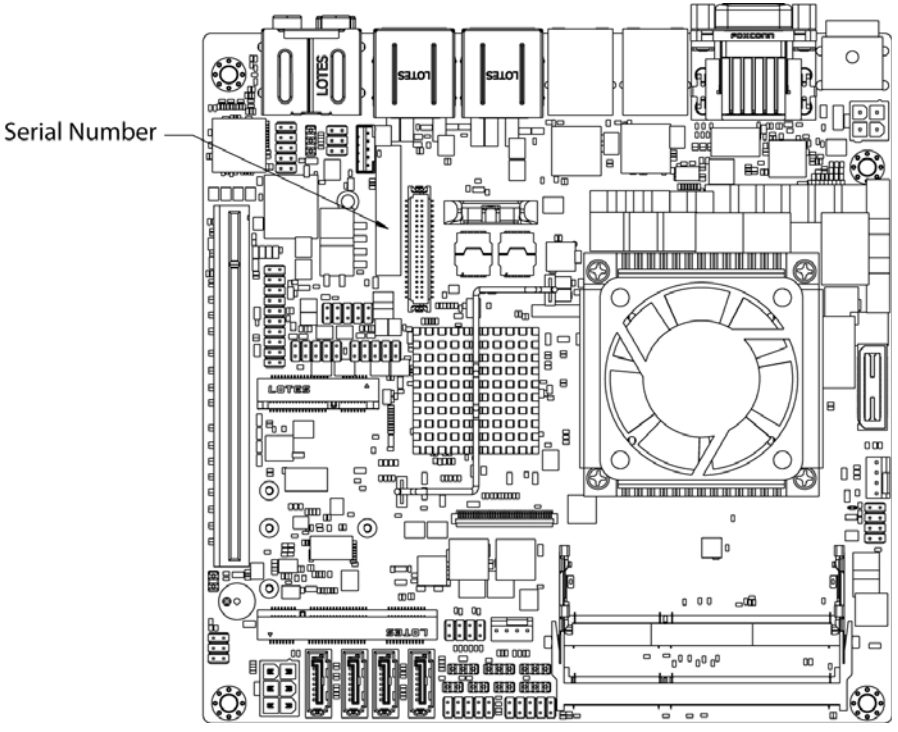
Figure 1-2 MITX-CORE-820 Mechanical Data (Side View)



1.5 Board Identification

This section shows the serial number and its location on the board.

Figure 1-3 MITX-CORE-820 Serial Number Location



1.6 Ordering Information

Use the following order numbers when ordering board variants or board accessories.

The MITX-CORE-820 does not come installed with a CPU or processor cooler/heat sink. To order the processor, please contact Intel© customer support for the ordering information.

Table 1-3 Ordering Information

Ordering Number	Description
0106848J01C	MITX-CORE-820
0106848J62A	MCASE-820
MITX-CORE-HTSNK	MITX-CORE Heatsink

2.1 Environmental and Power Requirements

The following environmental and power requirements are applicable to the MITX-CORE-820.

2.1.1 Environmental Requirements

The following table lists the environmental requirements that the board must meet when operated in your particular system configuration.

Operating temperatures refer to the temperature of the air circulating around the motherboard and not to the component temperature.

NOTICE

Product Damage

- High humidity and condensation on surfaces cause short circuits.
- Do not operate the product outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Overheating and Damage of the Product

- Operating the product without forced air cooling can lead to overheating and thus damage of the product.
- When operating the product, make sure that forced air cooling is available in the shelf.

Table 2-1 Environmental Requirements

Parameter	Operating	Non-Operating
Cooling Method	Forced air	
Temp Cycle Class	-	-40°C to 85°C:500 cyc

Table 2-1 Environmental Requirements (continued)

Parameter	Operating	Non-Operating
Temperature	0°C to 55 °C	-40°C to 85°C
Humidity	10 to 90% Non-condensing	-
Vibration	0.01g^2/Hz at 5-500 Hz Random vibration	-
Shock	20 g 11 ms sine or saw	-
Altitude	-60 to 4000 m ASL	-

2.1.2 Power Requirements

The MITX-CORE-820 is designed to receive power from an input power connector that accepts +12V or +14.4V~+19.5V in the back-panel IO region, or from a 4-pin +12V ATX power connector. When a charger board is used, the power can be supplied using a 4-pin +12 V ATX power connector from the adapter or battery connected to charger board. The TDP of the board is 70W (no peripheral). The maximum power consumption of the board is 180W (with the following assumptions: 75W PCI Express Graphics card, all of the USB ports are active or powered, all components and peripherals on the boards are running at full loading). The power supply used for MITX-CORE-820 should have margin to meet the power consumption in different circumstance.

When the back-panel IO power connector is used to power the board, the 4-pin +12V ATX power connector can also be used as an output DC source, but assuming this wouldn't affect the power of the board.

2.1.3 Power Dissipation

The following table shows the power dissipation of the board's critical components.

Table 2-2 Power Dissipation of Critical Components

Part	TDP (W)	Operation Limit (C)
CPU	Maximum: 45	Tj=100
Chipset	3.9	Tj=108

Table 2-2 Power Dissipation of Critical Components

Part	TDP (W)	Operation Limit (C)
SODIMM	5W (Two SODIMMs)	Tc=85
WG82574L	0.473W	Tc=109
WG82579LM	0.659W	Tc=106

2.2 Unpacking and Inspecting the Board

Read all notices and cautions prior to unpacking the product.

NOTICE

Damage of Circuits

- **Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten its life.**
- **Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.**

Shipment Inspection

1. Verify that you have received all items of your shipment.
   - Quick Start Guide and Safety Notes summary
   - Motherboard
   - Two SATA power Cables
   - Two SATA data cables
   - Driver CD
   - I/O Shield

2. Check for damage and report any damage or difference to customer service.
3. Remove the desiccant bag shipped together with the board and dispose of it according to your country's legislation.

NOTICE

Environmental Damage

- Improper disposal of used products may harm the environment.
- Always dispose of used products according to your country's legislation and manufacturer's instructions.

This product has been thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, contact customer service immediately.

2.3 Preparing the Installation Environment

Before you install or replace components, pay attention to the following:

- Wear an ESD-preventive wrist strap to prevent the static electricity from damaging the device.
- Keep the area where the components reside clean and keep the components away from heat-generating devices, such as radiator.
- Ensure that your sleeves are tightened or rolled up above the elbow. For safety purposes, it is not recommended to wear jewelry, watch, glasses with metal frame, or clothes with metal buttons.
- Do not exert too much force, or insert or remove the components forcibly. Avoid damage to the components or plug-ins.
- Confirm the feasibility of the of operation

There are available spare parts of the components to be installed or replaced in the equipment warehouse. When the available spare parts are lacking, contact Emerson Network Power for help in time. For details on how to get help from Emerson Network Power, visit http://www.emersonnetworkpower.com/embeddedcomputing

Make sure that the new components are in good condition, without defects such as oxidation, chemical corrosion, missing components, or transportation damage. Read this document to familiarize yourself with the proper installtion and replacement procedures of the component, as well as to master the skills required by the operation.

- **Check the environment**
  Make sure that the power supply, temperature, and humidity meet the operating requirements for the board and its components. For details, refer to the respective system documentation.
- **Prepare the parts and the tools**
  Prepare the components to be installed or replaced. When you hold or transport the components, use the special antistatic package. Prepare the cross screwdriver, screws, plastic supports, cooling gel, and ESD-preventive wrist strap.
- **Confirm installation or changing position**
  Confirm the position where MITX-CORE-820 will be installed.
- If a serious problem occurs and cannot be solved when you install or replace the component, contact Emerson Network Power for technical support.

2.4 Memory Module Installation

When installing or replacing the module, pay attention to the following:

- The MITX-CORE-820 supports up to 16GB dual-channel, non-ECC, unbuffered DDR3 SO-DIMM.
- The SO-DIMMs must have the same sizes, frequencies, types and technologies, physical designs, and manufacturers.
- SO-DIMMs must be of single or dual rank type. Quad rank type modules are not supported.

NOTICE

Pin Damage

- **Forcing the module into the system may damage connector pins. If the module freezes during insertion, pull it out and try again.**

Installing Memory Module

1. Wear the ESD-preventive wrist strap.
2. Lay the MITX-CORE-820, where the SO-DIMM is to be installed, on the antistatic desktop.
3. Take the SO-DIMM out of the antistatic package, holding it by the edges.
4. Line up the notch located on the row of the metal pins at the bottom of the module with the key in the SO-DIMM slot on the motherboard.
5. Insert the SO-DIMM in a slantwise position or at a 45° angle to slide the module into place.
6. Press the module down against the motherboard until you hear it snap into place. The modules must be properly aligned before you press it down into its final position. Remove the module from the socket and reinstall it if you cannot press it down into its final position.

Removing Memory Module

1. Wear the ESD-preventive wrist strap.
2. Release the module from the slot by pushing the spring latches on either side of the module outward.
3. Lift the module from the motherboard.

NOTICE

Damage of the Product and Additional Devices and Modules

- **Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.**
- **Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.**

2.5 Processor Cooler Installation

Installing the Processor Cooler

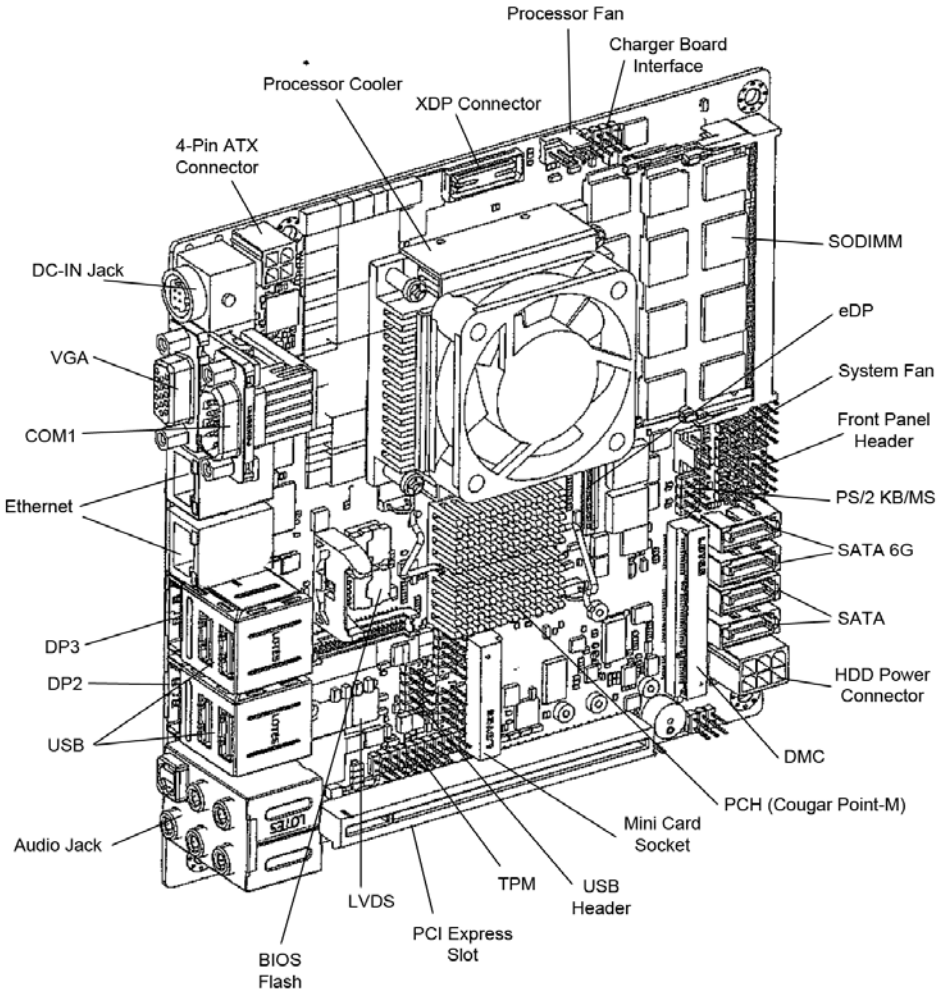
1. Wear the ESD-preventive wrist strap.
2. Take the processor cooler and the backplate out of the anti-static package.
3. Prepare the backplate by taking off the protective film to reveal the glue layer.
4. Align the backplate to the motherboard. The screw holes on backplate should fit exactly over the holes on the motherboard. Make sure the glue layer of the backplate does not touch any other part of the motherboard.
5. Place the cooler on the backplate and secure it with the provided screws.
6. Plug the fan header into the fan connector on the motherboard.

Removing the Processor Cooler

1. Wear the ESD-preventive wrist strap.
2. Disconnect the fan header from the fan connector on the motherboard.
3. Loosen the screws to remove the processor cooler from the backplate.

3.1 Board Layout

Figure 3-1 MITX-CORE-820 Module Component



3.2 Connector Definitions

The following table lists the connectors and headers located on the MITX-CORE-820 motherboard along with a link to each connector's associated pin out definition document. Connectors or headers are defined in the following sections.

Table 3-1 MITX-CORE-820 Connectors

Reference Designator	Function	Pinout Definition
P6	LVDS Connector	See *LVDS, on page 41*
P29	LVDS Panel VDD Selector	See *LVDS, on page 41*
P8	LVDS Inverter Connector	See *LVDS, on page 41*
P9	Front Panel Audio Header	See *Audio, on page 54*
P30	S/PDIF Out Header	See *Audio, on page 54*
P3	TPM/Port80 Header	See *TPM/Port 80 Interface, on page 58*
P24	USB Internal Header	See *USB 2.0, on page 47*
P25	USB/eUSB Header	See *USB 2.0, on page 47*
P26	USB Header	See *USB 2.0, on page 47*
P14	EC Debug Header	See *Debug Header, on page 52*
P17	SATA HDD Power Header	See *Storage, on page 46*
P5	PS/2 Header	See *PS/2, on page 51*
P2	System Fan Header	See *Fan Header, on page 51*
P18	Wake UP Header	See *Wake Events, on page 61*
P4	Clear CMOS Header	See *RTC Circuit, on page 56*
P31	Charge LED 1	See *On Board LED Interface, on page 59*
P34	Charge LED 2	See *On Board LED Interface, on page 59*
P27	Case Open Header	See *Case Open Header, on page 59*
P33	Internal Graphics Disable	See *Internal Graphics Disable, on page 60*
P1	Front Panel Header	See *User GPIO Header, on page 60*
P28	User GPIO Header	See *User GPIO Header, on page 60*
P22	Charge Board Interface	See *Charge Board Interface, on page 52*

Table 3-1 MITX-CORE-820 Connectors (continued)

Reference Designator	Function	Pinout Definition
P23	CPU Fan Header	See *Fan Header, on page 51*
J15	eDP Connector	See *Embedded Display Port (eDP), on page 43*
J11	Audio Jack	See *Audio, on page 54*
J13	DC-IN Jack	See *Power Supplies, on page 48*
J12	ATX Power Supply Connector	See *Power Supplies, on page 48*

3.3 LED Controls

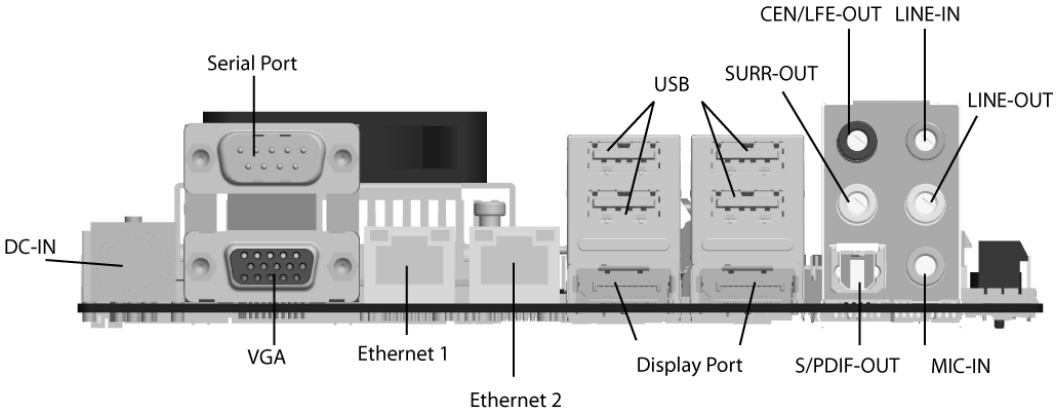
The MITX-CORE-820 has one green LED and one red LED to indicate the charging and discharging status.

Table 3-2 LED Control Indicator

Battery Status	Green LED Status	Red LED Status
Charging	Inactive	Active
Fully Charged	Active	Inactive
Discharging	Inactive	Inactive
Battery Low	Inactive	Blinking

3.4 Rear I/O Connectors

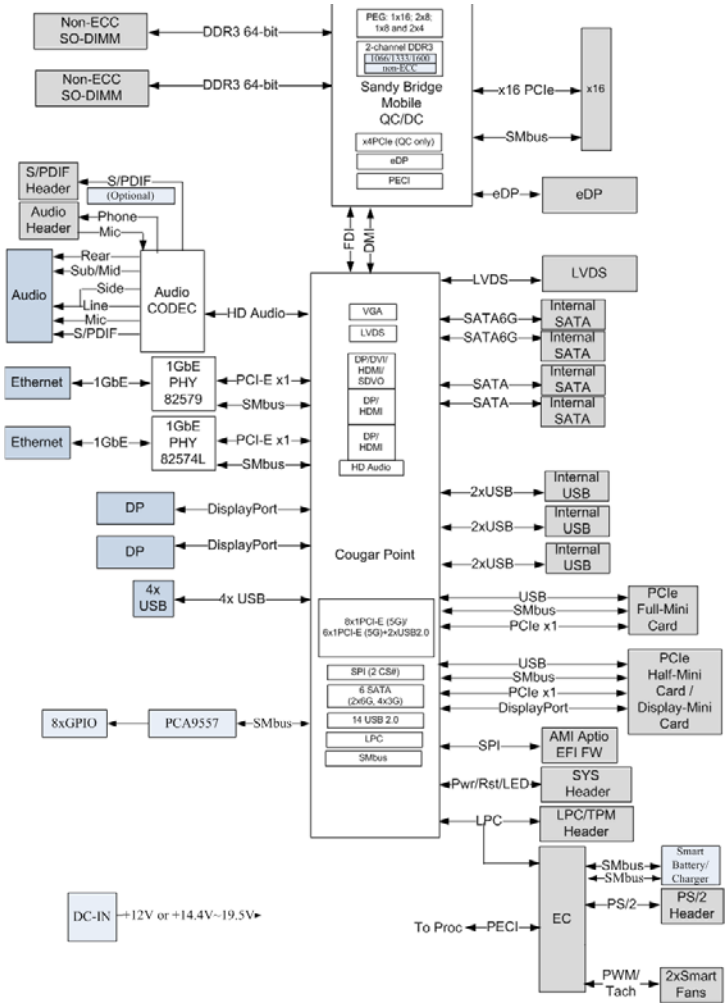
Figure 3-2 Rear I/O Connectors



4.1 Block Diagram

This engineering specification defines a standard Mini-ITX motherboard. The board supports a single DC-Jack or ATX 4-pin power input and smart battery power input. The board communicates with a charger board with the smart battery input through a header on the motherboard.

Figure 4-1 Block Diagram



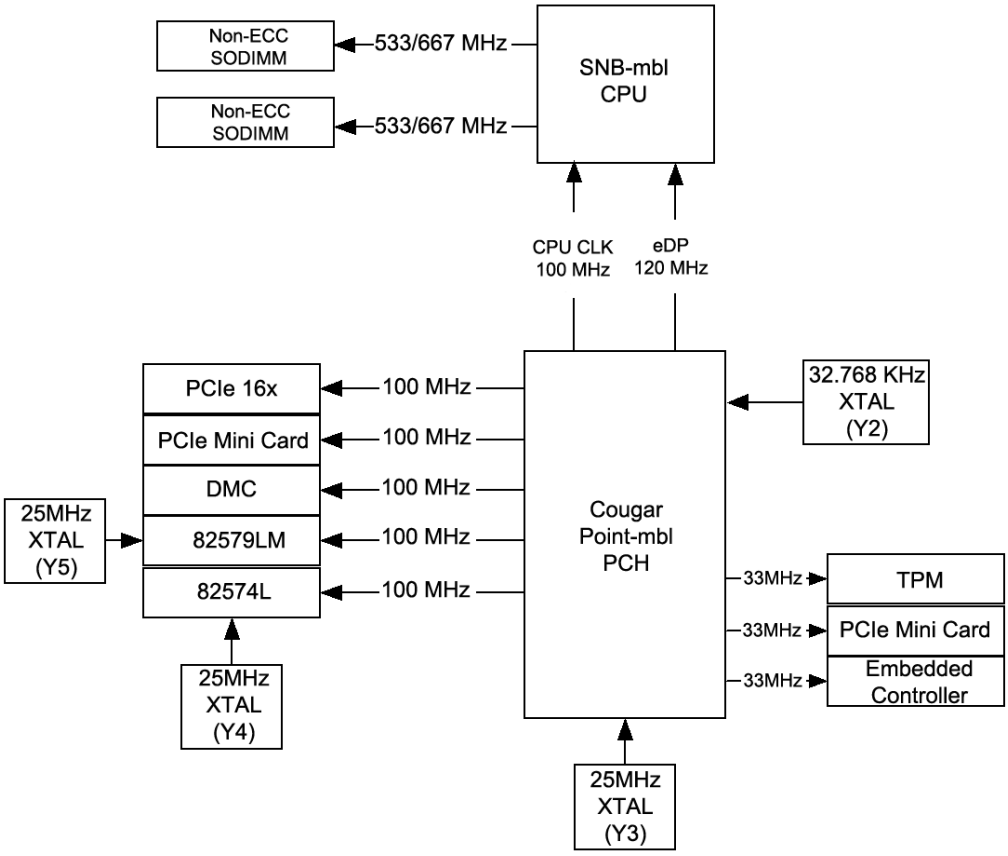
4.2 Processor

The board supports one 45 W 4-core Core i7 Intel Sandy Bridge-Mobile rPGA 988B embedded processor. The board also provides the option to support one 35 W 2-core Core i5 Celeron Intel Sandy Bridge-Mobile PGA Embedded processor.

4.3 Motherboard Clock Diagram

The MITX-CORE-820 implements full integrated clocking mode as the only platform clock solution.

Figure 4-2 Platform Clocks Distribution



4.4 Chipset

Mobile Intel 6 series PCH is used on the board. The board can support QM67 with Core i3, i5 and i7 processors. It can also support the low end version HM65 with Celeron SKU.

Table 4-1 PCH SKUs

Feature Set		SKU Name				
		QM67	UM67	HM67	HM65	QS67
PCI Express 2.0 Ports		8	8	8	8	8
PCI Interface		No	No	No	No	No
USB 2.0 Ports		14	14	14	12[5]	14
Total number of SATA Ports ● SATA Ports (6 Gb/s, 3 Gb/s and 1.5 Gb/s ● SATA Ports (3 Gb/s and 1.5 Gb/s only)		6 2[4] 4	6 2[4] 4	6 2[4] 4	6 2[4] 4	6 2[4] 4
HDMI/DVI/VGA/SDVO/Display Port/eDP/LVDS		Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support with PAVP 2.0		Yes	Yes	Yes	Yes	Yes
Intel © Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	Raid 0/1/5/10 Support	Yes	No	Yes	No	Yes
Intel © Anti-Theft		Yes	Yes	Yes	Yes	Yes
Intel © AMT 7.0		Yes	No	No	No	Yes
Intel © Remote PC Assist Technology - Proactive		Yes	Yes	Yes	No	Yes
Intel © Remote PC Assist Technology - Reactive		Yes	Yes	Yes	Yes	Yes

4.5 System Memory

The MITX-CORE-820 supports one DDR3 1066MT/s/1333MT/s/1600MT/s SODIMM per channel, for a total of 2 DDR3 SODIMMs. Maximum memory capacity is 16 GB (8 GB per SODIMM) using 2 GB technology. Minimum capacity is a single 1 GB SODIMM using 1 GB technology.

4.6 Video

The MITX-CORE-820 supports dual-independent displays using the Mobile Intel® 6 Series Chipset Integrated Graphics Controller. The primary display shall be LVDS (eDP) or VGA, and the secondary display shall be Display Port. During boot, the BIOS will detect if a VGA monitor is attached. If VGA is attached, then the primary display shall be VGA. If VGA is not detected, then BIOS shall default to LVDS or eDP. eDP and LVDS cannot be used at the same time.

4.6.1 LVDS

The MITX-CORE-820 supports dual-channel LVDS on pipe A of the Integrated Graphics Controller. The Intel 6 Series chipset supports up to 24-bit color per pixel, so the design can support both 18-bit and 24-bit LCD panels utilizing different cables.

Table 4-2 LVDS Connector (P6)

Pin	Signal	Pin	Signal
1	LVDSA_DATA0	2	LVDSB_DATA0
3	LVDSA_DATA0#	4	LVDSB_DATA0#
7	LVDSA_DATA1	8	LVDSB_DATA1
9	LVDSA_DATA1#	10	LVDSB_DATA1#
13	LVDSA_DATA2	14	LVDSB_DATA2
15	LVDSA_DATA2#	16	LVDSB_DATA2#
19	LVDSA_DATA3	20	LVDSB_DATA3
21	LVDSA_DATA3#	22	LVDSB_DATA3#
25	LVDSA_CLK	26	LVDSB_CLK
27	LVDSA_CLK#	28	LVDSB_CLK#
31	LVDS_DDC_CLK	32	LVDS_DDC_DATA
33,35,37,39	+VDD_LVDS	36,38,40	+VDD_LVDS
5, 11,17,23,29	GND	6,12,18, 24,30,34	GND

The design implements a separate LVDS and Backlight Inverter connectors located on the board. The connectors follow the common parts used on Emerson products.

Table 4-3 LVDS Panel VDD Selector (P29)

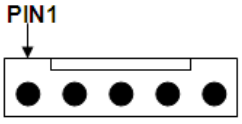
Jumper setting (Jumper:P29)	Configuration
P29 (2-4)	+3.3 V (Default)
P29 (3-4)	+12 V
P29 (6-4)	+5 V

A jumper on the board is used to select power supply for LVDS monitor. +3.3 V is the default, while +5 V or +12 V are other options. +12 V and +5 V can be used to power the inverter, with +12 V as default.

Table 4-4 LVDS Inverter Connector (P8)

Pin	Signal
1	+V12S
2	L_BKLT_EN
3	GND
4	L_BKLT_CTRL
5	+V5S

Figure 4-3 LVDS Inverter Connector (P8)



4.6.2 VGA

The design implements a VGA connector on the board edge.

4.6.3 Display Port

There are two display ports (DP) on the rear IO. It follows the DP specifications V1.1 and has the ability to support dual-mode DP. An HDMI monitor can be connected to the DP port using a DP-to-HDMI adapter. There is also a dedicated DP port to DMC slot.

4.6.4 Embedded Display Port (eDP)

The product provides a eDP interface which can connect to a Flat-Panel Display (FPD) with 30-pin/40-pin eDP connector for LED backlight with LED Driver on PCB for the Embedded Display Port Spec v1.1. The interface can support 1, 2 or 4 lanes eDP with up to 2.7 Gb/s per lane.

Table 4-5 eDP Connector (J15)

Pin#	Signal Name	Pin#	Signal Name
1	VDD_LVDS	21	DP_TXN0
2	VDD_LVDS	22	DP_TXP0
3	VDD_LVDS	23	GND
4	VDD_LVDS	24	EMB_AUXP
5	VDD_LVDS	25	EMB_AUXN
6	GND	26	GND
7	GND	27	V3.3S
8	GND	28	V12S
9	GND	29	GND
10	EMB_HPD	30	GND
11	GND	31	V5S
12	DP_TXN3	32	V5S
13	DP_TXP3	33	L_BKLT_CTRL
14	GND	34	L_BKLT_EN
15	DP_TXN2	35	V12S
16	DP_TXP2	36	V3.3S
17	GND	37	GND

Table 4-5 eDP Connector (J15) (continued)

Pin#	Signal Name	Pin#	Signal Name
18	DP_TXN1	38	SMB_THRM_CLK
19	DP_TXP1	39	SMB_THRM_DATA
20	GND	40	GND

4.7 PCI Express

The MITX-CORE-820 has one x16 5G PCI-Express slot which supports graphics cards up to 75 W in power. The position of the PCI-Express slot follows the Mini-ITX Addendum Version 1.1 of the microATX Motherboard Interface Specification Version 1.2.

The Cougar Point-mbl PCH has one x1 PCI-Express port (port 6) to the WG82579LM and one x1 PCI-Express port (port 3) to the WG82574L. Port 7 will be used for a PCI-Express Mini Card connector for WiFi/WiMAX, port 8 is used for DMC card slot.

4.8 LAN on Motherboard

The MITX-CORE-820 provides two GbE ports. One port uses the Intel 6 Series PCH integrated MAC and the Intel WG82579LM GbE PHY. The Intel WG82579LM is connected to PCH through the 1x PCI-Express. The other Gbe port uses Intel WG82574L controller (MITX-CORE-820 only). The design provides two RJ-45 connectors supporting 10/100/1000 Base T. LAN is powered by suspend well to support AMT and wake-on-LAN while in S5. WG82579LM uses +V3.3 M and WG82574L uses +V3.3 A.

LAN connector has two integrated LEDs.

- A single green LED
  - OFF (no light) - LAN link is not established
  - ON (steady light) - LAN link is established
  - Blinking - indicates LAN link activity

- Dual color green and yellow LED
  - OFF (no light) - indicates 10 Mb/s data rate
  - Green - indicates 100 Mb/s data rate
  - Yellow - indicates 1000 Mb/s data rate.

Table 4-6 LAN1 Connector

Pin	Signal	Pin	Signal
1	LAN1_MDI0P	2	LAN1_MDI0N
3	LAN1_MDI1P	4	LAN1_MDI1N
5	+VCT_LAN_C	6	+VCT_LAN_C
7	LAN1_MDI2P	8	LAN1_MDI2N
9	LAN1_MDI3P	10	LAN1_MDI3N
L1	LAN1_LED_LNK#_ACT	12	LAN1_LED_LNK#_ACT_R
L3	LAN1_LED_1000#	14	LAN1_LED_100#

Table 4-7 LAN2 Connector

Pin	Signal	Pin	Signal
1	LAN2_MDI0P	2	LAN2_MDI0N
3	LAN2_MDI1P	4	LAN2_MDI1N
5	VCC1V8_LAN_C	6	VCC1V8_LAN_C
7	LAN2_MDI2P	8	LAN2_MDI2N
9	LAN2_MDI3P	10	LAN2_MDI3N
L1	LAN2_LED_LNK#_ACT	12	LAN2_LED_LNK#_ACT_R
L3	LAN2_LED_1000#	14	LAN2_LED_100#

4.9 WiFi/WiMax

The MITX-CORE-820 supports a PCI-Express Mini-Card 1.2 Dual Head to Head Socket designed to comply with the PCI-Express Mini-Card ElectroMechanical 1.2 Specification. The design supports a PCI-Express Display Mini-Card in place of the second half mini-card in the head to head socket design. The PCI-Express Mini-Card port is interoperable with the Intel WiMAX Link Advanced-N+ 6250 and WiFi Link Advanced-N 6200 Series wireless devices. The MITX-CORE-820 supports PCI-Express, USB and SMbus to all PCI-Express full mini-card, half mini-card, and display mini-card sites. The MITX-CORE-820 supports one display port to the display mini-card site.

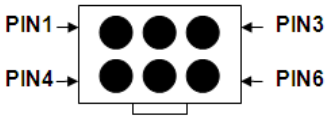
4.10 Storage

The MITX-CORE-820 supports two SATA 3G and two SATA 6G ports with standard vertical data connectors. The SATA power connector provides sufficient +3.3V, +5V, +12V power to accommodate both SSD and rotating-media drives of 1.8", 2.5" and 3.5" sizes. The MITX-CORE-820 supports RAID 0, 1, 5, 10 across all SATA interfaces (MITX-CORE-820 only).

Table 4-8 SATA HDD Power Connector Pinout (P17)

Pin	Signal	Pin	Signal
1	+V12S	2	GND
3	+V3.3S	4	GND
5	GND	6	+V5S

Figure 4-4 SATA HDD Power Connector (P17)



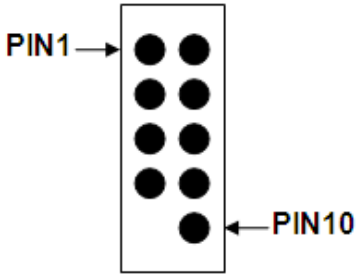
4.11 USB 2.0

The MITX-CORE-820 implements four standard type A connectors located in the backpanel I/O region of the motherboard. In addition, three standard.100"x.100" 10-pin, dual-row header supporting dual-ports are located on the motherboard (see Table 4-3 for pinout). One of the 10-pin headers provides mechanical support for retention standoff to support Intel® Z-U130 Value Solid State Drive (standard profile). All USB ports, including the powered USB, supports low-speed, full-speed, and high-speed using the USB 2.0 Enhanced Host Controller Interface (EHCI). Figure 4-5 shows the pinout of the connector.

Table 4-9 USB Internal Header (P24, P25, P26) Pinout

Pin	Signal	Pin	Signal
1	+V5A	2	+V5A
3	USB_PN1	4	USB_PN2
5	USB_PP2	6	USB_PP2
7	GND	8	GND
9	NC	10	NC

Figure 4-5 USB Internal Header (P24, P25, P26)



4.12 Power Supplies

The MITX-CORE-820 receives power from an input power connector that accepts +12 V or +14.4 V~+19.5 V in the back-panel IO region, or from a 4-pin +12 V ATX power connector. When a charger board is used, the power can be supplied using a 4-pin +12 V ATX power connector from the adapter or battery connected to charger board.

Table 4-10 DC-IN Jack Pin Definitions

Pin	Signal	Pin	Signal
1	GND	2	+VDC_IN
3	GND	4	+VDC_IN

Figure 4-6 DC-IN Jack Front View

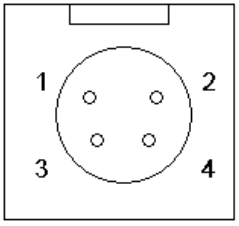
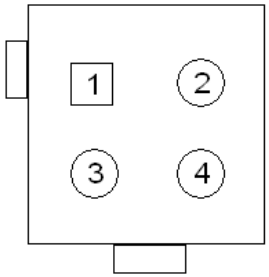


Table 4-11 ATX Power Supply Connector (J12)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+VDC_IN	4	+VDC_IN

Figure 4-7 ATX Power Supply Connector Top View



4.12.1 Power Consumption

The following table lists the estimated maximum power consumption of MITX-CORE-820 in three states:

Table 4-12 Board MAX Power Consumption Estimation

State	Power Consumption	Configuration
Idle (CMOS Setup)	30W	SNB i7-2710QE, 2x 2G SODIMM
Idle (Windows XP Pro)	20W	
Full Loading (TAT+3DMark)	70W	SNB i7-2710QE, 2x 4G SODIMM

4.12.2 Power Sequencing Requirements

The power sequencing meets the PCH power sequencing requirements.

4.12.3 Power Management

The MITX-CORE-820 design is ACPI 4.0a compliant. System power states S0 (Power-on), S3 (Suspend to RAM), S4 (Suspend to Disk), and S5 (Soft Off) is supported. Deep Sleep Sx is also supported after the option in BIOS setup is enabled. The board provides FET's to power off appropriate power planes.

4.12.4 Power Measurement

The MITX-CORE-820 design provides the ability to measure power consumption on DC-IN supply rails.

4.13 Embedded Controller

The MITX-CORE-820 design implements a Nuvoton NPCE791C embedded controller. The following sections list the functionality of the embedded controller, or EC.

4.13.1 Voltage Monitor

The MITX-CORE-820 design implements voltage monitoring capability on +V3A, +V5A and +V1.5S rails. The ADC of EC can be used as voltage monitor.

4.13.2 Serial Port

EC implements one RS-232 compatible serial port on the rear IO. It has RXD, TXD, RTS#, CTS# and RI# signals on the port.

Table 4-13 Serial Port Connectors (J5)

Pin	Signal	Pin	Signal
1	NC	2	COM_RXD#
3	COM_TXD	4	NC
5	GND	6	NC
7	COM_RTS#	8	COM_CTS#
9	COM_RI#		

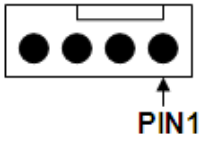
4.13.3 Fan Header

The MITX-CORE-820 design provides one 4-wire fan header on the motherboard planar for the CPU fan and one 4-wire fan header on the motherboard planar for the system. Fans support fan tachometer input and PWM fan speed control. The design uses 4-pin locking connector equivalent to Molex 47053-1000. Table 4-14 shows the pinout.

Table 4-14 CPU and System Fan Headers (P2 and P23) Description

Pin	Signal	Pin	Signal
1	GND	2	+V12S
3	TACH	4	PWM

Figure 4-8 CPU and System Fan Headers (P2 and P23)



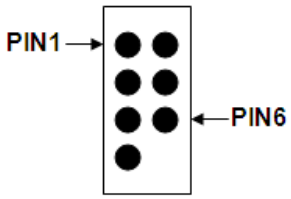
4.13.4 PS/2

The MITX-CORE-820 design implements two PS/2 ports for keyboard and mouse. The ports may be implemented as vertical headers on the motherboard planar if there is no space in the backpanel I/O region. One PS/2 header can support two PS/2 ports for keyboard and mouse. Table 4-15 and Figure 4-9 shows the pinout for PS/2.

Table 4-15 PS/2 Header (P5) Description

Pin	Signal	Pin	Signal
1	KB_DATA	2	MOUSE_DATA
3	GND	4	+V5A
5	KB_CLK	6	MOUSE_CLK
7	NC	8	KEY

Figure 4-9 PS/2 Header (P5)



4.13.5 Debug Header

This header is used only for debugging.

Table 4-16 EC Debug Header (P14) Description

Pin	Signal	Pin	Signal
1	EC_TCK	2	EC_TDO
3	EC_TMS	4	GND
5	EC_TDI	6	EC_RDY#

4.13.6 Charge Board Interface

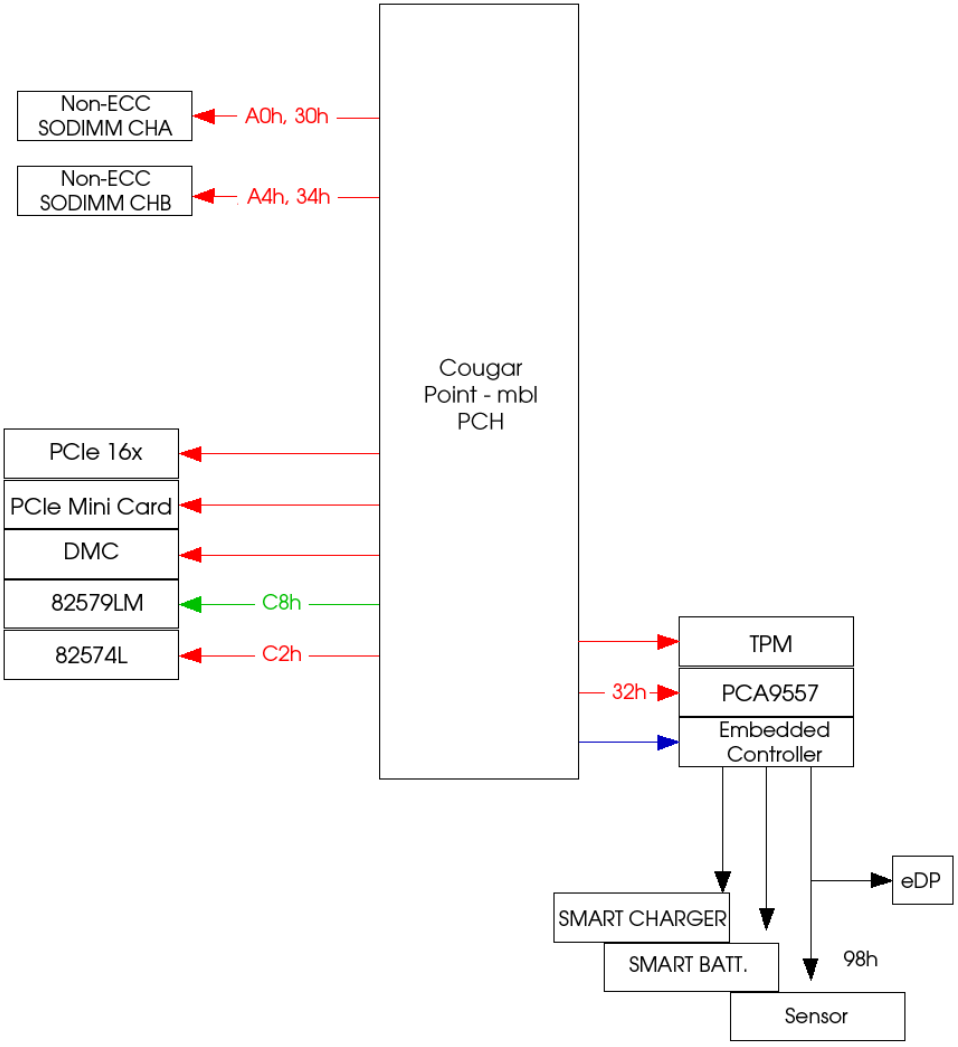
The MITX-CORE-820 design supports a charge board interface from the EC. There are two SMBUS communicating with the Smart Charger and the Smart Battery respectively. EC also accepts ACAV (AC_Present) and monitors charge/discharge current information from the charge board.

Table 4-17 Charge Board Interface (P22)

Pin	Signal	Pin	Signal
1	SMB_BS_DATA	2	SMB_BATT_DATA
3	GND	4	CHAR_ACAV
5	SMB_BS_CLK	6	SMB_BATT_CLK
7	CHAR_IAC	8	KEY

4.14 SMBUS Architecture

Figure 4-10 SMBUS Architecture



4.15 Audio

The MITX-CORE-820 design supports a minimum 7.1-channel HD Audio CODEC with the following connectivity:

- Rear IO
  - Stereo Line In
  - Stereo Line Out (Front Speakers)
  - Mic In
  - Stereo Rear Speakers
  - Middle/Sub Speaker
  - S/PDIF and Stereo Side Speakers
- Internal Audio Header
  - Mic In
  - Stereo Headphone Out
  - S/PDIF

Table 4-18 Audio Jack Board Side Pin Definitions (J11)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AGND	2	MIC1_L	3	MIC1_JD	4	AGND	5	MIC1_R
		22	LOUT_L	23	LOUT_JD	24	AGND	25	LOUT_R
		32	LIN_L	33	LIN_JD	34	AGND	35	LIN_R
41	AGND	42	CEN_CN	43	CEN_JD	44	AGND	45	LFE_CN
		52	SURR_L_CN	53	SURR_JD	54	AGND	55	SURR_R_CN
A	SPDIF_OUT	B	+V5S	C	GND				

Figure 4-11 Rear Panel Audio Jack

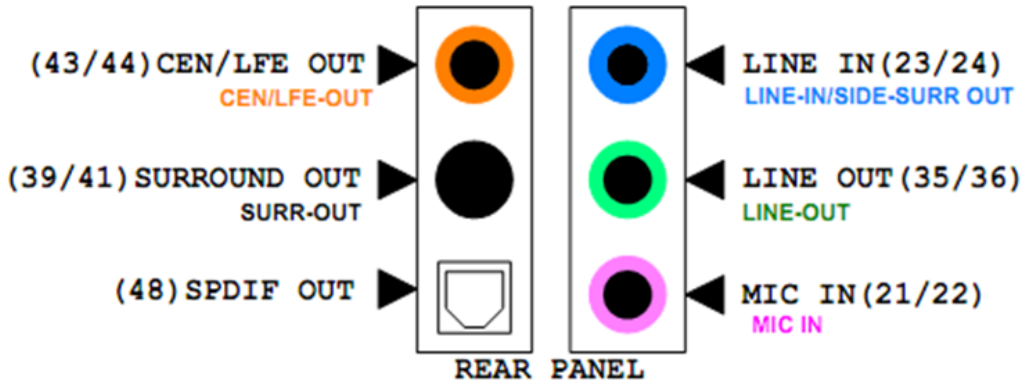


Table 4-19 Front Panel Audio Header (P9) Description

Pin	Signal	Pin	Signal
1	MIC2_L	2	GND
3	MIC2_R	4	FP_AUDIO_PSNT#
5	LOUT2_R	6	MIC2_JD
7	GND	8	KEY
9	LOUT2_L	10	LOUT2_JD

Figure 4-12 Front Panel Audio Header (P9)

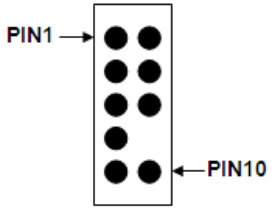


Table 4-20 S/PDIF Out Header (P30)

Pin	Signal
1	+V5S
2	SPDIF_OUT_HDMI
3	GND

This function is optional as per user's request.

4.16 Watchdog Timer

The MITX-CORE-820 implements a two-stage watchdog timer (WDT), such as the one integrated with PCH, with a programmable timeout (one second to ten minutes minimum) and the ability for software to enable and disable. The BIOS disables the device at boot, and the software will re-enable when watchdog application loads. Stage-1 timeout event causes an interrupt and Stage-2 timeout event causes a reset. WDT is disabled before entering S3 state, and re-enabled upon exiting S3.

4.17 RTC Circuit

There is an on-board battery holder for a BR2032 or an equivalent battery. This battery holder allows for quick and easy replacement of a 3 V button cell lithium battery which provides back-up power to the on-board RTC.

Table 4-21 Clear CMOS Header (P4)

Pin	Signal	Pin	Signal
1	NC	2	RTC_RST#
3	GND		

4.17.1 Boot Block

The SPI flash supports the boot block section which contains the code to boot to a minimum DOS. Once the board boots to a minimum DOS, the software program to reflash, the SPI flash can be run from the DOS command prompt. The boot block will be completely protected.

4.18 SPI Flash

The MITX-CORE-820 design does not support a firmware hub. Instead, it has two SPI flash devices (minimum 8 MB each) that provides flash support for the system BIOS, Intel® WG82579LM LAN image/MAC address and the manageability engine/AMT firmware. The SPI flash devices can be socketed during debugging. SPI flash provides an alternative to the firmware hub for system BIOS.

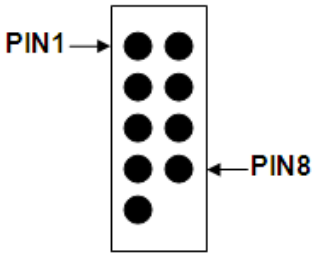
4.19 Front Panel Header

There is a standard front panel header on the board:

Table 4-22 Front Panel Header (P1) Definition

Pin	Signal	Pin	Signal
1	SATA_LED#_R	2	POWER_LED#_R
3	SATA_LED#	4	POWER_LED#
5	GND	6	EXT_PWRBTN_N
7	PM_SYSRST#	8	GND
9	NC	10	KEY

Figure 4-13 Front Panel Header (P1)



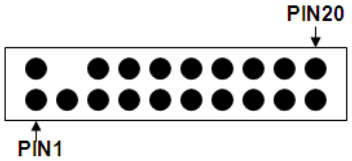
4.20 TPM/Port 80 Interface

There is an Intel standard 2x10 100" header for TPM and Port 80 debug on the board. In some cases, the PCI-Express card and the TPM module can exist together on the board. However, if the height of the heat sink from the bottom of the PCI-Express 16x card is over the standard specifications, it may have a mechanical conflict with the TPM module, which is plugged on to the TPM header. This is not a defect on the motherboard.

Table 4-23 TPM/Port80 Header (P3) Definition

Pin	Signal	Pin	Signal
1	CLK_PCI_TPM	2	GND
3	LPC_FRAME#	4	KEY
5	TPM_RST_N	6	+V5S
7	LPC_AD3	8	LPC_AD2
9	+V3.3S	10	LPC_AD1
11	LPC_AD0	12	GND
13	SMB_CLK_S	14	SMB_DATA_S
15	+V3.3A	16	INT_SERIRQ
17	GND	18	TPM_CLKRUN_N
19	PM_SUS_STAT#	20	PCH_DRQ#0

Figure 4-14 TPM/Port80 Header (P3)



4.21 On Board LED Interface

There is only one LED on board (D5) to indicate that the system has experienced a catastrophic error and cannot continue to operate. There are LED interfaces on the front header to indicate the power LED and SATA HDD activity. The power LED is driven by the embedded controller. There are two other LED headers to show charge status indication. One is used to indicate charging and one is used to indicate insufficient battery.

Table 4-24 Charge LED 1 (P31)

Pin	Signal
1	+V3.3A_KBC
2	C_PWM

Table 4-25 Charge LED 2 (P34)

Pin	Signal
1	+V3.3A_KBC
2	D_PWM

4.22 Case Open Header

Case open header is reserved for customized application.

Table 4-26 Case Open Header (P27)

Pin	Signal
1	SM_INTRUDER#
2	GND

4.23 Internal Graphics Disable

Table 4-27 Internal Graphics Disable Header (P33)

Jumper setting (Jumper:P33)	Configuration
P33 (1-2)	NC (DEFAULT)
P33 (2-3)	I-GRAPHICS DISABLE

4.24 User GPIO Header

The MITX-CORE-820 supports a GPIO header with support for 4xGPI and 4xGPO & ground(s).

Table 4-28 User GPIO Header (P28)

Pin	Signal	Pin	Signal
1	PCA9557_GPO0	2	PCA9557_GPI0
3	PCA9557_GPO1	4	PCA9557_GPI1
5	PCA9557_GPO2	6	PCA9557_GPI2
7	PCA9557_GPO3	8	PCA9557_GPI3
9	+V5A	10	GND

4.25 Debug Support

The MITX-CORE-820 shall support the following ports for debug:

- Extended Debug Port (XDP) tool for processor run control and debug
- Port 80 display for BIOS POST codes

4.26 Wake Events

The MITX-CORE-820 supports a wake up signal header, that can cause the platform to move from S3 sleep state to S0.

Table 4-29 Wake Up Header (P18)

Pin	Signal
1	+V5A
2	GND
3	WAKEUP_GPI

4.27 Manageability

The Gala MITX-CORE-820 supports Intel AMT 7.0. design and provides support for M0, M1 and M-off manageability states. It also supports serial-over-console, IDE redirect, remote power up, shutdown and reset. The Gala MITX-CORE-820 reads and receives alerts for voltage monitor, fan tachometer, CPU temperature and ambient temperature. The AMT firmware used is written to expect the existence of an embedded ACPI controller that is typically found in Interl mobile reference designs.

5.1 Embedded Controller Overview

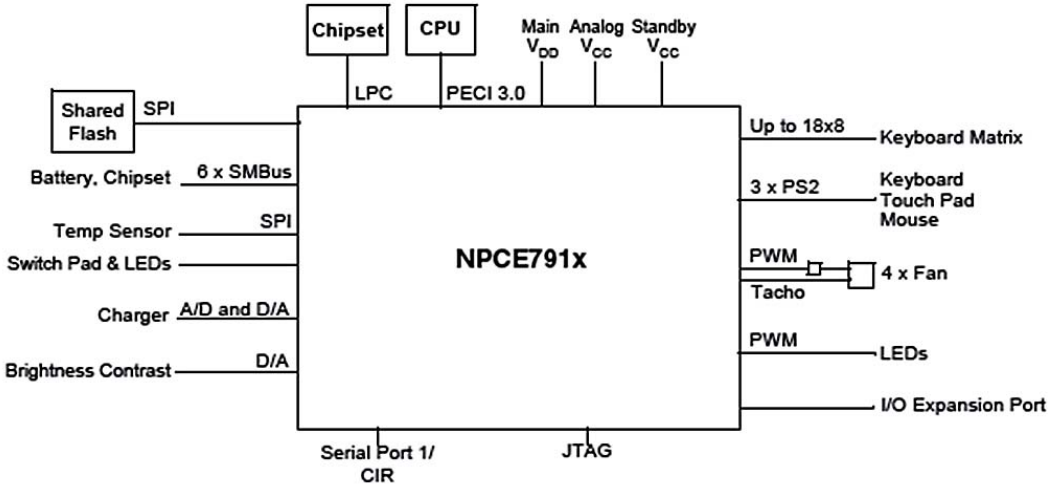
The embedded controller (EC) is an essential component in modern mobile, ultra-mobile and embedded computer systems.

The Nuvoton keyboard controller and scanner firmware for the Nuvoton NPCE791x keyboard/embedded controller is compatible with the industry standard 8042 interface and can scan locally defined OEM keyboard matrix. It simultaneously supports a scanned keyboard, external keyboards, and PS/2 mice. Options are also available for battery charging and monitoring firmware. EC firmware is also fully functional in ACPI(SCI) or legacy environments.

In the MITX-CORE-820, the NPCE791C from Nuvoton was selected as the EC silicon. It provides the power sequence controller, PS2 KB/MS interface, battery management, thermal/temperature/fan speed control, serial port and LED controller.

The following diagram shows the system block of NPCE791x.

Figure 5-1 NPCE791x System Block Diagram



The NPCE791x is a highly integrated, embedded controller with an embedded RISC core and system functions. It targets a wide range of portable applications that use the Low Pin Count (LPC) interface and is designed to best meet the requirements of mobile systems.

5.2 System BIOS Porting

5.2.1 Host Configuration Address

The host processor accesses the NPCE791x keyboard/mouse host interface and registers at two addresses in the host address domain. These addresses are defined by two internal chip select specified in the NPCE791x host configuration registers.

5.2.2 Index-Data Register Pair

The core can set the address of the Super I/O configuration index/data register using HCBAL and HCBAH, which are byte-wide read/write register. HCBAL holds the least significant byte of a host motherboard PnP initial configuration address; while HCBAH holds the most significant byte. HCBAL and HCBAH registers are set to their default values by power-up reset and input reset. HCBAH is set to 00h, HCBAL is set to 4Eh to Super I/O configuration index/data address of 4E/4Fh. However, the HCBAL and HCBAH registers can be modified by a special process, please refer to NPCE791x datasheet.

5.2.3 Blanked Logical Device Register Structure

Each functional block is associated with a logical device number (LDN). The configuration registers are grouped in banks, with each bank holding the standard configuration registers of the corresponding logical device.

This table shows the LDN values of the NPCE791x functional blocks. Any value not listed is set as reserved.

Table 5-1 LDN Values

LDN	Functional Block
03h	Serial Port 1
04h	Mobile System Wake-Up Control
05h	KBC - Mouse Interface
06h	KBC - Keyboard interface
0Fh	Shared Memory

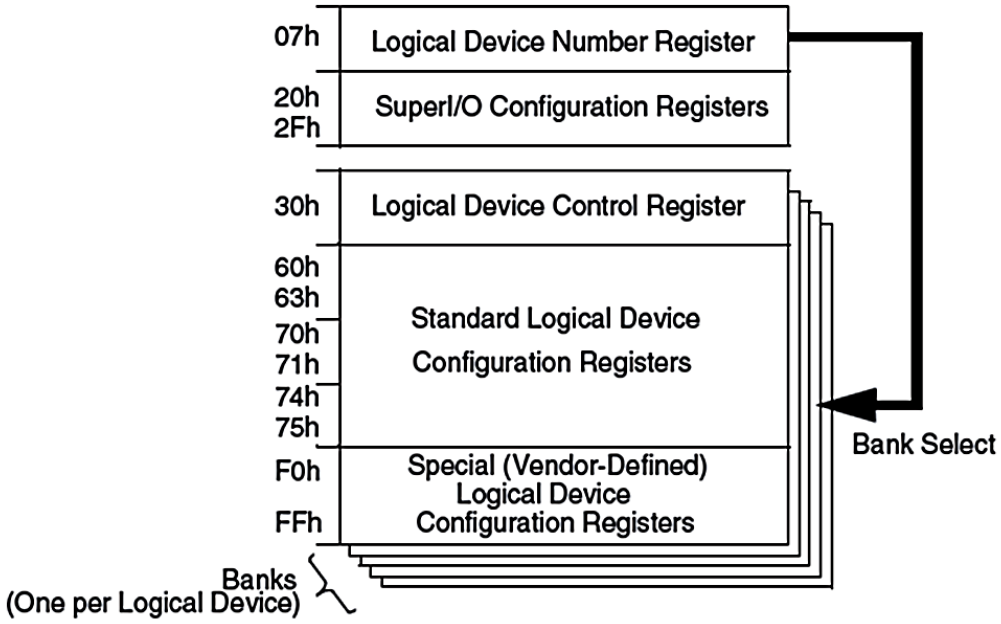
Table 5-1 LDN Values (continued)

LDN	Functional Block
11h	Power Management I/F Channel 1
12h	Power Management I/F Channel 2
17h	Power Management I/F Channel 3
1Dh	Extended Shared Memory

The host function control and configuration registers are not banked and are accessed only by the index-data register pairs. However, the device control and device configuration registers are replicated over the banks of each logical device. Two-dimensional indexing is used to access a specific register in a specific bank: the LDN register which selects the bank; and the index

registers which selects the register within the bank. Accessing the data register while the index register holds a value of 30h or higher actually accesses the logical device configuration registers. These are currently pointed to by the index register within the logical device currently selected by the LDN register

Figure 5-2 Structure of Standard Configuration Register



5.2.4 Standard Logical Device Configuration Register

All the standard logical device configuration registers can be accessed by the host processor after reset. All registers are read/write enabled. The following table shows the detailed definition of standard logical device configuration registers.

Table 5-2 Standard Configuration Register Map

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device number.
20h	Super I/O ID	Super I/O configuration register and ID registers
21h	Super I/O Configuration 1	
24h	Super I/O Chip Revision	
25h	Super I/O Configuration 5	
26h	Super I/O Configuration 6	
27h	Super I/O Revision ID	
28h	Super I/O General Purpose Scratch	
29h	Super I/O Configuration 9	
2Dh	Super I/O Configuration D	
2Eh - 2Fh	Reserved for Nuvoton use	
30h	Logical Device Control (Activate)	Enable or disable the logical device
60h - 61h	IO Base Address Descriptor 0	Indicates selected I/O lower limit address
62h - 63h	IO Base Address Descriptor 1	
70h	Interrupt Number	Indicates selected interrupt number
71h	IRQ Type Select	Indicates the type and polarity of the interrupt request number selected in 70h
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 or DMA 1 of the logical device.
75h	DMA Channel Select 1	
F0h - FFh	Device Specific Logical Device Configuration	Special (vendor-defined) configuration options.

5.2.5 KBC Address to Host Processor

The legacy settings of the keyboard and mouse addresses are 60h and 64h for the status/command and data registers.

This table shows the register mapping to the host processor I/O space. For simplicity, the host interface module specification refers to the legacy addresses.

Table 5-3 Mapping of Host Interface Registers to the Host Processor

Port	Legacy Address	Internal Chip Select	Type	Register Name
Keyboard and Mouse	60h	Keyboard/Mouse Data	Write	Data
	64h	Keyboard/mouse Command	Write	Command
	60h	Keyboard/Mouse Data	Read	Data
	64h	Keyboard/Mouse Command	Read	Status

5.2.6 EC I/O Port

The EC standard commands as described in ACPI 2.0 specifications are directly processed by the hardware logic. The data and command/status ports are set by default to 62h and 66h respectively and can be optionally mapped to other I/O address.

5.2.6.1 EC Status Register

The following table shows the EC status I/O Port Register.

Table 5-4 EC Status I/O Port Register

Status Bit	Name	Description
7	Reserved	
6	Reserved	
5	SCI	1: Indicates if there are more SCI event or events in the SCI queue. Upon detecting this bit being set, the system should query the SCI event queue to obtain the SCI ID number. Receiving and completing the EC standard commands will not cause the SCI bit to be set.

Table 5-4 EC Status I/O Port Register (continued)

Status Bit	Name	Description
4	Burst Enable	1 - Enables the burst 0 - Disables the burst
3	Flag	1 = Previous access port is command port (EC_CMD/EC_STS) 0 = Previous access port is data port
2	Reserved	
1	IBF	Input buffer full flag
0	OBF	Output buffer full flag

5.2.7 EC Command Register

There are seven valid commands for the EC command register (Write IO 66h). Other values are ignored by the EC if it is being written.

Table 5-5 EC Command Register

Value	Command	Description
80h	EC Read	Read operation for an internal register in EC space
81h	EC Write	Write operation for an internal register in EC space
82h	EC Burst Enable	Enable EC burst operation mode
83h	EC Burst Disable	Disable EC burst operation mode
84h	EC Query	Query the SCI event queue
Others	Firmware Command	No responded from hardware EC.

5.2.8 EC Command Program Sequence

Table 5-6 EC Command Program Sequence

Command Byte	Command Name	Programming Sequence
80h	Read EC	Write EC_CMD with 80h Write address byte to EC_DAT Wait SCI for OBF=1 Read EC_DAT with data in
81h	Write EC	Write EC_CMD with 81h Wait SCI for IBF=0 Write address byte to EC_DAT Wait SCI for IBF=0 Write data byte to EC_DAT Wait SCI for IBF=0
82h	Burst Enable	Write EC_CMD with 82h Wait SCI for OBF=1 Read EC_DAT with 90h
83h	Burst Disable	Write EC_CMD with 83h Wait SCI for IBF=0
84h	Query EC	Write EC_CMD with 84h Wait SCI for OBF=1 Read EC_DAT with SCI ID number

5.2.9 EC Space Definition

Table 5-7 EC Space Definition

Table Offset	Length (Bytes)	Description
0x00	1	Thermal Version
0x01	1	Maximum Fan Level Support

Table 5-7 EC Space Definition (continued)

Table Offset	Length (Bytes)	Description
0x02	6	Fan Speed
0x08	2	Current Fan Speed
0x0A	1	CPU Level 1 Trip
0x0B	1	CPU Level 1 Hysteresis
0x0C	1	CPU Level 2 Trip
0x0D	1	CPU Level 2 Hysteresis
0x0E	1	CPU Level 3 Trip
0x0F	1	CPU Level 3 Hysteresis
0x10	1	CPU Level 4 Trip
0x11	1	CPU Level 4 Hysteresis
0x12	1	CPU Level 5 Trip
0x13	1	CPU Level 5 Hysteresis
0x14	1	CPU Level 6 Trip
0x15	1	CPU Level 6 Hysteresis
0x16	1	Throttling on threshold
0x17	1	Throttling off threshold
0x18	1	System Level 1 Trip
0x19	1	System Level 1 Hysteresis
0x1A	1	System Level 2 Trip
0x1B	1	System Level 2 Hysteresis
0x1C	1	System Level 3 Trip
0x1D	1	System Level 3 Hysteresis
0x1E	1	System Level 4 Trip
0x1F	1	System Level 4 Hysteresis
0x20	1	System Level 5 Trip
0x21	1	System Level 5 Hysteresis
0x22	1	System Level 6 Trip

Table 5-7 EC Space Definition (continued)

Table Offset	Length (Bytes)	Description
0x23	1	System Level 6 Hysteresis
0x24	1	VGA Level 1 Trip
0x25	1	VGA Level 1 Hysteresis
0x26	1	VGA Level 2 Trip
0x27	1	VGA Level 2 Hysteresis
0x28	1	VGA Level 3 Trip
0x29	1	VGA Level 3 Hysteresis
0x2A	1	VGA Level 4 Trip
0x2B	1	VGA Level 4 Hysteresis
0x2C	1	VGA Level 5 Trip
0x2D	1	VGA Level 5 Hysteresis
0x2E	1	VGA Level 6 Trip
0x2F	1	VGA Level 6 Hysteresis
0x30	1	Core1 Level 1 Trip
0x31	1	Core1 Level 1 Hysteresis
0x32	1	Core1 Level 2 Trip
0x33	1	Core1 Level 2 Hysteresis
0x34	1	Core1 Level 3 Trip
0x35	1	Core1 Level 3 Hysteresis
0x36	1	Core1 Level 4 Trip
0x37	1	Core1 Level 4 Hysteresis
0x38	1	Core1 Level 5 Trip
0x39	1	Core1 Level 5 Hysteresis
0x3A	1	Core1 Level 6 Trip
0x3B	1	Core1 Level 6 Hysteresis
0x3C	1	Core2 Level 1 Trip
0x3D	1	Core2 Level 1 Hysteresis

Table 5-7 EC Space Definition (continued)

Table Offset	Length (Bytes)	Description
0x3E	1	Core2 Level 2 Trip
0x3F	1	Core2 Level 2 Hysteresis
0x40	1	Core2 Level 3 Trip
0x41	1	Core2 Level 3 Hysteresis
0x42	1	Core2 Level 4 Trip
0x43	1	Core2 Level 4 Hysteresis
0x44	1	Core2 Level 5 Trip
0x45	1	Core2 Level 5 Hysteresis
0x46	1	Core2 Level 6 Trip
0x47	1	Core2 Level 6 Hysteresis
0x48	1	CPU temperature
0x49	1	System temperature
0x4A	1	VGA temperature
0x4B	1	CORE 1
0x4C	1	CORE 2
0x4D	1	CPU Offset
0x4E	1	CPU temperature for shutdown system
0x4F	1	Fan speed to be set
0x50	1	Throttling State
0x51	1	System Configuration Byte
0x52	1	Device Status Byte
0x90	1	Power Status
0x91	1	Reserved
0x92	2	Battery Voltage
0x94	2	Battery Current
0x96	2	Battery Relative State of Charge
0x98	2	Battery Remaining capacity

Table 5-7 EC Space Definition (continued)

Table Offset	Length (Bytes)	Description
0x9A	2	Battery Return Time to Empty
0x9C	2	Battery Status
0x9E	2	Battery Fully Charge Capacity
0xA0	2	Battery Designed Capacity
0xA2	2	Battery Designed Voltage
0xA4	2	Battery Average Time to Empty
0xA6	2	Battery Average Time to Full
0xA8	2	Battery Manufacture Date
0xAA	2	Battery Serial Number
0xAC	2	Battery Charging Current
0xAE	2	Battery Charging Voltage
0xB0	2	Battery Temperature

5.2.10 Event List

Table 5-8 Q Event List

Q Event ID	Description
_Q30	Real AC Insertion/Removal Event
_Q31	Real Battery Insertion/Removal Event
_Q32	Real Battery Low Event
_Q33	Real Battery Very Low Event
_Q34	CPU Throttling On/Off Event
_Q36	Thermal Trip Event

5.2.11 OS Driver Support

The ACPI-compliant operating systems provide the embedded controller driver and battery driver.

5.3 EC Firmware Porting

5.3.1 Power Sequence Control

The hardware provides the power sequencing table. The following tables should be filled to implement the platform's various power sequences.

```
/*
    Time base is 1mS.

    A --> "PORT PIN" of power sequence
    B --> Active "HIGH" or "LOW"
    C --> Delay time to next step.
    D --> Next sequence. The terminated signature of the sequence is
"0x7F".
    E --> Direction "OUTPUT" or "INPUT"
*/
const PWRSEQ_DESCRIPTOR PwrOnSeq_Table[] =
{
  /* A               B     C    D       E */
  {PORT_PIN(4, 0) | HIGH,  01, 0x01 | OUTPUT},    /* 0 - SB_ENABLE */
  {PORT_PIN(0, 6) | HIGH,  20, 0x02 | INPUT},     /* 1 - SB_PWROK */
  {PORT_PIN(4, 2) | HIGH,  20, 0x03 | OUTPUT},    /* 2 - RSMRST */
  {PORT_PIN(3, 3) | LOW,   01, 0x0A | OUTPUT},    /* 3 - PWRBTN_SB */
  {PORT_PIN(4, 7) | HIGH,  01, 0x7F | OUTPUT},    /* 4 - HW_PWRGD */
  {PORT_PIN(0, 7) | HIGH,  00, 0x00 | INPUT },    /* 5 - SLP_S4 */
  {PORT_PIN(5, 0) | HIGH, 100, 0x04 | OUTPUT},    /* 6 - CPU_VR_ON */
  {PORT_PIN(3, 0) | HIGH, 120, 0x06 | INPUT },    /* 7 - ALLPWROK */
  {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 8 - */
  {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 9 - */
  {PORT_PIN(1, 0) | HIGH,  01, 0x0B | INPUT },    /* A - SLP_S3 */
  {PORT_PIN(4, 4) | HIGH,  01, 0x0C | OUTPUT},    /* B - SUSON */
  {PORT_PIN(4, 5) | HIGH,  01, 0x07 | OUTPUT},    /* C - MAINON */
  {UNUSED_PIN     | LOW,   00, 0x00 | INPUT },    /* D - */
 {UNUSED_PIN     | LOW,   00, 0x00 | INPUT },    /* E - */
  {UNUSED_PIN     | LOW,   00, 0x00 | INPUT }     /* F - */
```

```
};
/* Power off Sequence Table */
const PWRSEQ_DESCRIPTOR PwrOffSeq_Table[] =
{
    /* A               B     C    D       E */
    {PORT_PIN(4, 7) | LOW,   20, 0x01 | OUTPUT},    /* 0 - HW_PWRGD */
     {PORT_PIN(5, 0) | LOW,  100, 0x02 | OUTPUT},   /* 1 - CPU_VR_ON */
    {PORT_PIN(4, 5) | LOW,   20, 0x03 | OUTPUT},    /* 2 - MAINON */
    {PORT_PIN(4, 4) | LOW,   01, 0x7F | OUTPUT},    /* 3 - SUSON */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 4 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT},     /* 5 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 6 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 7 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT},     /* 8 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT},     /* 9 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT}     /* A - Reserved */
};
const PWRSEQ_DESCRIPTOR SuspendSeq_Table[] =
{
    /* A               B     C    D       E */
    {PORT_PIN(4, 7) | LOW,   01, 0x01 | OUTPUT},    /* 0 - HW_PWRGD */
    {PORT_PIN(5, 0) | LOW,  100, 0x02 | OUTPUT},    /* 1 - CPU_VR_ON */
    {PORT_PIN(4, 5) | LOW,   01, 0x7F | OUTPUT},    /* 2 - MAINON */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 3 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT },    /* 4 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 5 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 6 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT },    /* 7 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT}     /* 8 - Reserved */
};
```

```
const PWRSEQ_DESCRIPTOR ResumeSeq_Table[] =
{
    /* A               B     C    D       E */
    {PORT_PIN(4, 4) | HIGH,  01, 0x01 | OUTPUT},    /* 0 - SUSON */
    {PORT_PIN(4, 5) | HIGH,  01, 0x02 | OUTPUT},    /* 1 - MAINON */
    {PORT_PIN(3, 0) | HIGH, 120, 0x03 | INPUT},     /* 2 - ALLPWROK */
    {PORT_PIN(5, 0) | HIGH, 100, 0x04 | OUTPUT},    /* 3 - CPU_VR_ON */
    {PORT_PIN(4, 7) | HIGH,  01, 0x7F | OUTPUT},    /* 4 - HW_PWRGD */
    {UNUSED_PIN     | LOW,   00, 0x00 | INPUT},     /* 5 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 6 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT},    /* 7 - Reserved */
    {UNUSED_PIN     | LOW,   00, 0x00 | OUTPUT}     /* 8 - Reserved */
};
```

5.3.2 PECI

EC should be able to read the CPU temperatures through the PECI interface. A PECI initialization and a PECI polling function should be implemented. Samples of this include OEM_PECI_Init(void) and OEM_PECI_Polling(void).

```
void OEM_PECI_Init(void)
{
    /*---------------------------------------------------------------*/
   /* Initialize the PECI module
*/
    /*---------------------------------------------------------------*/
    PECI_Init(PECI_CallBack, 0);

    /*---------------------------------------------------------------*/
  /* Configure PECI domain and client address
*/
    /*---------------------------------------------------------------*/
    PECI_SetDomain(PECI_DOMAIN);
    PECI_SetAddress(PECI_CLIENT_ADDR);

    peci_client_available = 0;
}

void OEM_PECI_Polling(void)
{

if(!(REG_READ(PECI_CTL_STS) & 0x01))   /*If PECI not busy*/
   {
        if(peci_client_available)
        {
            PECI_GetTemp();
        }
    else
    {
        PECI_Ping();
    }
    }
```

5.3.3 Thermal & Fan Speed Control

EC gets the CPU temperature by PECI interface. It can also get the memory temperature through the thermal sensor in the DIMM slot (the local thermal sensor of W83L771). EC can get the system temperature through the remove sensor of W83L771 (slave address 1001100xb).

There are two fans. One is for the CPU FAN (TA1, A_PVM) and the other is SYS FAN (TB1, B_PWM).

5.3.3.1 Thermal Trip

EC sets up the six thermal trip levels. The following table shows the instances of these levels.

Table 5-9 Thermal Trip Levels

State	Fan level	Fan speed (rpm)	CPU Temp (°C)		System Temp (°C)	
			Hysteresis	Trip	Hysteresis	Trip
0	Level 0	1200	40	50	40	50
1	Level 1	2400	45	60	45	60
2	Level 2	3600	55	65	55	65
3	Level 3	4800	60	70	60	70
4	Level 4	6000	65	83	65	83
5	Level 5	7000	80	92	80	92

5.3.3.2 Thermal Throttling

There is no applicable thermal throttling settings.

5.3.4 Battery Information - Charging & Discharging Control

The hardware selects a battery, so the EC firmware could report the battery information and write the code for charging and discharging.

There are five charging states:

- Wake-up charging
- Pre-charging

- Slow charging
- Fast charging
- Full charging

Discharging

- Monitor battery in low/very low states
- Generation sci/smi to host
- Blinking battery indicator
- Shutdown system
- Record system shutdown caused

Charging protection

- Terminate charging
  - Report from battery
  - Over voltage
  - Over temperature
  - Maximum safety time
- Discharging
  - Terminated discharging detected
  - Shutdown system
  - Avoid battery damaged

Hardware should select a battery.

5.3.5 Voltage Monitor

The MITX-CORE-820 uses the EC pins to monitor the following voltages: +5V, +3.3V, +1.5V, +1.5V. EC should be able to read the voltage and if possible, should have a method and pass the value to BIOS or EAPI application.

5.3.6 Wake Up Requirement

The PS2 kb/mouse supports wake up from sleep state, in both S1/S3, but not S5.

5.3.7 LEDs Control

The MITX-CORE-820 has a green LED and a red LED to indicate the charging or discharging status

Table 5-10 LED Control Status

Battery Status	Green LED Status	Red LED Status
Charging	Inactive	Active
Fully Charged	Active	Inactive
Discharging	Inactive	Inactive
Battery Low	Inactive	Blinking

A LED for indicating power on/off is implemented.

```
const LEDs_DESCRIPTOR LEDs_Table[] =
{
  {PORT_PIN(3, 2) | LOW, 0x00},   // 0 - Battery LED Green
  {PORT_PIN(3, 1) | LOW, 0x00},   // 1 - Battery LED RED
 {UNUSED_PIN     | LOW, 0x00},   // 2 - Scroll Lock LED
 {UNUSED_PIN  | LOW, 0x00},   // 3 - CAPS Lock LED
 {UNUSED_PIN | LOW, 0x00},   // 4 - NUMLock LED
 {UNUSED_PIN     | LOW, 0x00},   // 5 - Touchpad Disabled LED
 {UNUSED_PIN     | LOW, 0x00},   // 6 - Bluetooth LED
 {UNUSED_PIN     | LOW, 0x00},   // 7 - Wireless LED
 {UNUSED_PIN | LOW, 0x31},   // 8 - Power LED
 {UNUSED_PIN     | LOW, 0x00}    // 9 - 3G LED.
```

5.3.8 PS2 Interface & Device Configuration

NPCE791x provides three PS/2 channels including channel 1, channel 2 and channel 3. For the MITX-CORE-820, the channel 3 is for PS2 mouse, the channel 2 is for PS2 keyboard and the channel 1 is not used.

5.3.9 Input Events Detection through GPIO

EC detects the following events:

- Power Switch
- AC adaptor In/Out
- Battery In/Out Event

The power switch and AC adaptor In/Out could be detected through the event table below.

```
/*
  Time Base is 10mS.
    A --> "PORT PIN" definition for Events
    B --> Active "HIGH" or "LOW"
    C --> Event debounce counter.
    D --> "ACTION" of event
*/
const EVENT_DESCRIPTOR Events_Table[] =
   {   /* A                              B     C,      D*/
   {PORT_PIN(0, 3) | LOW,  10,    0x0000},      /* 0x00 - Power Switch Event.*/
   {PORT_PIN(0, 4) | HIGH, 10,   0x9130},     /* 0x01 - AC Adaptor In/Out Event. */
    {PORT_PIN(9, 1) | LOW,  10,    0x9131},      /* 0x02 - Battery In/Out Event. */
    {UNUSED_PIN     | LOW,  00,    0x9137},      /* 0x03 - PME Event. */
};
//#define Events_Size (sizeof(Events_Table) / sizeof(EVENT_DESCRIPTOR))
```

However, the MITX-CORE-820 does not have a GPIO pin for the battery in/out detection. EC uses the SMBUS polling method to detect if the battery is present.

5.4 EC Firmware Flash

5.4.1 Flash with SF100

The MITX-CORE-820 uses the Nuvoton W25Q80 as a flash device. The EC firmware is stored in the SPI flash part. The SF100 can be used to flash the firmware into the flash part.

5.4.2 Flash with ECDT

Nuvoton provides a USB to the JTAG board. A JTAG header is also reserved for the MITX-CORE-820 board. The EC debug tool can also be used to download the EC code to be used by the JTAG to flash the USB to the board.

5.4.3 Flash with Utility

Nuvoton provides the flash update application for Nuvoton embedded controllers. It runs on either 16-bit DOS or Windows XP/Vista 32-bit/64-bit. It programs the flash of the Nuvoton EC with the contents of a flash binary image file, which holds EC firmware and/or system BIOS.

5.4.4 Crisis Recovery

The NPCE791x BOOTER Program resides in the on-chip ROM. After reset, it performs all boot procedures, including NPCE791x initialization based on the header data. Then it checks the EC firmware in the flash and if it detects a problem, the BOOTER enters recovery mode and allows debugging via JTAG.

5.5 EC Debug Interface

5.5.1 Serial Port

The Serial Port 1 provides the UART functionality by supporting serial data communication with a remote peripheral device or a modem. The functional block can function as a standard 16450 or 16550 or as an extended UART. The BIOS can use it to implement the console redirection function.

5.5.2 JTAG Interface

The MITX-CORE-820 provides JTAG interface for the NPCE791x silicon. Connect the USB to the JTAG board with the Gala board through the ECDT utility to debug the EC firmware.

5.6 Accessing the ME BX Setup Menu

The following procedure will allow you to access the ME BX setup menu.

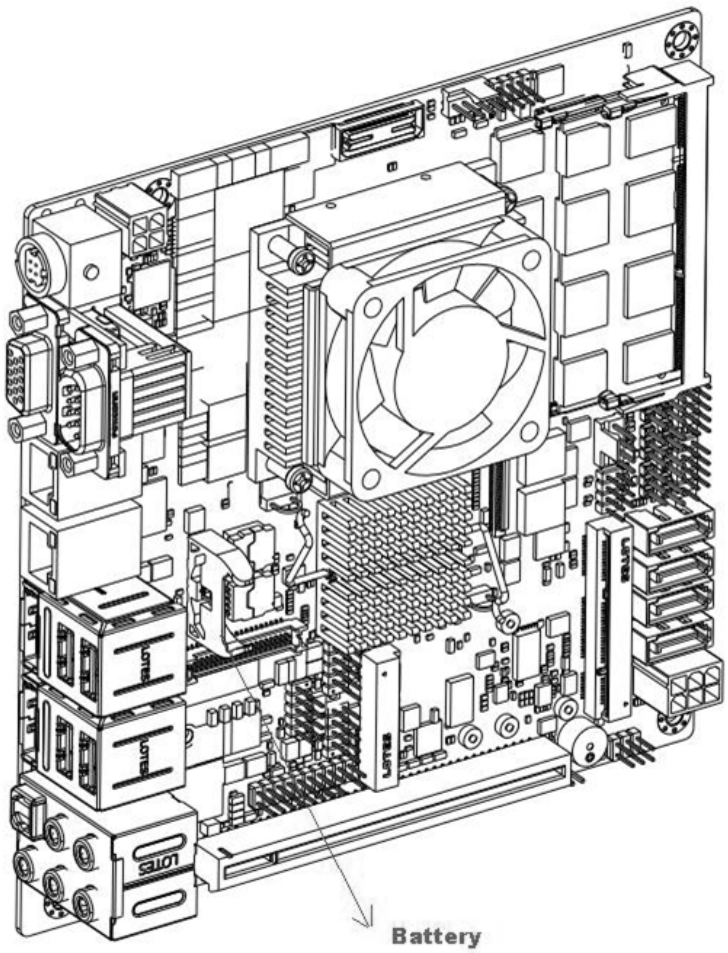
1. During BIOS POST, press the hotkey F4.
2. Disable the Intel AMT hotkey function in the BIOS setup. Select "Advanced", choose "Intel AMT configuration" then select "Intel AMT hotkey".
3. Enable the Intel AMT setup prompt that is located on the same page. Save and exit. During the BIOS POST, press CTRL+P.

Replacing the Battery

A.1 Overview

The board contains an on-board Lithium coin battery BR2032. Its location is show in the following figure:

Figure A-1 Battery Location



The battery provides data retention of one year summing up all periods of actual data use. Emerson therefore assumes that there usually is no need to exchange the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage

- Incorrect exchange of lithium batteries can result in a hazardous explosion.
- When exchanging the on-board lithium battery, make sure that both the new and the old battery are exactly the same battery models.
- If the respective battery model is not available, contact your local Emerson sales representative for the availability of alternative and officially approved battery models.

Data Loss

- If the battery no longer provides enough power, the RTC is initialized and the data in the NVRAM is lost.
- Exchange the battery before one year of actual battery use has elapsed.

Data Loss

- Exchanging the battery always results in data loss of the devices which use the battery as power backup.
- Back up affected data before exchanging the battery.

Data Loss

- Installing a battery type other than the type installed by the manufacturer may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime.
- Only use the same type of lithium battery as is already installed.

A.2 Procedure Description

The following procedure describes how to exchange the battery.

Exchange Procedure

To exchange the battery, proceed as follows:

NOTICE

PCB and Battery Holder Damage

- **Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.**

Product Damage

- **Do not deform the battery holder retaining tab during the battery exchange procedure so that the battery holder retaining tab continues to perform its function and so that the battery holder maintains a low profile.**

1. Gently lift the battery retaining tab.
2. Remove the battery.
3. Install the new battery in such a way that the plus sign marked on it is face up.

Related Documentation

B.1 Emerson Network Power - Embedded Computing Documents

The publications listed below are referenced in this manual. You can obtain electronic copies of Emerson Network Power - Embedded Computing publications by contacting your local Emerson sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Visit http://www.emersonnetworkpower.com/embeddedcomputing.
2. Under **Resources**, click **Technical Documentation**.
3. Enter the publication number or the complete name of the product in the Search box.

Table B-1 Emerson Network Power - Embedded Computing Publications

Document TItle	Publication Number
MITX-CORE-820 Quick Start Guide	6806800M44D
MITX-CORE-820 Safety Notes Summary	6806800M43D
MCASE-820 Installation and Use	6806800M41D

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Emerson intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Emerson representative.

The product has been designed to meet the standard industrial safety requirements. It must only be used in its specific area of office telecommunication industry, industrial control, and development. It must not be used in safety critical components, life supporting devices or on aircraft.

Only personnel trained by Emerson or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel is allowed to remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Emerson representative for service and repair to make sure that all safety features are maintained.

Emerson and our suppliers take significant steps to make sure that there are no bent pins on the backplane or connector damage to the boards prior to leaving the factory. Bent pins caused by improper installation or by inserting boards with damaged connectors could void the Emerson warranty for the backplane or boards.

This product operates with dangerous voltages that can cause injury or death. Use extreme caution when handling, testing, and adjusting this equipment and its components.

System Installation

Damage of Circuits

Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten its life.
Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Pin Diagram
Forcing the module into the system may damage connector pins.
If the module hangs during insertion, pull it out and insert it again.

Damage of the Product and Additional Devices and Modules
Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.
Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.

Operation

System Damage
During the course of handling, shipping, and assembly, pins, mounting screws, fans and other items can become loose or damaged.
Do not operate a damaged shelf, this can cause damage to devices that interact with it.

System Overheating
Cooling Vents

Improper cooling can lead to blade and system damage and can void the manufacturer's warranty.
To ensure proper cooling and undisturbed airflow through the system always operate the system in a horizontal position. Do not obstruct the ventilation openings at the top, sides and back of the system. Keep the fresh air intake at the bottom-front side of the chassis completely clear. Make sure that the fresh air supply is not mixed with hot exhaust from other devices. Make sure that all slots are populated with either blades, filler blades, or dummy blades.

Product Damage
High humidity and condensation on surfaces cause short circuits.
Do not operate the product outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Expansion and FRU Replacement

Product Damage
Bent pins or loose components can cause damage to the product, the backplane, or other system components.
Carefully inspect the product and the backplane for both pin and component integrity before installation.

Personal Injury
During operation, hot surfaces may be present on the heat sinks and components of the product.
To prevent injury from hot surfaces do not touch any of the exposed components or heatsinks on the product when handling. Use the handle and face plate when removing the product from the enclosure.

Battery

Data Loss
If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
Replace the battery before seven years of actual battery use have elapsed.

Data Loss
Replacing the battery always results in data loss of the devices which use the battery as power backup.
Back up affected data before exchanging the battery.

Data Loss
Installing another battery type than the one that is mounted at product delivery may cause data loss since other battery types may be specified for other environments or may have a shorter lifetime.
Only use the same type of lithium battery as is already installed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder.
Do not use a screw driver to remove the battery from its holder.

Environment

Environmental Damage
Improperly disposing of used products may harm the environment.
Always dispose of used products according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Systems innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am System zur Folge haben.

Emerson ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem System in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem System um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Emerson.

Das Produkt erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie, im Zusammenhang mit Industriesteuerungen und in der Entwicklung verwendet werden. Es darf nicht in sicherheitskritischen Anwendungen, lebenserhaltenden Geräten oder in Flugzeugen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Emerson ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Systems fern. Entfernen Sie auf keinen Fall die Systemabdeckung. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf die Systemabdeckung entfernen, um Systemkomponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am System durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Emerson. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

System Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Schäden an Steckern
Wenn Sie das Modul mit Gewalt installieren, können die Anschlussstifte in den Steckern beschädigt werden.
Falls sich das Modul während der Installation verkantet, ziehen Sie es wieder heraus und führen Sie sie erneut ein.

Beschädigung des Produktes und der Zusatzmodule
Fehlerhafter Ein- oder Ausbau von Zusatzmodulen führt zu Beschädigung des Produktes oder der Zusatzmodule.
Lesen Sie deshalb vor dem Ein- oder Ausbau von Zusatzmodulen die Dokumentation und benutzen Sie angemessenes Werkzeug.

Betrieb

Beschädigung des Systems
Während des Transportes, Zusammenbaus und dem Umgang mit dem System können sich Schrauben, Lüfter oder andere Teile lösen oder beschädigt werden.

Nehmen Sie ein beschädigtes System nicht in Betrieb. Sonst können andere Einrichtungen, die mit dem System kommunizieren, beschädigt werden.

Überhitzung des Systems
Lüftungsöffnungen

Unzureichende Lüftung kann Schäden an Blades und am System verursachen und die Herstellergarantie ungültig werden lassen.
Um eine ausreichende Lüftung zu gewährleisten, stellen Sie sicher, dass das System während des Betriebs waagerecht steht. Halten Sie die Lüftungsschlitze an der Oberseite, der Rückseite und den Seiten des Systems frei. Halten Sie die Frischluftzufuhröffnung an der unteren Vorderseite des Systems völlig frei und stellen Sie sicher, dass sich die Frischluft nicht mit der Abluft von anderen Systemen mischt.

Beschädigung des Systems
Hohe Luftfeuchtigkeit und Kondensat auf den Oberflächen der Produkte kann zu Kurzschlüssen führen.
Betreiben Sie die Produkte nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur und stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf den Produkten kein Kondensat befindet.

Erweiterung und FRU Austausch

Beschädigung des Produktes
Verbogene Stecker oder lose Teile können das Produkt, die Backplane oder andere Systemkomponenten beschädigen.
Prüfen Sie das Produkt und die Backplane vor dem Einabau sorgfältig auf verbogene Stecker und lose Teile.

Verletzungsgefahr
Während des Betriebs können Oberflächen an den Kühlkörpern oder anderen Komponenten sehr heiß werden.
Um Verletzungen durch Verbrennung zu vermeiden, berühren Sie während der Arbeit keine Komponenten oder Kühlkörper auf dem Produkt. Fassen Sie das Produkt an den Handles und der Frontblende an, wenn Sie es aus dem System herausnehmen.

Batterie

Datenverlust
Wenn die Batterie nur noch ungenügend geladen ist, wird der RTC zurückgesetzt und Daten im NVRAM gehen verloren.
Tauschen Sie daher die Batterie nach spätestens einem Jahr aus.

Datenverlust
Der Austausch der Batterie führt unweigerlich zu Datenverlust bei Bauteilen, die die Batterie als Backup verwenden.
Sichern Sie daher alle Daten, die bei Austausch der Batterie verloren gehen.

Datenverlust
Wenn Sie einen anderen Batterietyp installieren als der, der bei Auslieferung des Produktes installiert war, kann Datenverlust die Folge sein, da die neu installierte Batterie für andere Umgebungsbedingungen oder eine andere Lebenszeit ausgelegt sein könnte.
Verwenden Sie daher den gleichen Batterietyp, der bei Auslieferung des Produktes installiert war.

Beschädigung des PCBs und der Batteriehalterung
Wenn Sie die Batterie mit einem Schraubendreher ausbauen, können das PCB und die Batteriehalterung beschädigt werden.
Benutzen Sie keinesfalls einen Schraubendreher um die Batterie aus der Halterung zu nehmen.

Environment

Umweltverschmutzung
Falsche Entsorgung der Produkte schadet der Umwelt.
Entsorgen Sie alte Produkte gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

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HOW TO REACH LITERATURE AND TECHNICAL SUPPORT:

For literature, training, and technical assistance and support programs, visit
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