Technical Note

Migrating from Macronix's MX25L25635F to Micron's N25Q 256Mb Flash Device

Introduction

The purpose of this technical note is to compare features of the Micron® N25Q (256Mb) and Macronix MX25L25635F Flash memory devices. Features compared include memory organization, package options, signal descriptions, the software command set, electrical specifications, and device identification.

Memory Array Architecture

Table 1: Device Comparison

N25Q Features	MX25L Features
Program 1 to 256 bytes	Program 1 to 256 bytes
Uniform sector erase (64KB)	Uniform sector erase (32KB and 64KB)
Uniform subsector erase (4KB)	Uniform subsector erase (4KB)
Cycling endurance 100,000	Cycling endurance 100,000
Data retention 20 years	Data retention 20 years

Package Configurations

Table 2: Package Configurations

Package	N25Q 256Mb	MX25L25635F
V-PDFN8 (8mm x 6mm)	Yes	Yes
SOP2-16/300 mil	Yes	Yes
T-PBGA24 (6mm x 8mm)	Yes	–

Signal Descriptions

Table 3: Signal Descriptions

N25Q Signal	MX25L Signal	Type	Description	Notes
C	SCLK	Input	Serial clock	
DQ0	SI/SIO0	Input or I/O	Serial data input or I/O	
DQ1	SO/SIO1	Output or I/O	Serial data output or I/O	
S#	CS#	Input	Chip select	
W#/V_{PP}/DQ2	WP#/SIO2	Input or I/O	Write protect/enhanced program supply voltage or I/O	1
HOLD#/DQ3	RESET#/SIO3	Input or I/O	HOLD or I/O	
V_{CC}	V_{CC}	Input	Supply voltage	
V_{SS}	GND	Input	Ground	
RESET#				2

Notes:
1. V_{PP} is not available on the MX25L25635F device.
2. The additional RESET pin is available for part numbers N25Q256A83E1240X and N25Q256A83ESF40X only. On these two parts, the additional RESET pin must be connected to an external pull-up. For the MX25L device, the pull-up is internal. For other part numbers, RESET# takes the place of HOLD#.

Commands

Table 4: Command Set

Command	Command Code N25Q	Command Code MX25L25635F	Notes
RESET Operations			
READ ENABLE	66h	66h	
RESET MEMORY	99h	99h	
NOP	N/A	00h	
PERFORMANCE ENHANCE MODE RESET	N/A	FFh	1
IDENTIFICATION Operations			
READ ID	9E/9Fh	9Fh	
MULTIPLE I/O READ ID	AFh	AFh	
READ ELECTRONICS SIGNATURE	N/A	ABh	
READ MAN & DEV ID	N/A	90h	
READ SERIAL FLASH DISCOVERY PARAMETER	5Ah	5Ah	
READ Operations			
READ	03h	03h	
FAST READ	0Bh	0Bh	
DUAL OUTPUT FAST READ	3Bh	3Bh	
DUAL INPUT/OUTPUT FAST READ	BBh	BBh	
QUAD OUTPUT FAST READ	6Bh	6Bh	
QUAD INPUT/OUTPUT FAST READ	EBh	EBh or EAh	
FAST_READ.DTR	0Dh	N/A	
DUAL OUTPUT FAST READ DTR	3Dh	N/A	
DUAL INPUT/OUTPUT FAST READ DTR	BDh	N/A	
QUAD OUTPUT FAST READ DTR	6Dh	N/A	
QUAD INPUT/OUTPUT FAST READ DTR	EDh	N/A	
4-BYTE ADDRESS MODE Operations			
ENTER 4-BYTE ADDRESSING	B7h	B7h	2
EXIT 4-BYTE ADDRESSING	E9h	E9h	
4-BYTE READ	13h	13h	
4-BYTE FAST_READ	0Ch	0Ch	
4-BYTE DUAL OUTPUT FAST READ	3Ch	3Ch	
4-BYTE DUAL INPUT/OUTPUT FAST READ	BCh	BCh	
4-BYTE QUAD OUTPUT FAST READ	6Ch	6Ch	
4-BYTE QUAD INPUT/OUTPUT FAST READ	ECh	ECh	
4-BYTE Page Program	12h	12h	3
4 BYTE Quad Page Program	34h	3Eh	3
4-BYTE Sector Erase – 64KB	DCh	DCh	3
4-BYTE Sector Erase – 32KB	N/A	5C	

Table 4: Command Set (Continued)

Command	Command Code N25Q	Command Code MX25L25635F	Notes
4-BYTE Sub-Sector Erase – 4KB	21h	21h	3
WRITE Operations			
WRITE ENABLE	06h	06h	
WRITE DISABLE	04h	04h	
Register Operations			
READ STATUS REGISTER	05h	05h	
WRITE STATUS REGISTER	01h	01h	
READ LOCK REGISTER	E8h	2Dh	
WRITE LOCK REGISTER	E5h	2Ch	
READ FLAG STATUS REGISTER	70h	N/A	
CLEAR FLAG STATUS REGISTER	50h	N/A	4
READ NONVOLATILE CONFIGURATION REGISTER	B5h	N/A	
WRITE NONVOLATILE CONFIGURATION REGISTER	B1h	N/A	
READ VOLATILE CONFIGURATION REGISTER	85h	N/A	
WRITE VOLATILE CONFIGURATION REGISTER	81h	N/A	
READ ENHANCED VOLATILE CONFIGURATION REGISTER	65h	N/A	
WRITE ENHANCED VOLATILE CONFIGURATION REGISTER	61h	N/A	
READ EXTENDED ADDRESS REGISTER	C8h	C8h	
WRITE EXTENDED ADDRESS REGISTER	C5h	C5h	
Misc. Operations			
READ SECURITY REGISTER	N/A	2Bh	
WRITE SECURITY REGISTER	N/A	2Fh	
READ CONFIGURATION REGISTER	N/A	15h	
AUTOBOOT REGISTER READ	N/A	16h	
AUTOBOOT REGISTER WRITE	N/A	17h	
AUTOBOOT REGISTER ERASE	N/A	18h	
PPB LOCK BIT WRITE	N/A	A6h	
PPB LOCK BIT READ	N/A	A7h	
DYB READ	N/A	E0h	
DYB WRITE	N/A	E1h	
PPB READ	N/A	E2h	
PPB PROGRAM	N/A	E3h	
PPB ERASE	N/A	E4h	
PASSWORD READ	N/A	27h	
PASSWORD PROGRAM	N/A	28h	
PASSWORD UNLOCK	N/A	29h	
WRITE PROTECTION SELECTION	N/A	68h	

Table 4: Command Set (Continued)

Command	Command Code N25Q	Command Code MX25L25635F	Notes
SET BURST LENGTH	N/A	C0h	
GANG BLOCK LOCK	N/A	7Eh	
GANG BLOCK UN-LOCK	N/A	98h	
PROGRAM Operations			
PAGE PROGRAM	02h	02h	
DUAL INPUT FAST PROGRAM	A2h	N/A	
EXTENDED DUAL INPUT FAST PROGRAM	D2h	N/A	
QUAD INPUT FAST PROGRAM	32h	N/A	
EXTENDED QUAD INPUT FAST PROGRAM	12h/38h	38h	5
ERASE Operations			
BULK ERASE	C7h	60h or C7h	
SECTOR ERASE – 64KB	D8h	D8h	6
SECTOR ERASE – 32KB	N/A	52h	
SUB-SECTOR ERASE – 4KB	20h	20h	6
PROGRAM/ERASE SUSPEND	75h	B0h	
PROGRAM/ERASE RESUME	7Ah	30h	
ONE-TIME PROGRAMMABLE (OTP) Operations			
READ OTP ARRAY	4Bh	4Bh	
PROGRAM OTP ARRAY	42h	42h	
ENTER SECURE OTP	N/A	B1h	7
EXIT SECURE OTP	N/A	C1h	7
DEEP POWER-DOWN			
DEEP POWER-DOWN	B9h	B9h	8
RELEASE FROM DEEP POWER-DOWN	ABh	ABh	8
QUAD Operations			
ENTER QUAD	35h	35h	3
EXIT QUAD	F5h	F5h	3

Notes:
1. Execution in place (XIP) device reset. For the N25Q device, FFh sequence is used to exit from DUAL or QUAD protocol (see XIP and Protocol Exiting Algorithm (page 11)).
2. The MX25L device also sets addressing protocol by volatile bit BAR<7>; the N25Q device does the same by NVCR<0> or with the ENTER 4BYTE ADDRESS command.
3. Available for part numbers N25Q256A83ESF40x and N25Q256A83E1240x only.
4. Program/erase error bits are cleared by CLEAR FLAG STATUS REGISTER on the N25Q device; the MX25L device does the same in status register 1.
5. 38h is available for part numbers N25Q256A83ESF40x and N25Q256A83E1240x only.
6. The N25Q device requires that 4-byte addressing be enabled by opcode or default at power-up (NVCR) before the command.
7. These commands are not necessary for enabling access to the OTP array (64KB instead of 4KB, such as in the MX25 device). The N25Q device is featured with READ OTP/PROGRAM OTP.

8. DEEP POWER-DOWN operation is available on N25Q 1.8V devices only.

Table 5: Different Commands Sharing Same Command Code

Command	N25Q 256Mb Command	MX25L25635F Command	Notes
ABh	RELEASE FROM DEEP POWER-DOWN	RELEASE FROM DEEP POWER-DOWN and READ ELECTRONIC SIGATURE	
12h	EXTENDED QUAD INPUT FAST PROGRAM	4-BYTE PAGE PROGRAM	1
B1h	WRITE NVCR	ENTER SECURE OTP	
20h	Manufacturer ID (9Fh)	Memory Type (90h)	

Note: 1. The sharing of this command is not valid for N25Q256A83ESF40x and N25Q256A83E1240x devices.

READ Commands

The READ/FAST READ command set for the N25Q and MX25L devices is identical and each device follows the standard three- and four-address byte protocol.

Both the N25Q and MX25L devices have configurable dummy cycles. MX25L dummy cycles can be configured by configuration register bits 7 and 8; N25Q dummy cycles can be configured by nonvolatile configuration register bits 12–15 or by volatile configuration register bits 7–4. N25Q also offers DTR FAST READ commands.

Quad commands are available without any register setting in extended SPI protocol for N25Q, while MX25L requires Quad enable bit setting via the WRSR command.

Quad I/O SPI protocol is available in both devices (refer to the N25Q data sheet for more details); N25Q can enter or exit this protocol via VECR or NVCR settings (when power-up is configurable); MX25L can enter or exit via dedicated opcode (power-up always in SPI mode).

Table 6: Minimum Number of Dummy Cycles Required per Each Frequency

Frequency	FAST READ		DUAL OUTPUT FAST READ		DUAL I/O FAST READ		QUAD OUTPUT FAST READ		QUAD I/O FAST READ	
MHz	N25Q	MX25L	N25Q	MX25L	N25Q	MX25L	N25Q	MX25L	N25Q	MX25L
≤50	1	6	1	6	1	4	2	6	3	4
≤80	1	6	1	6	3	4	4	6	6	6
≤90	1	6	2	6	4	6	4	8	8	8
≤104	3	6	4	6	6	6	6	8	9	8
≤133	–	10	–	10	–	10	–	10	–	10

Notes:
1. The MX25L device does not utilize double transfer rate (DTR).
2. To configure Performance Enhance Mode in the MX25L device (Execute-in-Place [XIP] in the N25Q device), configure two dummy clock cycles, as shown in the table above. (The N25Q device requires 1 clock cycle for XIP.)

Power-Up Commands

The MX25L device has two power-up limitations: power-up requires a certain V_{CC} slope and it must stay within the V_{CC} rise time specification (^{t}VR). The N25Q device has no power-up limitation and can speed up the power-on sequence.

Execute-in-Place (XIP)

The N25Q device enters and exits XIP via volatile and non-volatile configuration register settings. The non-volatile configuration register sets XIP mode at power-on of the device. Once enabled, XIP management in the N25Q matches that of the Macronix XIP usage mode. Macronix uses two confirmation nibbles to enter or exit XIP mode. The solution is fully compatible with the N25Q XIP methodology; other bits are don't care. The table below compares XIP read configuration at power-on for both devices.

Table 7: XIP Mode at Power-On

Read Configuration	N25Q	MX25L
FAST READ	Yes	N/A
DUAL OUTPUT FAST READ	Yes	N/A
DUAL I/O FAST READ	Yes	N/A
QUAD OUTPUT FAST READ	Yes	N/A
QUAD I/O FAST READ	Yes	Yes

Figure 1: XIP Timing Configuration

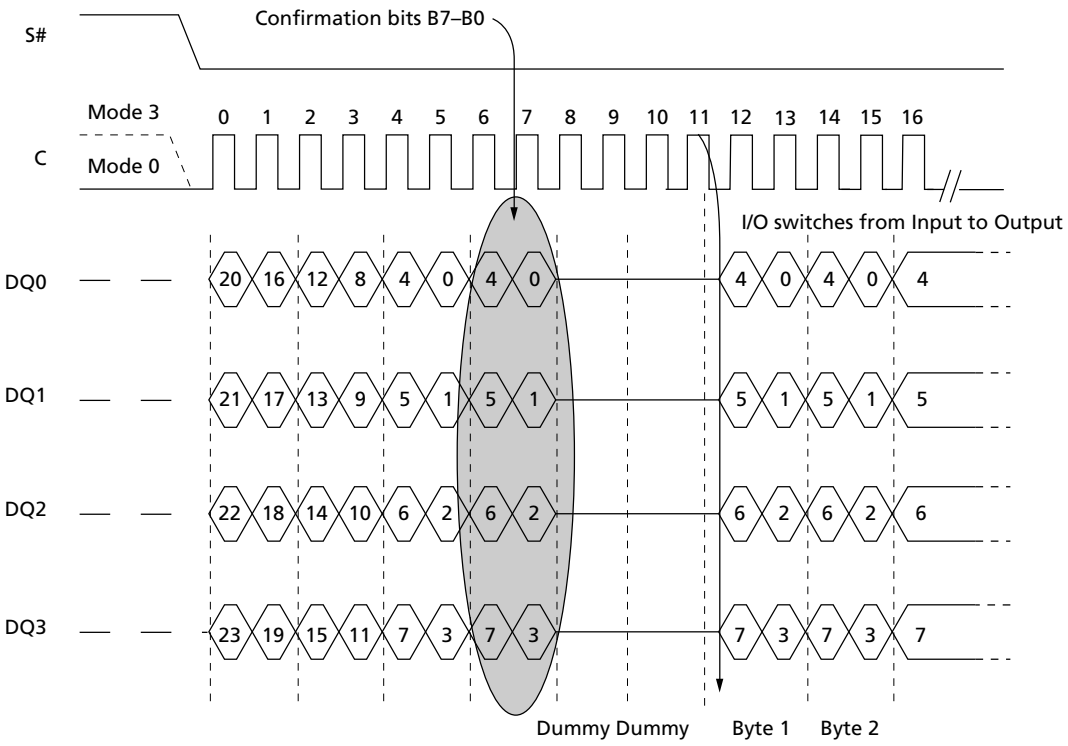


Table 8: XIP Confirmation Bit Software Commands

XIP Confirmation Bit	N25Q	MX25L
Enter/confirm XIP mode	B4 = 0 (B7–B5 and B3–B0 = "Don't Care")	B7 ≠ B3 and B6 ≠ B2 and B5 ≠ B1 and B4 ≠ B0
Exit XIP mode	B4 = 1 (B7–B5 and B3–B0 = "Don't Care")	B7 = B3 or B6 = B2 or B5 = B1 or B4 = B0

XIP and Protocol Exiting Algorithm

For MX25L and N25Q devices, XIP mode and all memory and registers can be reset by the RESET# pin. If you only want to reset XIP mode for Macronix devices, using command FFh for N25Q, use the following procedure:

Note: This procedure is required because, when power loss occurs, the device may start in an indeterminate state (XIP or an unnecessary protocol).

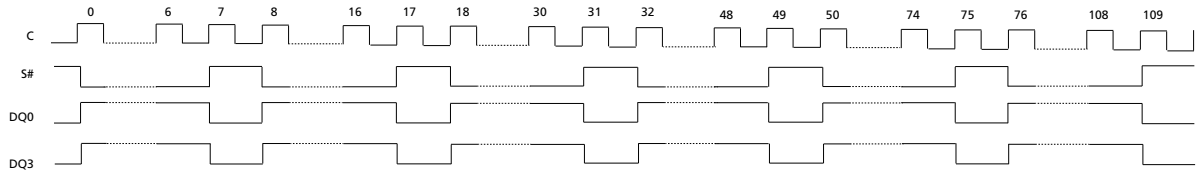
1. Perform the XIP exiting sequence.
2. Perform the dual SPI protocol exiting sequence.

Note: During execution of the WRITE NONVOLATILE CONFIGURATION REGISTER command, ^{t}SHSL2 must be at least 50ns.

XIP Exiting Sequence

Below is the RESET sequence for all possible XIP configurations (QUAD I/O, DUAL I/O, and FAST READ).

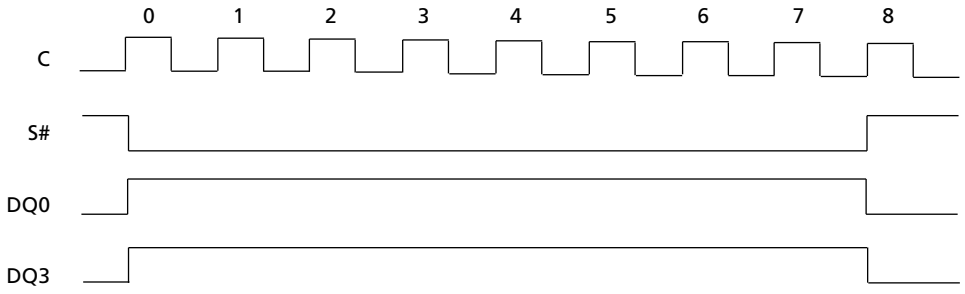
Figure 2: XIP Exiting Sequence



SPI Protocol Exiting Sequence

Exit from DUAL or QUAD SPI protocol using the following FFh sequence.

Figure 3: Dual SPI Protocol Exiting Sequence



Electrical Characteristics

Table 9: DC Current Characteristics

Parameter	Symbol	N25Q		MX25L		Unit
		Min	Max	Min	Max	
Standby current	I_{CC1}	–	100	–	60	µA
Operating current (FAST READ QUAD I/O)	I_{CC3}	–	20	–	20	mA
Operating current (PAGE PROGRAM)	I_{CC4}	–	20	–	25	mA
Operating current (WRITE STATUS REGISTER)	I_{CC5}	–	20	–	20	mA
Operating current (ERASE)	I_{CC6}	–	20	–	25	mA

Table 10: DC Voltage Specifications

Parameter	Symbol	N25Q		MX25L		Unit
		Min	Max	Min	Max	
Input low voltage	V_{iL}	-0.5	0.3 V_{CC}	-0.5	0.8	V
Input high voltage	V_{iH}	0.7 V_{CC}	V_{CC} + 0.4	0.8 V_{CC}	V_{CC} +0.4	V
Output low voltage	V_{OL}	–	0.4	–	0.2	V
Output high voltage	V_{OH}	V_{CC} -0.2	–	V_{CC} -0.2	–	V

AC Characteristics

Table 11: AC Specifications

AC specifications compare the fastest versions available at the full voltage range (2.7-3.6V).

Parameter	Symbol	Alternate Symbol	N25Q		MX25L		Unit
			Min	Max	Min	Max	
Clock frequency (x1 FAST READ)	^{f}C	^{f}C	–	108	–	133	MHz
Clock frequency (x2, x4 FAST READ)	^{f}C	^{f}C	–	108	–	84	MHz
Clock frequency (READ)	^{f}R	^{f}R	–	54	-	50	MHz
S# active setup time	$^{t}SLCH$	^{t}CSS	4	–	5	–	ns
Data-in setup time	$^{t}DVCH$	^{t}DSU	2	–	2	–	ns
Data-in hold time	$^{t}CHDX$	^{t}DH	3	–	4	–	ns
S# deselect time after correct READ (ARRAY READ to ARRAY READ)	$^{t}SHSL1$	^{t}CSH	20	–	7	–	ns
S# deselect time after incorrect READ or different instruction (ERASE/PROGRAM to READ)	$^{t}SHSL2$	^{t}CSH	50	–	30	–	ns
Output disable time (2.7 - 3.6V)	$^{t}SZQZ$	^{t}DIS	–	8	–	8	ns
Clock low to output valid (30pF)	$^{t}CLQV$	^{t}V	–	7	–	8	ns
Output hold time	$^{t}CLQX$	^{t}HO	1	-	1	-	ns
HOLD to output Low-Z	$^{t}HHQZ$	^{t}LZ	N/A	8	N/A	N/A	ns
HOLD to output High-Z	$^{t}HLQZ$	^{t}HZ	N/A	8	N/A	N/A	ns

Program and Erase Specifications

Table 12: Program and Erase Specifications

Operation	N25Q		MX25L		Unit
	Typ	Max	Typ	Max	
PAGE PROGRAM (256 bytes)	0.4	5	0.6	3	ms
4KB SUBSECTOR ERASE	0.25	0.8	0.043	0.2	s
64KB SECTOR ERASE	0.7	3	0.34	2	s
BULK ERASE	240	480	120	300	s

Configuration and Memory Map

Table 13: Sectors and Subsectors

Sector	Subsector	Address Range	
		Start	End
511	8191	01FF F000h	01FF FFFFh
	:	:	:
	8176	01FF 0000h	01FF 0FFFh
:	:	:	:
255	4095	00FF F000h	00FF FFFFh
	:	:	:
	4080	00FF 0000h	00FF 0FFFh
:	:	:	:
127	2047	007F 0000h	007F 0FFFh
	:	:	:
	2032	007F 0000h	007F 0FFFh
:	:	:	:
63	1023	003F F000h	003F FFFh
	:	:	:
	1008	003F 0000h	003F 0FFFh
:	:	:	:
0	15	0000 F000h	0000 FFFFh
	:	:	:
	0	0000 0000h	0000 0FFFh

Device Identification

Manufacturer identification is assigned by JEDEC. As a result, the N25Q and MX25L devices have a different manufacturer ID and memory type code even though their memory capacity is identical. Command 9Fh is used to read the codes in both devices.

N25Q has a unique ID (UID) composed of 17 read-only bytes, which contain the following data:

- The first byte is set to 10h.
- The next two bytes of extended device ID specify device configuration (top, bottom, or uniform architecture and hold or reset functionality).
- The next 14 bytes contain optional customized factory data. The customized factory data bytes are factory programmed. Refer to the N25Q 256Mb data sheet for more information.

Table 14: Read Identification Summary

Parameter	N25Q Code	MX25L Code
Manufacturer ID	20h	C2h
Memory type	BAh	20h
Memory capacity	19h (256Mb)	19h

Part Numbers

Micron Part Number	Macronix Part Number[1]	Package	Secure	Media	Note
N25Q256A13E1240E	N/A	T-PBGA	No	Tray	2
N25Q256A13E1240F	N/A	T-PBGA	No	Tape & Reel	
N25Q256A13E1241E	N/A	T-PBGA	Yes	Tray	
N25Q256A13E1241F	N/A	T-PBGA	Yes	Tape & Reel	
N25Q256A83E1240E	N/A	T-PBGA	No	Tray	
N25Q256A83E1240F	N/A	T-PBGA	No	Tape & Reel	
N25Q256A83E1241E	N/A	T-PBGA	Yes	Tray	
N25Q256A83E1241F	N/A	T-PBGA	Yes	Tape & Reel	
N25Q256A13EF840E	MX25L25635FZ2I-10G	V-PDFN-8	No	Tray	
N25Q256A13EF840F	MX25L25635FZ2I-10G	V-PDFN-8	No	Tape & Reel	
N25Q256A13ESF40F	MX25L25635FMI-10G	SO16 Wide	No	Tray	
N25Q256A13ESF40G	MX25L25635FMI-10G	SO16 Wide	No	Tube	
N25Q256A13ESFA0F	N/A	SO16 Wide	No	Tape & Reel	3
N25Q256A13ESFH0F	N/A	SO16 Wide	No	Tape & Reel	
N25Q256A83ESF40F	MX25L25635FMI-10G	SO16 Wide	No	Tape & Reel	4
N25Q256A83ESF40G	MX25L25635FMI-10G	SO16 Wide	No	Tube	

Notes:
1. All available Macronix devices have a clock frequency of 104 Mhz MAX.
2. T-PBGA package not available with Macronix devices.
3. Automotive test for Micron. (No difference for Macronix devices.)
4. RESET# pin for Micron devices.

Conclusion

Comparing features of the Micron N25Q 256Mb and MX25L25635F Flash memory devices enables users to migrate applications from the MX25L to the N25Q 256Mb device.

Revision History

Rev. C – 11/12

- Updated Memory Array Architecture section
- Updated Signal Descriptions section
- Updated Commands section
- Replaced Reset Algorithm section with XIP and Protocol Exiting Algorithm section
- Updated electrical, AC characteristics, and program and erase specifications
- Added Part Numbers section

Rev. B – 7/12

- Updated note 1 in Table 4: Command Set
- Updated N25Q QUAD OUTPUT FAST READ values in Table 6: Minimum Number of Dummy Cycles Required per Each Frequency
- Updated Table 7: XIP Mode at Power-On
- Added Reset Algorithm section

Rev. A – 5/12

- Initial release

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