MICROCHIP

3V
Tips ‘n Tricks

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Tips ‘N Tricks Introduction

NOTES:

TIPS ‘N TRICKS INTRODUCTION

The 3.3 volt to 5 volt connection.

Overview

One of the by-products of our ever increasing need for processing speed is the steady reduction in the size of the transistors used to build microcontrollers. Up-integration at cheaper cost also drives the need for smaller geometries. With reduced size comes a reduction in the transistor breakdown voltage, and ultimately, a reduction in the supply voltage when the breakdown voltage falls below the supply voltage. So, as speeds increase and complexity mounts, it is an inevitable consequence that the supply voltages would drop from 5V to 3.3V, or even 1.8V for high density devices.

Microchip microcontrollers have reached a sufficient level of speed and complexity that they too are making the transition to sub-5V supply voltages. The challenge is that most of the interface circuitry is still designed for 5V supplies. This means that, as designers, we now face the task of interfacing 3.3V and 5V systems. Further, the task includes not only logic level translation, but also powering the 3.3V systems and translating analog signals across the 3.3V/5V barrier.

This Tips ‘n Tricks book addresses these challenges with a collection of power supply building blocks, digital level translation blocks and even analog translation blocks. Throughout the book, multiple options are presented for each of the transitions, spanning the range from all-in-one interface devices, to low-cost discrete solutions. In short, all the blocks a designer is likely to need for handling the 3.3V challenge, whether the driving force is complexity, cost or size.

Note: The tips ‘n tricks presented here assume a 3.3V supply. However, the techniques work equally well for other supply voltages with the appropriate modifications.

Power Supplies

One of the first 3.3V challenges is generating the 3.3V supply voltage. Given that we are discussing interfacing 5V systems to 3.3V systems, we can assume that we have a stable 5 VDC supply. This section will present voltage regulator solutions designed for the 5V to 3.3V transition. A design with only modest current requirements may use a simple linear regulator. Higher current needs may dictate a switching regulator solution. Cost sensitive applications may need the simplicity of a discrete diode regulator. Examples from each of these areas are included here, with the necessary support information to adapt to a wide variety of end applications.

TABLE -1: POWER SUPPLY COMPARISONS

Method	V_{REG}	I_Q	Eff.	Size	Cost	Transient Response
Zener Shun Reg.	10% Typ	5 mA	60%	Sm	Low	Poor
Series Linear Reg.	0.4% Typ	1 µA to 100 µA	60%	Sm	Med	Excellent
Switching Buck Reg.	0.4% Typ	30 µA to 2 mA	93%	Med to Lg	High	Good

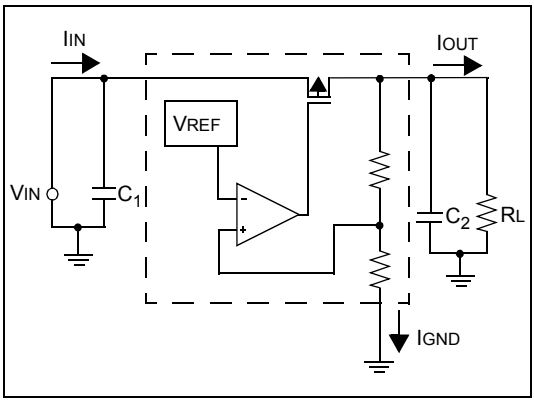
TIP #1 Powering 3.3V Systems From 5V Using an LDO Regulator

The dropout voltage of standard three-terminal linear regulators is typically 2.0-3.0V. This precludes them from being used to convert 5V to 3.3V reliably. Low Dropout (LDO) regulators, with a dropout voltage in the few hundred milli-volt range, are perfectly suited for this type of application. Figure 1-1 contains a block diagram of a basic LDO system with appropriate current elements labeled. From this figure it can be seen that an LDO consists of four main elements:

1. pass transistor
2. bandgap reference
3. operational amplifier
4. feedback resistor divider

When selecting an LDO, it is important to know what distinguishes one LDO from another. Device quiescent current, package size and type are important device parameters. Evaluating for each parameter for the specific application yields an optimal design.

FIGURE 1-1: LDO VOLTAGE REGULATOR

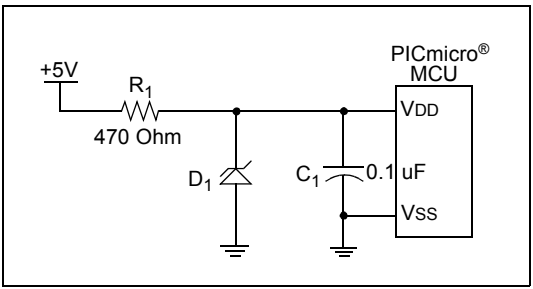


An LDOs quiescent current, IQ, is the device ground current, IGND, while the device is operating at no load. IGND is the current used by the LDO to perform the regulating operation. The efficiency of an LDO can be approximated as the output voltage divided by the input voltage when IOUT>>IQ. However, at light loads, the IQ must be taken into account when calculating the efficiency. An LDO with lower IQ will have a higher light load efficiency. This increase in light load efficiency has a negative effect on the LDO performance. Higher quiescent current LDOs are able to respond quicker to sudden line and load transitions.

TIP #2 Low-Cost Alternative Power System Using a Zener Diode

Details a low-cost regulator alternative using a Zener diode.

FIGURE 2-1: ZENER SUPPLY



A simple, low-cost 3.3V regulator can be made out of a Zener diode and a resistor as shown in Figure 2-1. In many applications, this circuit can be a cost-effective alternative to using a LDO regulator. However, this regulator is more load sensitive than a LDO regulator. Additionally, it is less energy efficient, as power is always being dissipated in R_1 and D_1.

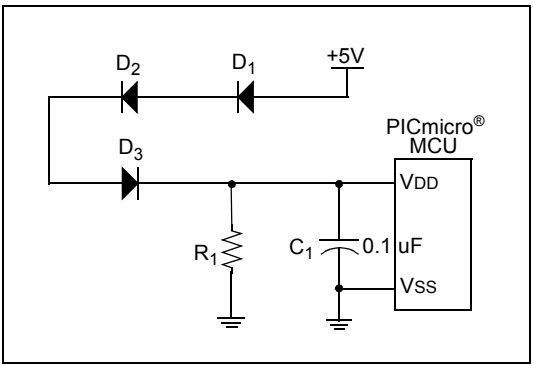
R_1 limits the current to D_1 and the PICmicro® MCU so that V_{DD} stays within the allowable range. Because the reverse voltage across a Zener diode varies as the current through it changes, the value of R_1 needs to be considered carefully.

R_1 must be sized so that at maximum load, typically when the PICmicro MCU is running and is driving its outputs high, the voltage drop across R_1 is low enough so that the PICmicro MCU has enough voltage to operate. Also, R_1 must be sized so that at minimum load, typically when the PICmicro MCU is in Reset, that V_{DD} does not exceed either the Zener diode’s power rating or the maximum V_{DD} for the PICmicro MCU.

TIP #3 Lower Cost Alternative Power System Using 3 Rectifier Diodes

Figure 3-1 details a lower cost regulator alternative using 3 rectifier diodes.

FIGURE 3-1: DIODE SUPPLY



We can also use the forward drop of a series of normal switching diodes to drop the voltage going into the PICmicro MCU. This can be even more cost-effective than the Zener diode regulator. The current draw from this design is typically less than a circuit using a Zener.

The number of diodes needed varies based on the forward voltage of the diode selected. The voltage drop across diodes D_1-D_3 is a function of the current through the diodes. R_1 is present to keep the voltage at the PICmicro MCUs V_{DD} pin from exceeding the PICmicro MCUs maximum V_{DD} at minimum loads (typically when the PICmicro MCU is in Reset or sleeping). Depending on the other circuitry connected to V_{DD}, this resistor may have its value increased or possibly even eliminated entirely. Diodes D_1-D_3 must be selected so that at maximum load, typically when the PICmicro is running and is driving its outputs high, the voltage drop across D_1-D_3 is low enough to meet the PICmicro MCUs minimum V_{DD} requirements.

TIP #4 Powering 3.3V Systems From 5V Using Switching Regulators

A buck switching regulator, shown in Figure 4-1, is an inductor-based converter used to step-down an input voltage source to a lower magnitude output voltage. The regulation of the output is achieved by controlling the ON time of MOSFET Q1. Since the MOSFET is either in a lower or high resistive state (ON or OFF, respectively), a high source voltage can be converted to a lower output voltage very efficiently.

The relationship between the input and output voltage can be established by balancing the volt-time of the inductor during both states of Q1.

$$(V_s - V_o) * t_{on} = V_o * (T - t_{on})$$

Where: $T \equiv t_{on} / Duty\_Cycle$

It therefore follows that for MOSFET Q1:

$$Duty\_Cycle_{Q1} = V_o / V_s$$

When choosing an inductor value, a good starting point is to select a value to produce a maximum peak-to-peak ripple current in the inductor equal to ten percent of the maximum load current.

$$V = L * (di/dt)$$

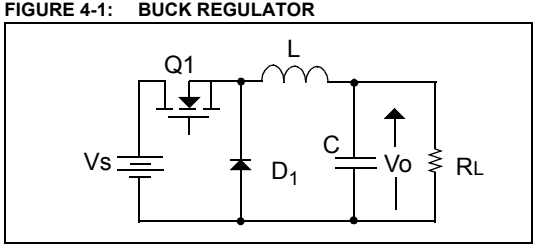
$$L = (V_s - V_o) * (t_{on} / I_o * 0.10)$$

When choosing an output capacitor value, a good starting point is to set the LC filter characteristic impedance equal to the load resistance. This produces an acceptable voltage overshoot when operating at full load and having the load abruptly removed.

$$Z_o \equiv \sqrt{L/C}$$
$$C = L/R^2 = (I_o^2 * L)/V_o^2$$

When choosing a diode for D_1, choose a device with a sufficient current rating to handle the inductor current during the discharge part of the pulse cycle (I_L).

FIGURE 4-1: BUCK REGULATOR



Digital Interfacing

When interfacing two devices that operate at different voltages, it is imperative to know the output and input thresholds of both devices. Once these values are known, a technique can be selected for interfacing the devices based on the other requirements of your application. Table 4-1 contains the output and input thresholds that will be used throughout this document. When designing an interface, make sure to reference your manufacturers data sheet for the actual threshold levels.

TABLE 4-1: INPUT/OUTPUT THRESHOLDS

	V_{OH} min	V_{OL} max	V_{IH} min	V_{IL} max
5V TTL	2.4V	0.5V	2.0V	0.8V
3.3V LVTTL	2.4V	0.4V	2.0V	0.8V
5V CMOS	4.7V (Vcc-0.3V)	0.5V	3.5V (0.7xVcc)	1.5V (0.3xVcc)
3.3V LVCMOS	3.0V (Vcc-0.3V)	0.5V	2.3V (0.7xVcc)	1.0V (0.3xVcc)

TIP #5 3.3V → 5V Direct Connect

The simplest and most desired way to connect a 3.3V output to a 5V input is by a direct connection. This can be done only if the following 2 requirements are met:

- The V_{OH} of the 3.3V output is greater than the V_{IH} of the 5V input
- The V_{OL} of the 3.3V output is less than the V_{IL} of the 5V input

An example of when this technique can be used is interfacing a 3.3V LVCMOS output to a 5V TTL input. From the values given in Table 4-1, it can clearly be seen that both of these requirements are met.

3.3V LVCMOS V_{OH} of 3.0 volts is greater than 5V TTL V_{IH} of 2.0 volts

and

3.3V LVCMOS V_{OL} of 0.5 volts is less than 5V TTL V_{IL} of 0.8 volts.

When both of these requirements are not met, some additional circuitry will be needed to interface the two parts. See Tips 6, 7, 8 and 13 for possible solutions.

TIP #6 3.3V → 5V Using a MOSFET Translator

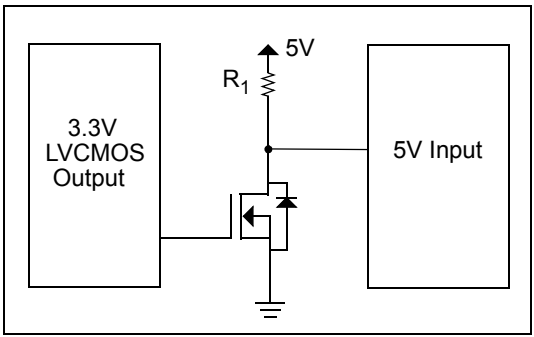
In order to drive any 5V input that has a higher V_{IH} than the V_{OH} of a 3.3V CMOS part, some additional circuitry is needed. A low-cost two component solution is shown in Figure 6-1.

When selecting the value for R_1, there are two parameters that need to be considered; the switching speed of the input and the current consumption through R_1. When switching the input from a '0' to a '1', you will have to account for the time the input takes to rise because of the RC time constant formed by R_1, and the input capacitance of the 5V input plus any stray capacitance on the board. The speed at which you can switch the input is given by the following:

$$T_{SW} = 3 \times R_1 \times (C_{IN} + C_S)$$

Since the input and stray capacitance of the board are fixed, the only way to speed up the switching of the input is to lower the resistance of R_1. The trade-off of lowering the resistance of R_1 to get faster switching times is the increase in current draw when the 5V input remains low. The switching to a '0' will typically be much faster than switching to a '1' because the ON resistance of the N-channel MOSFET will be much smaller than R_1. Also, when selecting the N-channel FET, select a FET that has a lower V_{GS} threshold voltage than the V_{OH} of 3.3V output.

FIGURE 6-1: MOSFET TRANSLATOR



TIP #7 3.3V → 5V Using A Diode Offset

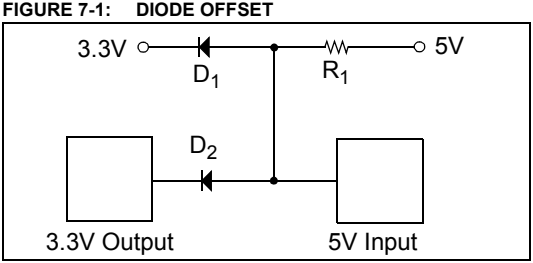
The inputs voltage thresholds for 5V CMOS and the output drive voltage for 3.3V LVTTL and LVCMOS are listed in Table 7-1.

TABLE 7-1: INPUT/OUTPUT THRESHOLDS

	5V CMOS Input	3.3V LVTTL Output	3.3V LVCMOS Output
High Threshold	> 3.5V	> 2.4V	> 3.0V
Low Threshold	< 1.5V	< 0.4V	< 0.5V

Note that both the high and low threshold input voltages for the 5V CMOS inputs are about a volt higher than the 3.3V outputs. So, even if the output from the 3.3V system could be offset, there would be little or no margin for noise or component tolerance. What is needed is a circuit that offsets the outputs and increases the difference between the high and low output voltages.

FIGURE 7-1: DIODE OFFSET



When output voltage specifications are determined, it is done assuming that the output is driving a load between the output and ground for the high output, and a load between 3.3V and the output for the low output. If the load for the high threshold is actually between the output and 3.3V, then the output voltage is actually much higher as the load resistor is the mechanism that is pulling the output up, instead of the output transistor.

If we create a diode offset circuit (see Figure 7-1), the output low voltage is increased by the forward voltage of the diode D_1, typically 0.7V, creating a low voltage at the 5V CMOS input of 1.1V to 1.2V. This is well within the low threshold input voltage for the 5V CMOS input. The output high voltage is set by the pull-up resistor and diode D_2, tied to the 3.3V supply. This puts the output high voltage at approximately 0.7V above the 3.3V supply, or 4.0 to 4.1V, which is well above the 3.5V threshold for the 5V CMOS input.

Note: For the circuit to work properly, the pull-up resistor must be significantly smaller than the input resistance of the 5V CMOS input, to prevent a reduction in the output voltage due to a resistor divider effect at the input. The pull-up resistor must also be large enough to keep the output current loading on the 3.3V output within the specification of the device.

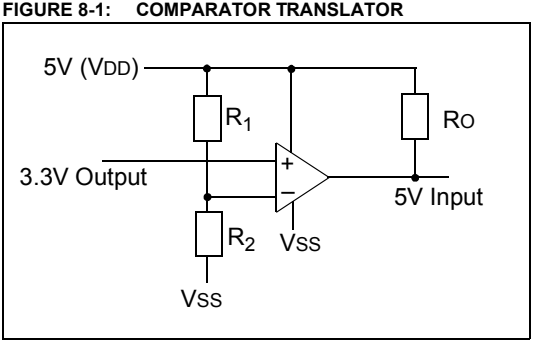
TIP #8 3.3V → 5V Using A Voltage Comparator

The basic operation of the comparator is as follows:

- When the voltage at the inverting (-) input is greater than that at the non-inverting (+) input, the output of the comparator swings to Vss.
- When the voltage at the non-inverting (+) input is greater than that at the non-inverting (-) input, the output of the comparator is in a high state.

To preserve the polarity of the 3.3V output, the 3.3V output must be connected to the non-inverting input of the comparator. The inverting input of the comparator is connected to a reference voltage determined by R_1 and R_2, as shown in Figure 8-1.

FIGURE 8-1: COMPARATOR TRANSLATOR



Calculating R_1 and R_2

The ratio of R_1 and R_2 depends on the logic levels of the input signal. The inverting input should be set to a voltage halfway between V_{OL} and V_{OH} for the 3.3V output. For an LVCMOS output, this voltage is:

$$1.75V = \frac{(3.0V + .5V)}{2}$$

Given that R_1 and R_2 are related by the logic levels,

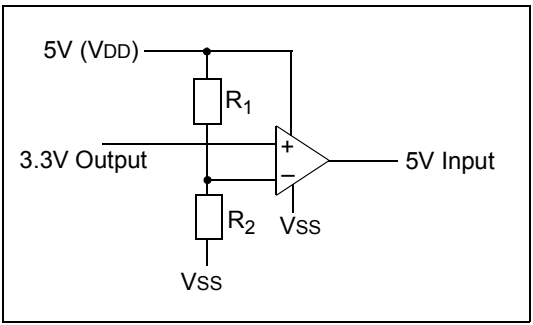
$$R_1 = R_2 \left(\frac{5V}{1.75V} - 1\right)$$

assuming a value of 1K for R_2, R_1 is 1.8K.

An op amp wired up as a comparator can be used to convert a 3.3V input signal to a 5V output signal. This is done using the property of the comparator that forces the output to swing high (V_{DD}) or low (Vss), depending on the magnitude of difference in voltage between its ‘inverting’ input and ‘non-inverting’ input.

Note: For the op amp to work properly when powered by 5V, the output must be capable of rail-to-rail drive.

FIGURE 8-2: OP AMP AS A COMPARATOR

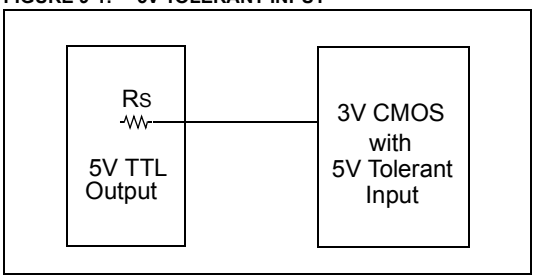


TIP #9 5V – 3.3V Direct Connect

5V outputs have a typical V_{OH} of 4.7 volts and a V_{OL} of 0.4 volts and a 3.3V LVCMOS input will have a typical V_{IH} of 0.7 x V_{DD} and a V_{IL} of 0.2 x V_{DD}.

When the 5V output is driving low, there are no problems because the 0.4 volt output is less than in the input threshold of 0.8 volts. When the 5V output is high, the V_{OH} of 4.7 volts is greater than 2.1 volt V_{IH}, therefore, we can directly connect the 2 pins with no conflicts **if the 3.3V CMOS input is 5 volt tolerant**.

FIGURE 9-1: 5V TOLERANT INPUT



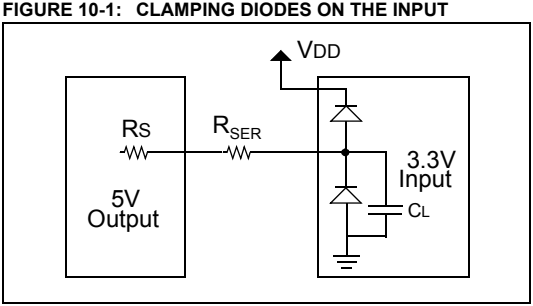
If the 3.3V CMOS input is not 5 volt tolerant, then there will be an issue because the maximum volt specification of the input will be exceeded.

See Tips 10-13 for possible solutions.

TIP #10 5V → 3.3V With Diode Clamp

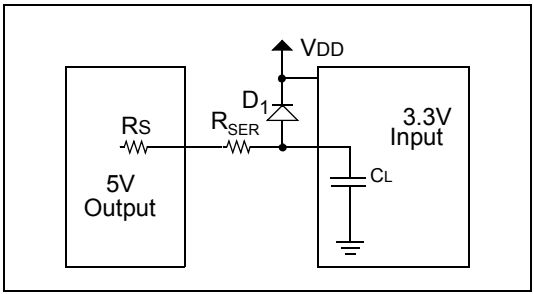
Many manufacturers protect their I/O pins from exceeding the maximum allowable voltage specification by using clamping diodes. These clamping diodes keep the pin from going more than a diode drop below Vss and a diode drop above VDD. To use the clamping diode to protect the input, you still need to look at the current through the clamping diode. The current through the clamp diodes should be kept small (in the micro amp range). If the current through the clamping diodes gets too large, then you risk the part latching up. Since the source resistance of a 5V output is typically around 10 ohms, an additional series resistor is still needed to limit the current through the clamping diode as shown Figure 10-1. The consequence of using the series resistor is it will reduce the speed at which we can switch the input because the RC time constant formed the capacitance of the pin (CL).

FIGURE 10-1: CLAMPING DIODES ON THE INPUT



If the clamping diodes are not present, a single external diode can be added to the circuit as shown in Figure 10-2.

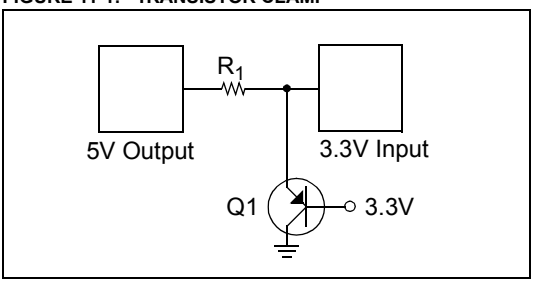
FIGURE 10-2: WITHOUT CLAMPING DIODES



TIP #11 5V → 3.3V Active Clamp

One problem with using a diode clamp is that it injects current onto the 3.3V power supply. In designs with a high current 5V outputs, and lightly loaded 3.3V power supply rails, this injected current can float the 3.3V supply voltage above 3.3V. To prevent this problem, a transistor can be substituted which routes the excess output drive current to ground instead of the 3.3V supply. Figure 11-1 shows the resulting circuit.

FIGURE 11-1: TRANSISTOR CLAMP

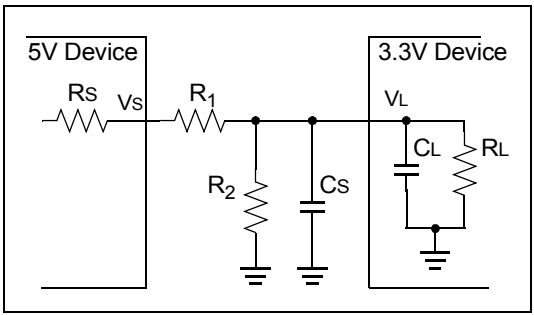


The base-emitter junction of Q1 performs the same function as the diode in a diode clamp circuit. The difference is that only a small percentage of the emitter current flows out of the base of the transistor to the 3.3V rail, the bulk of the current is routed to the collector where it passes harmlessly to ground. The ratio of base current to collector current is dictated by the current gain of the transistor, typically 10-400, depending upon which transistor is used.

TIP #12 5V → 3.3V Resistor Divider

A simple resistor divider can be used to reduce the output of a 5V device to levels appropriate for a 3.3V device input. An equivalent circuit of this interface is shown in Figure 12-1.

FIGURE 12-1: RESISTIVE INTERFACE EQUIVALENT CIRCUIT



Typically, the source resistance, RS, is very small (less than 10 ohms) so its affect on R_1 will be negligible provided that R_1 is chosen to be much larger than RS. At the receive end, the load resistance, RL, is very large (greater than 500 k ohms) so its affect on R_2 will be negligible provided that R_2 is chosen to be much less than RL.

There is a trade-off between power dissipation and transition times. To keep the power requirements of the interface circuit at a minimum, the series resistance of R_1 and R_2 should be as large as possible. However, the load capacitance, which is the combination of the stray capacitance, CS, and the 3.3V device input capacitance, CL, can adversely affect the rise and fall times of the input signal. Rise and fall times can be unacceptably long if R_1 and R_2 are too large.

Neglecting the affects of RS and RL, the formula for determining the values for R_1 and R_2 is given by Equation 12-1.

EQUATION 12-1: DIVIDER VALUES

$$\frac{V_S}{R1 + R2} = \frac{V_L}{R2} \quad \text{; General relationship}$$

$$R1 = \frac{(V_S - V_L) \cdot R2}{V_L} \quad \text{; Solving for } R_1$$

$$R1 = 0.515 \cdot R2 \quad \text{; Substituting voltages}$$

The formula for determining the rise and fall times is given in Equation 12-2. For circuit analysis, the Thevenin equivalent is used to determine the applied voltage, V_A, and the series resistance, R. The Thevenin equivalent is defined as the open circuit voltage divided by the short circuit current. The Thevenin equivalent, R, is determined to be $0.66*R_1$ and the Thevenin equivalent, V_A, is determined to be $0.66*V_S$ for the circuit shown in Figure 12-2 according to the limitations imposed by Equation 12-2.

EQUATION 12-2: RISE/FALL TIME

$$t = -\left[R \cdot C \cdot \ln\left(\frac{V_F - V_A}{V_I - V_A}\right)\right]$$

Where:

- t = Rise or Fall time
- R = $0.66*R_1$
- C = C_S+C_L
- V_I = Initial voltage on C (V_L)
- V_F = Final voltage on C (V_L)
- V_A = Applied voltage ($0.66*V_S$)

As an example, suppose the following conditions exist:

- Stray capacitance = 30 pF
- Load capacitance = 5 pF
- Maximum rise time from 0.3V to 3V ≤ 1 μS
- Applied source voltage Vs = 5V

The calculation to determine the *maximum* resistances is shown in Equation 12-3.

EQUATION 12-3: EXAMPLE CALCULATION

Solve Equation 12-2 for R:

$$R = -\left[\frac{t}{C \cdot \ln\left(\frac{V_F - V_A}{V_I - V_A}\right)}\right]$$

Substitute values:

$$R = -\left[\frac{10 \cdot 10^{-7}}{35 \cdot 10^{-12} \cdot \ln\left(\frac{3 - (0.66 \cdot 5)}{0.3 - (0.66 \cdot 5)}\right)}\right]$$

Thevenin equivalent maximum R:

$$R = 12408$$

Solve for maximum R_1 and R_2:

$$R1 = 0.66 \cdot R \qquad R2 = \frac{R1}{0.515}$$

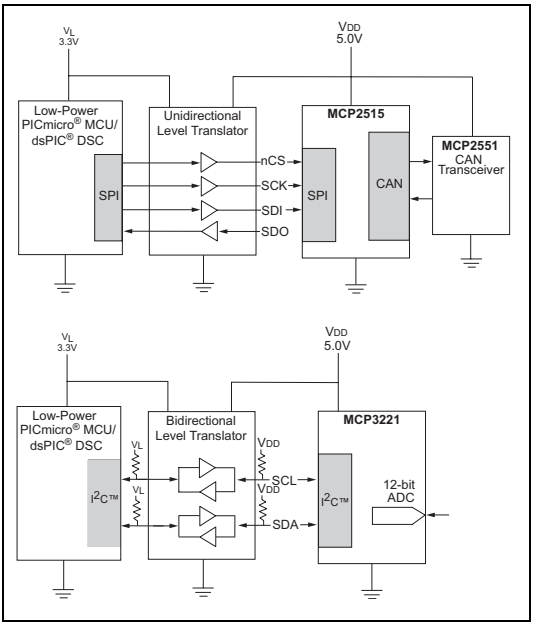
$$R1 = 8190 \qquad R2 = 15902$$

TIP #13 3.3V → 5V Level Translators

While level translation can be done discretely, it is often preferred to use an integrated solution. Level translators are available in a wide range of capabilities. There are unidirectional and bidirectional configurations, different voltage translations and different speeds, all giving the user the ability to select the best solution.

Board-level communication between devices (e.g., MCU to peripheral) is most often done by either SPI or $I^2C^{™}$. For SPI, it may be appropriate to use a unidirectional level translator and for I^2C, it is necessary to use a bidirectional solution. Figure 13-1 below illustrates both solutions.

FIGURE 13-1: LEVEL TRANSLATOR



Analog

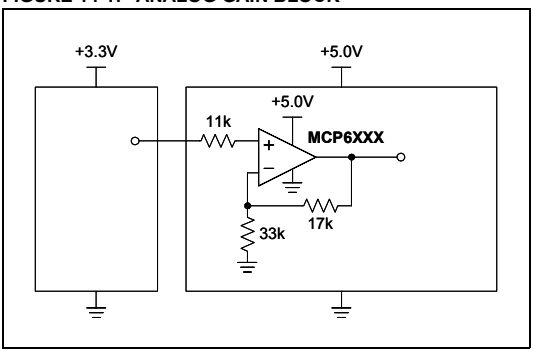
The final 3.3V to 5V interface challenge is the translation of analog signals across the power supply barrier. While low level signals will probably not require external circuitry, signals moving between 3.3V and 5V systems will be affected by the change in supply. For example, a 1V peak analog signal converted by an ADC in a 3.3V system will have greater resolution than an ADC in a 5V system, simply because more of the ADCs range is used to convert the signal in the 3.3V ADC. Alternately, the relatively higher signal amplitude in a 3.3V system may have problems with the system’s lower common mode voltage limitations.

Therefore, some interface circuitry, to compensate for the differences, may be needed. This section will discuss interface circuitry to help alleviate these problems when the signal makes the transition between the different supply voltages.

TIP #14 3.3V → 5V Analog Gain Block

To scale analog voltage up when going from 3.3V supply to 5V supply. The 33 kΩ and 17 kΩ set the op amp gain so that the full scale range is used in both sides. The 11 kΩ resistor limits current back to the 3.3V circuitry.

FIGURE 14-1: ANALOG GAIN BLOCK

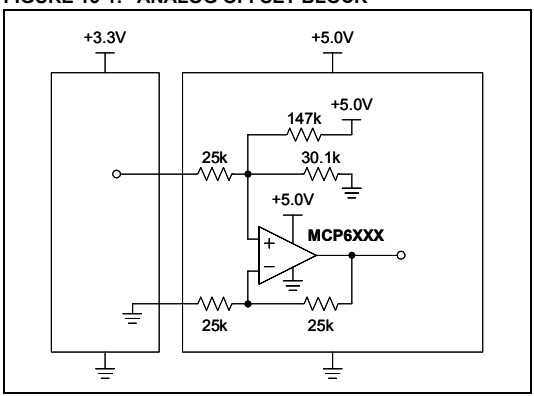


TIP #15 3.3V → 5V Analog Offset Block

Offsetting an analog voltage for translation between 3.3V and 5V.

Shift an analog voltage from 3.3V supply to 5V supply. The 147 kΩ and 30.1 kΩ resistors on the top right and the +5V supply voltage are equivalent to a 0.85V voltage source in series with a 25 kΩ resistor. This equivalent 25 kΩ resistance, the three 25 kΩ resistors, and the op amp form a difference amplifier with a gain of 1 V/V. The 0.85V equivalent voltage source shifts any signal seen at the input up by the same amount; signals centered at 3.3V/2 = 1.65V will also be centered at 5.0V/2 = 2.50V. The top left resistor limits current from the 5V circuitry.

FIGURE 15-1: ANALOG OFFSET BLOCK



TIP #16 5V → 3.3V Active Analog Attenuator

Reducing a signal’s amplitude from a 5V to 3.3V system using an op amp.

The simplest method of converting a 5V analog signal to a 3.3V analog signal is to use a resistor divider with a ratio R_1:R_2 of 1.7:3.3. However, there are a few problems with this.

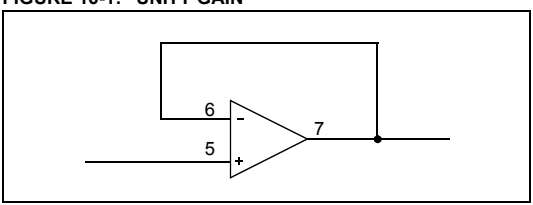
1) The attenuator may be feeding a capacitive load, creating an unintentional low pass filter.

2) The attenuator circuit may need to drive a low-impedance load from a high-impedance source.

Under either of these conditions, an op amp becomes necessary to buffer the signals.

The op amp circuit necessary is a unity gain follower (see Figure 16-1).

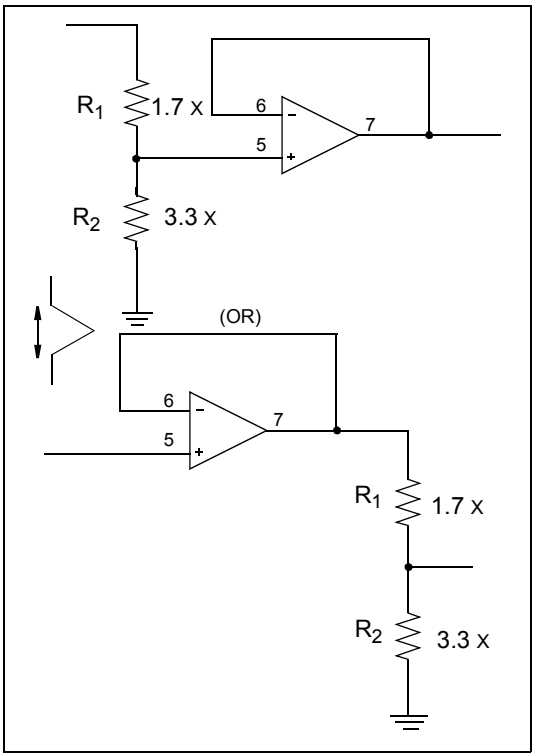
FIGURE 16-1: UNITY GAIN



This circuit will output the same voltage that is applied to the input.

To convert the 5V signal down to a 3V signal, we simply add the resistor attenuator.

FIGURE 16-2: OP AMP ATTENUATORS



If the resistor divider is before the unity gain follower, then the lowest possible impedance is provided for the 3.3V circuits. Also, the op amp can be powered from 3.3V, saving some power. If the X is made very large, then power consumed by the 5V side can be minimized.

If the attenuator is added after the unity gain follower, then the highest possible impedance is presented to the 5V source. The op amp must be powered from 5V and the impedance at the 3V side will depend upon the value of $R_1||R_2$.

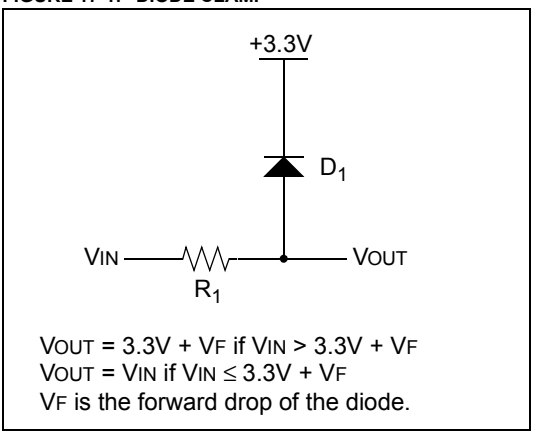
TIP #17 5V → 3V Analog Limiter

When moving a 5V signal down to a 3.3V system, it is sometimes possible to use the attenuation as gain. If the desired signal is less than 5V, then attaching that signal to a 3.3V ADC will result in larger conversion values. The danger is when the signal runs to the 5V rail. A method is therefore required to control the out-of-range voltages while leaving the in-range voltages unaffected. Three ways to accomplish this will be discussed here.

1. Using a diode to clamp the overvoltage to the 3.3V supply.
2. Using a Zener diode to clamp the voltage to any desired limit.
3. Using an op amp with a diode to perform a precision clamp.

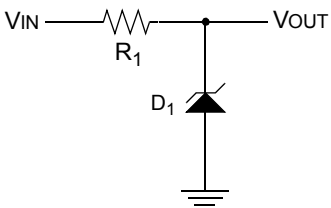
The simplest method to perform the overvoltage clamp is identical to the simple method of interfacing a 5V digital signal to the 3.3V digital signals. A resistor and a diode are used to direct excess current into the 3.3V supply. The resistor must be sized to protect the diode and the 3.3V supply while not adversely affecting the analog performance. If the impedance of the 3.3V supply is too low, then this type of clamp can cause the 3.3V supply voltage to increase. Even if the 3.3V supply has a good low-impedance, this type of clamp will allow the input signal to add noise to the 3.3V supply when the diode is conducting and if the frequency is high enough, even when the diode is not conducting due to the parasitic capacitance across the diode.

FIGURE 17-1: DIODE CLAMP



To prevent the input signal from affecting the supply or to make the input more robust to larger transients, a variation is to use a Zener diode. The Zener diode is slower than the fast signal diode typically used in the first circuit. However, they are generally more robust and do not rely on the characteristics of the power supply to perform the clamping. The amount of clamping they provide is dependant upon the current through the diode. This is set by the value of R_1. R_1 may not be required if the output impedance of the V_{IN} source is sufficiently large.

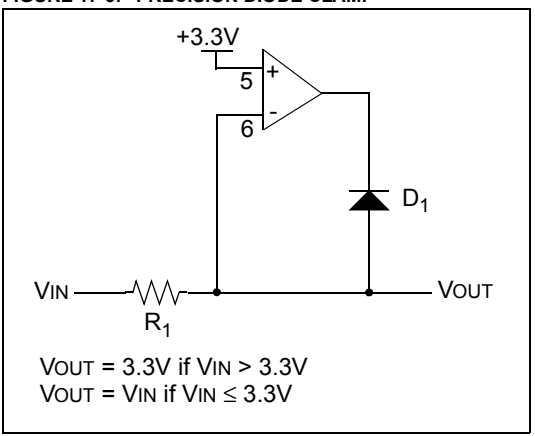
FIGURE 17-2: ZENER CLAMP



$V_{OUT} = V_{BR}$ if $V_{IN} > V_{BR}$
$V_{OUT} = V_{IN}$ if $V_{IN} \leq V_{BR}$
V_{BR} is the reverse breakdown voltage of the Zener diode.

If a more precise overvoltage clamp is required that does not rely upon the supply, then an op amp can be employed to create a precision diode. In Figure 17-3, such a circuit is shown. The op amp compensates for the forward drop in the diode and causes the voltage to be clamped at exactly the voltage supplied on the non-inverting input to the op amp. The op amp can be powered from 3.3V if it is rail-to-rail.

FIGURE 17-3: PRECISION DIODE CLAMP

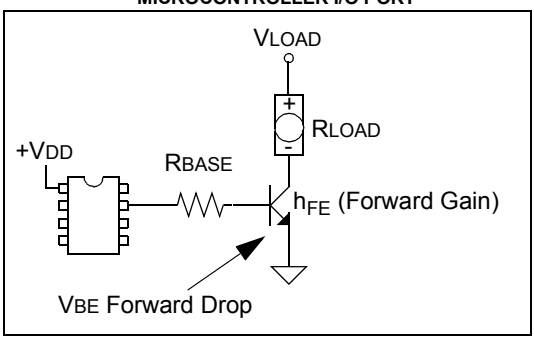


Because the clamping is performed by the op amp, there is no affect on the power supply. The impedance presented to the low voltage circuit is not improved by the op amp, it remains R_1 in addition to the source circuit impedance.

TIP #18 Driving Bipolar Transistors

When driving Bipolar transistors, the amount of base current “drive” and forward current gain (B/hFE) will determine how much current the transistor can sink. When driven by a microcontroller I/O port, the base drive current is calculated using the port voltage and the port current limit (typically 20 mA). When using 3.3V technology, smaller value base current limiting resistors should be used to ensure sufficient base drive to saturate the transistor.

FIGURE 18-1: DRIVING BIPOLAR TRANSISTORS USING MICROCONTROLLER I/O PORT



The value of RBASE will depend on the microcontroller supply voltage. Equation 18-1 describes how to calculate RBASE.

TABLE 18-1: BIPOLAR TRANSISTOR DC SPECIFICATIONS

Characteristic	Sym	Min	Max	Unit	Test Condition
OFF CHARACTERISTICS					
Collector-Base Breakdown voltage	$V_{(BR)CBO}$	60	—	V	I_C = 50 μA, I_E = 0
Collector-Emitter Break-down Voltage	$V_{(BR)CEO}$	50	—	V	I_C = 1.0 mA, I_B = 0
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	7.0	—	V	I_E = 50 μA, I_C = 0
Collector Cutoff Current	I_{CBO}	—	100	nA	V_{CB} = 60V
Emitter Cutoff Current	I_{EBO}	—	100	nA	V_{EB} = 7.0V
ON CHARACTERISTICS					
DC Current Gain	h_{FE}	120 180 270	270 390 560	—	V_{CE} = 6.0V, I_C = 1.0 mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	—	0.4	V	I_C = 50 mA, I_B = 5.0 mA

When using bipolar transistors as switches to turn on and off loads controlled by the microcontroller I/O port pin, use the minimum h_{FE} specification and margin to ensure complete device saturation.

EQUATION 18-1: CALCULATING THE BASE RESISTOR VALUE

$$R_{BASE} = \frac{(V_{DD} - V_{BE})xh_{FE}xR_{LOAD}}{V_{LOAD}}$$

3V technology example:

V_{DD} = +3V, V_{LOAD} = +40V, R_{LOAD} = 400Ω, h_{FE} min. = 180, V_{BE} = 0.7V

R_{BASE} = 4.14 kΩ, I/O port current = 556 µA

5V technology example:

V_{DD} = +5V, V_{LOAD} = +40V, R_{LOAD} = 400Ω, h_{FE} min. = 180, V_{BE} = 0.7V

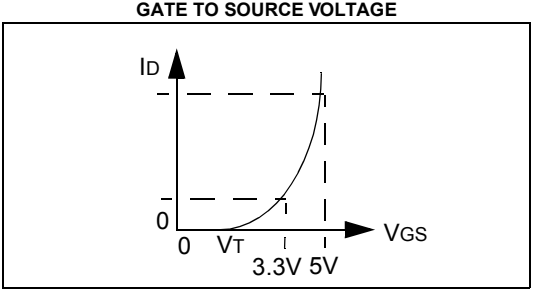
R_{BASE} = 7.74 kΩ, I/O port current = 556 µA

For both examples, it is good practice to increase base current for margin. Driving the base with 1 mA to 2 mA would ensure saturation at the expense of increasing the input power consumption.

TIP #19 Driving N-Channel MOSFET Transistors

Care must be taken when selecting an external N-Channel MOSFET for use with a 3.3V microcontroller. The MOSFET gate threshold voltage is an indication of the device’s capability to completely saturate. For 3.3V applications, select MOSFETs that have an ON resistance rating for gate drive of 3V or less. For example, a FET that is rated for 250 uA of drain current with 1V applied from gate-to-source is not necessarily going to deliver satisfactory results for 100 mA load with a 3.3V drive. When switching from 5V to 3V technology, review the gate-to-source threshold and ON resistance characteristics very carefully as shown in Figure 19-1. A small decrease in gate drive voltage can significantly reduce drain current.

FIGURE 19-1: DRAIN CURRENT CAPABILITY VERSUS GATE TO SOURCE VOLTAGE



Low threshold devices commonly exist for MOSFETs with drain-to-source voltages rated below 30V. MOSFETs with drain-to-source voltages above 30V typically have higher gate thresholds (VT).

TABLE 19-1: RDS(ON) AND VGS(TH) SPECIFICATIONS FOR IRF7467

RDS(on)	Static Drain-to-Source On-Resistance	—	9.4	12	mΩ	VGS = 10V, ID = 11A
		—	10.6	13.5		VGS = 4.5V, ID = 9.0A
		—	17	35		VGS = 2.8V, ID = 5.5A
VGS(th)	Gate Threshold Voltage	0.6	—	2.0	V	VDS = VGS, ID = 250 μA

As shown in Table 19-1, the threshold voltage for this 30V, N-Channel MOSFET switch is 0.6V. The resistance rating for this MOSFET is 35 mΩ with 2.8V applied gate, as a result, this device is well suited for 3.3V applications.

TABLE 19-2: RDS(ON) AND VGS(TH) SPECIFICATIONS FOR IRF7201

RDS(on)	Static Drain-to-Source On-Resistance	—	—	0.030	Ω	VGS = 10V, ID = 7.3A
		—	—	0.050		VGS = 4.5V, ID = 3.7A
VGS(th)	Gate Threshold Voltage	1.0	—	—	V	VDS = VGS, ID = 250 μA

Tips ‘n Tricks

For the IRF7201 data sheet specifications, the gate threshold voltage is specified as a 1.0V minimum. This does not mean the device can be used to switch current with a 1.0V gate-to-source voltage as there is no RDS(ON) specification for V_{GS}(th) values below 4.5V. This device is not recommended for 3.3V drive applications that require low switch resistance but can be used for 5V drive applications.

Additional Online Resources can be found:

www.microchip.com/3volts

- Application Notes
- Migration Documents
- 3 Volt Newsletter
- FAQ's

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