DESCRIPTION

The KS57C2616 single-chip 4-bit microcontroller is fabricated using an advanced CMOS process. With an up-to-896-dot LCD direct-drive capability, flexible 8-bit and 16-bit timer/counters, and serial I/O interface, the KS57C2616 offers an excellent design solution for a wide range of applications reguiring LCD support.

FEATURES

Memory

- 736 x 4-bit RAM
- 16,384 x 8-bit ROM

39 I/O Pins

- I/O: 35 pins
- Input only: 4 pins

Memory-Mapped I/O Structure

- Data memory bank 15

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

LCD Controller/Driver

- 56 segments and 16 common terminals
- 8 and 16 common selectable
- Internal resistor circuit for LCD bias
- All dots can be switched on/off

8-Bit Basic Timer

- Four interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer/event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer/event counter
- Arbitrary clock output
- External clock signal divider

Watch Timer

- Timer intervals: 0.5 s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Bit Sequential Carrier

- 16-bit serial data transfer in arbitrary format

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (4, 8, 64)

Instruction Execution Times

- 0.95 μs, 1.91 μs, 15.3 μs at 4.19 MHz (main)
- 122 μs at 32.768 kHz (subsystem)

Operating Temperature Range

- – 40 °C to 85 °C

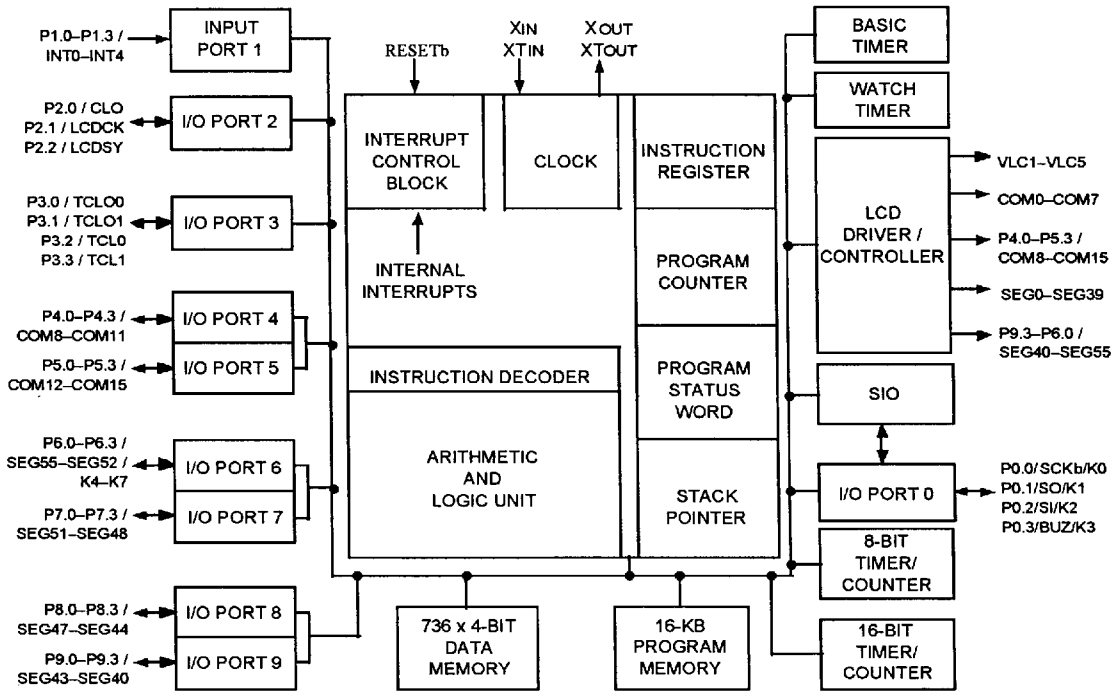
Operating Voltage Range

- 2.7 V to 6.0 V

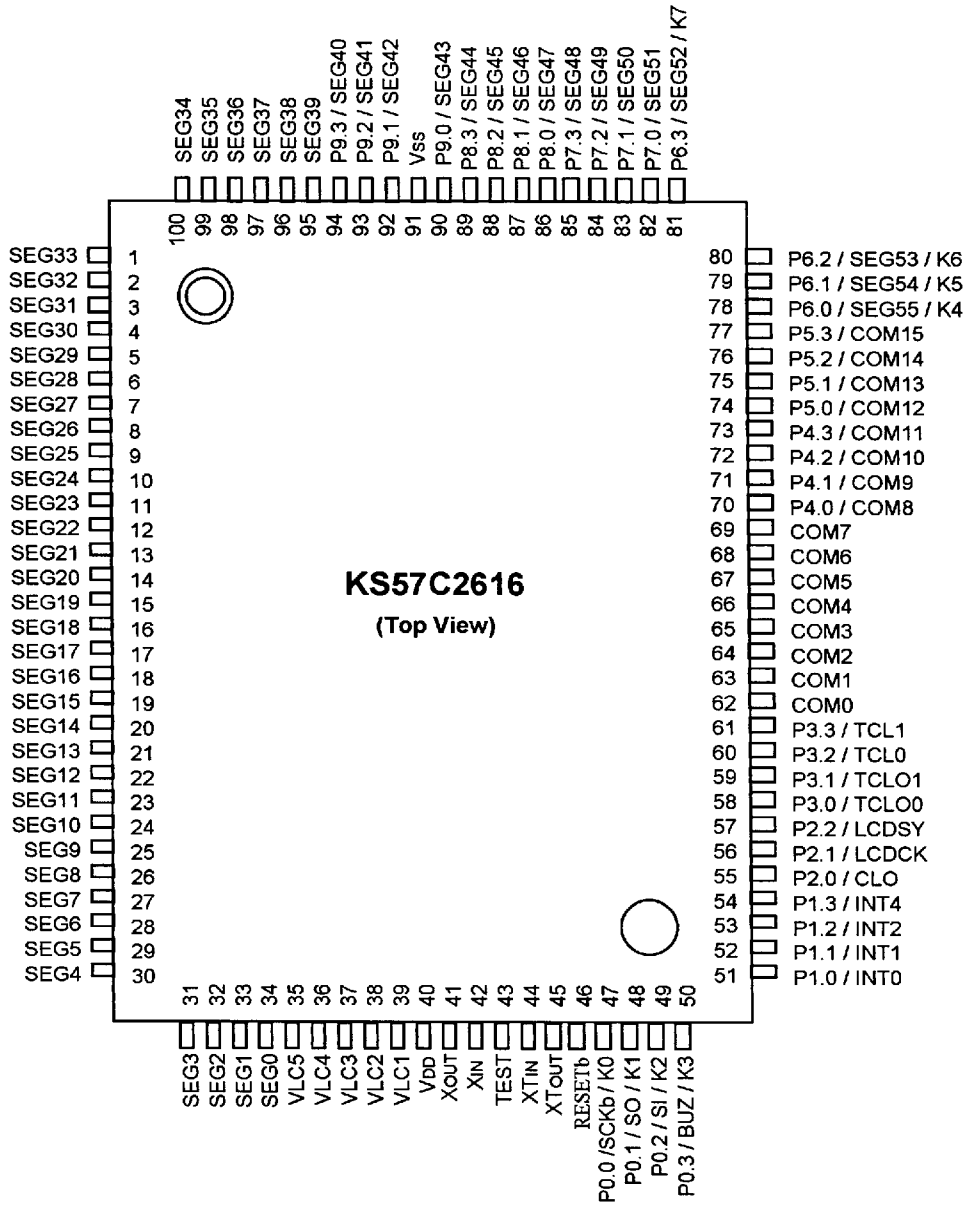
Package Type

- 100-pin QFP

BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN DESCRIPTIONS

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is supported. Individual pins are software configurable as inputs or as n-channel, open-drain or push-pull outputs. 4-bit pull-up resistors are software assignable. (Pull-ups are automatically disabled for output pins.)	47 48 49 50	SCKb/K0 SO/K1 SI/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is supported. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2 only.	51 52 53 54	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2	I/O	Same as port 0 except that port 2 is a 3-bit port.	55 56 57	CLO LCDCK LCDSY
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	58 59 60 61	TCLO0 TCLO1 TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-bit, 4-bit, or 8-bit read/write and test is supported. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable. (Pull-ups are automatically disabled for output pins.)	70–73 74–77	COM8–COM11 COM12–COM15
P6.0–P6.3 P7.0–P7.3	I/O	Same as ports 4 and 5.	78–81 82–85	SEG55/K4–SEG52/K7 SEG51–SEG48
P8.0–P8.3 P9.0–P9.3	I/O	Same as ports 4 and 5.	86–89 90, 92–94	SEG47–SEG44 SEG43–SEG40
SCKb	I/O	Serial I/O interface clock signal	47	P0.0/K0
SO	I/O	Serial data output	48	P0.1/K1
SI	I/O	Serial data input	49	P0.2/K2
BUZ	I/O	2-kHz, 4-kHz, 8-kHz or 16-kHz frequency output for buzzer sound	50	P0.3/K3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	51, 52	P1.0, P1.1
INT2	I	Quasi-interrupt with rising/falling edge detection	53	P1.2
INT4	I	External interrupt with rising/falling edge detection	54	P1.3

PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
CLO	I/O	Clock output	55	P2.0
LCDCK	I/O	LCD clock output for display expansion	56	P2.1
LCDSY	I/O	LCD synchronization clock output for display expansion	57	P2.2
TCLO0	I/O	Timer/counter 0 clock output	58	P3.0
TCLO1	I/O	Timer/counter 1 clock output	59	P3.1
TCL0	I/O	External clock input for timer/counter 0	60	P3.2
TCL1	I/O	External clock input for timer/counter 1	61	P3.3
COM0–COM7	O	LCD common signal output	62–69	–
COM8–COM11	I/O		70–73	P4.0–P4.3
COM12–COM15			74–77	P5.0–P5.3
SEG0–SEG39	O	LCD segment signal output	34–1, 100–95	–
SEG40–SEG43	I/O		94–92, 90	P9.3–P9.0
SEG44–SEG47			89–86	P8.3–P8.0
SEG48–SEG51			85–82	P7.3–P7.0
SEG52–SEG55			81–78	P6.3/K7–P6.0/K4
K0–K3	I/O	External interrupt (triggering edge is selectable)	47–50	P0.0–P0.3
K4–K7			78–81	P6.0–P6.3
V_{DD}	–	Main power supply	40	–
V_{SS}	–	Ground	91	–
RESETb	I	System RESETb input pin	46	–
V_{LC1}–V_{LC5}	–	LCD power supply	39–35	–
X_{IN}, X_{OUT}	–	Crystal, ceramic, or RC oscillator pins for system clock	42, 41	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock	44, 45	–
TEST	I	Test signal input (must be connected to V_{SS})	43	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

FUNCTION OVERVIEW

SAM4 CPU

All KS57-series microcontrollers have the advanced SAM4 CPU core. The SAM4 CPU can directly address up to 32 K bytes of program memory. The arithmetic logic unit (ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle. Most 8-bit arithmetic and logical operations execute in two cycles.

PROGRAM MEMORY

In its standard configuration, the 16,384 x 8-bit ROM is divided into four functional areas:

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 16-byte and 16,256-byte areas for general-purpose program memory

The REF instruction references 2 ¥ 1-byte and 2-byte instructions stored in locations 0020H–007FH. The REF instruction can also reference three-byte instructions such as JP or CALL. So that a REF instruction can reference these instructions, JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name. Unused locations in the reference area can be used as general-purpose registers.

DATA MEMORY

Overview

Data memory is organized into four areas:

— 32 x 4-bit working register area in bank 0

— 224 x 4-bit general-purpose area in bank 0

— 256 x 4-bit general-purpose area in bank 1

— 224 x 4-bit area for LCD data in bank 2

Data Memory Addressing Modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0,1 , 2 or 15 When the EMB flag is logic zero, restricted area can be accessed. When the EMB flag is set to logic one, all four data memory banks can be accessed according to the current SMB value.

Working Registers

The RAM's working register area in data memory bank 0 is further divided into four *register* banks. Each register bank has eight 4-bit registers that are addressable either by 1-bit or 4-bit instructions. Paired 4-bit registers can be addressed as double registers by 8-bit instructions.

Register A is the 4-bit accumulator and double register EA is the 8-bit extended accumulator. Double registers WX, WL, and HL are used as data pointers for indirect addressing. Unused working registers can be used as general-purpose memory.

CONTROL REGISTERS

Select Bank (SB) Register

Two 4-bit registers store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

The 'SMB n' instruction selects a data memory bank (0, 1, 2, or 15) and stores the upper four bits of the 12-bit data memory address in the SMB register. To select a register bank and store the address data in the SRB, you use the instruction 'SRB n'.

The instructions "PUSH SB" and "POP SB" move SRB and SMB values to and from the stack for interrupts and subroutines.

INTERRUPTS

Interrupt requests can be generated internally by on-chip processes (INTB, INTT0, INTT1, and INTS) or externally by peripheral devices (INT0, INT1, INT4, and INTK).

There are two quasi-interrupts: INT2 and INTW. INT2 detects rising/falling edges and INTW detects time intervals of 0.5 seconds or 3.19 milliseconds. The following components support interrupt processing:

— Interrupt enable flags

— Interrupt request flags

— Interrupt priority registers

— Power-down release circuit

POWER-DOWN

To reduce power consumption, there are two power-down modes: Idle and Stop. The IDLE instruction initiates Idle mode; the STOP instruction initiates Stop mode.

In Idle mode, the CPU clock stops while peripherals continue to operate normally. In Stop mode, system clock oscillation stops, halting all operations except for a few basic peripheral functions. A power-down is released by a reset or an interrupt.

I/O PORTS

The KS57C2616 has ten ports with four input-only pins and 35 configurable I/O pins, for a total of 39 pins.

OSCILLATOR CIRCUITS

The KS57C2616 microcontroller has two oscillator circuits: a main system clock circuit, and a subsystem clock circuit. The main or subsystem clock frequency can be divided by 4, 8, or 64 by manipulating PCON bits 1 and 0.

The system clock mode control register, SCMOD, lets you select the main system clock (fx) or a subsystem clock (fxt) as the CPU clock and to start or stop main system clock oscillation.

The watch timer, buzzer and LCD display operate normally with a subsystem clock source, as they operate at very slow speeds and with low power consumption (as low as 122 μs at 32.768 kHz.)

TIMERS and TIMER/COUNTERS

The timer function block has four main components: an 8-bit basic interval timer, an 8-bit timer/counter, a 16-bit timer/counter, and a watch timer.

The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected CPU clock frequency.

The programmable 8-bit and 16-bit timer/counters are used for external event counting, generation of arbitrary clock frequencies for output, and dividing external clock signals.

The 8-bit timer/counter is the source of the clock signal that is required to drive the serial I/O interface.

The watch timer has an 8-bit watch timer mode register, a clock selector, and a frequency divider circuit. Its functions include real-time and watch-time measurement, clock generation for the LCD controller, and frequency outputs for buzzer sound.

SERIAL I/O INTERFACE

Using the serial I/O interface, you can exchange 8-bit data with an external device. The serial interface can have an internal or an external clock source, or it can use the TOL0 signal that is generated by the 8-bit timer/counter 0, TC0.

If you use the TOL0 clock signal, you can modify its frequency to adjust the serial data transmission rate.

BIT SEQUENTIAL CARRIER

The bit sequential carrier (BSC) is a 16-bit register that can be manipulated using 1-bit, 4-bit, or 8-bit instructions.

Using 1-bit indirect addressing, addresses and bit locations can be specified sequentially. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register. BSC data can also be manipulated using direct addressing.

LCD CONTROLLER/DRIVER

The KS57C2616 microcontroller can directly drive an up-to-896-dot (56 seg x 16 com) LCD panel.

Data written to the LCD display RAM can be transferred automatically to the segment signal pins. When a subsystem clock is selected as the LCD clock source, the LCD display is enabled, even during Stop and Idle modes.

D.C. ELECTRICAL CHARACTERISTICS

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except as specified for V_{IH2} and V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, P3.2, P3.3, and RESETb	0.8 V_{DD}		V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}, and XT_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except as specified for V_{IL2} and V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, P3.2, P3.3, and RESETb			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, and XT_{IN}			0.4	
Output High Voltage	V_{OH}	V_{DD} = 2.7 V to 6.0 V I_{OH} = – 500 µA Ports 0, 2–9	0.8 V_{DD}	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 2.7 V to 6.0 V I_{OL} = 500 µA Ports 0, 2–9	–	–	0.1 V_{DD}	V
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except as specified for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD} X_{IN}, X_{OUT}, and XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except X_{IN}, X_{OUT}, and XT_{IN}	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V, X_{IN}, X_{OUT}, and XT_{IN}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-up Resistor	R_L	V_I = 0 V; V_{DD} = 5 V ± 10 % Ports 0–9 (except for P1.3)	15	40	80	kΩ
		V_{DD} = 3 V ± 10 %	30	–	200	
LCD Voltage Dividing Resistor	R_{LCD}	V_{DD} = 2.7 V to 6.0 V	25	55	80	kΩ

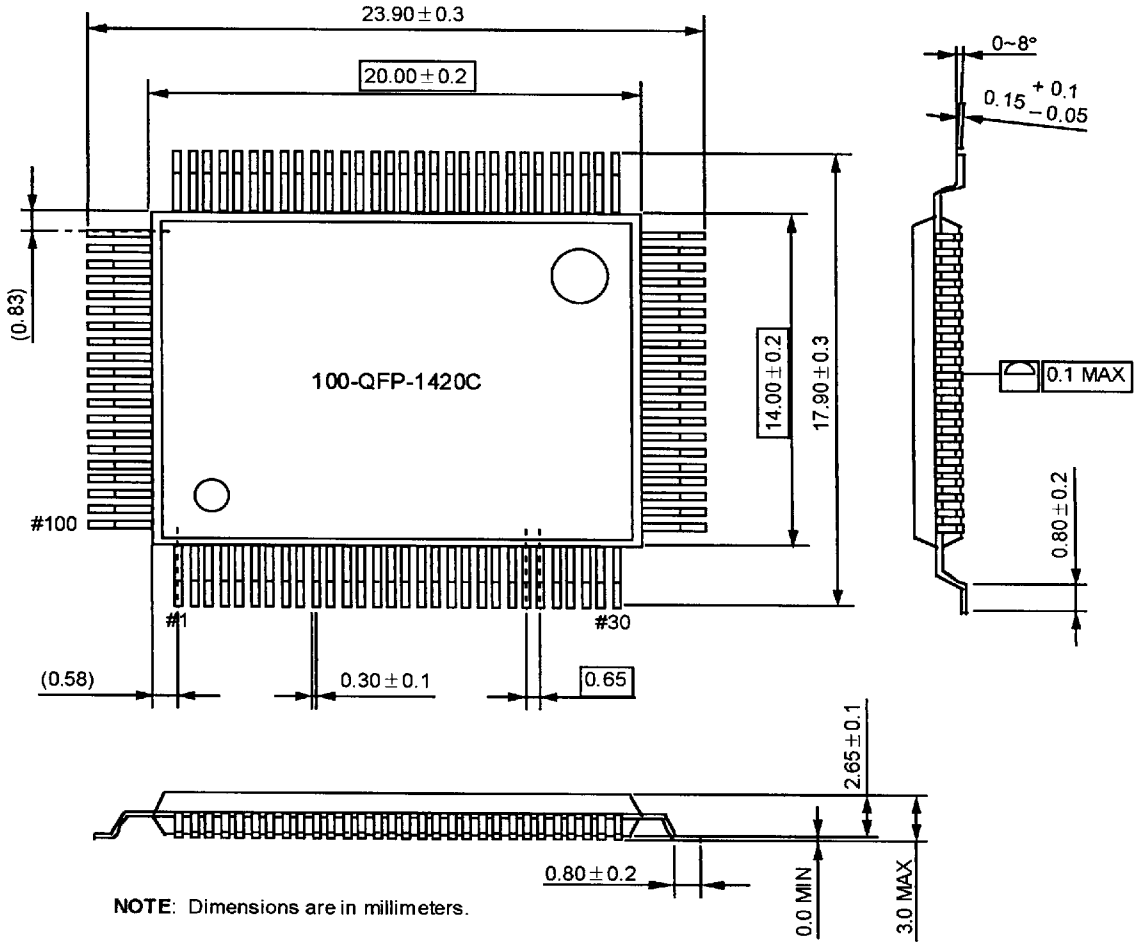
D.C. ELECTRICAL CHARACTERISTICS (Continued)

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
| V_{DD}–COMi | Voltage Drop	V_{DC}	−15 µA per common pin COMi, where i = 0–15	–	–	120	mV
| V_{DD}–SEGx | Voltage Drop	V_{DS}	−15 µA per segment pin SEGx, where x = 0–55	–	–	120	
V_{LC1} Output Voltage	V_{LC1}	V_{DD} = 3.5 V to 6.0 V (1) LCD clock = 0 Hz, V_{LC5} = 0 V	0.8 V_{DD} − 0.15	0.8 V_{DD}	0.8 V_{DD} + 0.15	V
V_{LC2} Output Voltage	V_{LC2}		0.6 V_{DD} − 0.15	0.6 V_{DD}	0.6 V_{DD}+ 0.15	
V_{LC3} Output Voltage	V_{LC3}		0.4 V_{DD} − 0.15	0.4 V_{DD}	0.4 V_{DD}+ 0.15	
V_{LC4} Output Voltage	V_{LC4}		0.2 V_{DD} − 0.15	0.2 V_{DD}	0.2 V_{DD} + 0.15	
Supply Current	I_{DD1} (2)	V_{DD} = 5 V ± 10 % (3) 4.19-MHz crystal oscillator C1 = C2 = 22 pF	–	2.5	8	mA
		V_{DD} = 3 V ± 10 % (4)		0.7	1.2	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10 % 4.19-MHz crystal oscillator C1 = C2 = 22 pF		1.3	1.8	
		V_{DD} = 3 V ± 10 %		0.6	1.0	
	I_{DD3} (5)	V_{DD} = 3 V ± 10 % 32-kHz crystal oscillator	–	15	90	µA
	I_{DD4} (5)	Idle mode; V_{DD} = 3 V ± 10 % 32-kHz crystal oscillator		7	15	
	I_{DD5}	Stop mode; XT_{IN} = 0 V V_{DD} = 5 V ± 10 %		0.7	5	
		V_{DD} = 3 V ± 10 %		0.5	3	

NOTES:
1. In 1/4 bias LCD operation mode, the V_{DD} range is 2.7 V to 6.0 V.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
4. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
5. When the SCMOD register is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

PACKAGE DIMENSIONS



NOTE: Dimensions are in millimeters.