VLSI TECHNOLOGY, INC.

VGT300 SERIES

1.0-MICRON GATE ARRAY SERIES

FEATURES

- Advanced 1.0 micron (drawn) silicon gate technology
- Seven array sizes from 30,300 to 246,500 available gates
- Continuous Gate™ architecture for maximum layout efficiency
- Designed for high-performance logic applications
  - — 350 ps typical internal cell delay
  - — 250 MHz flip-flop toggle frequency
  - — 3.5 ns I/O pair delay
- High reliability: over 2000 Volts ESD pad protection
- Low power consumption: typically 6.5 μW/gate/MHz
- High design productivity with VLSI's advanced compilers and logic synthesis tools
- Technology independence with VLSI Portable Library™
- Wide range of package styles and lead counts to fit demanding system environments

DESCRIPTION

The VGT300 Series of high-performance gate arrays is fabricated on an advanced, dual metal, planarized, fully implanted CMOS process, designed with true 1.0 micron silicon gate design rules. This family utilizes VLSI Technology's proprietary Continuous Gate technology, a special bent-gate architecture that is used to achieve high transistor densities, with a unique global routing scheme to offer high speed and a high integration design approach.

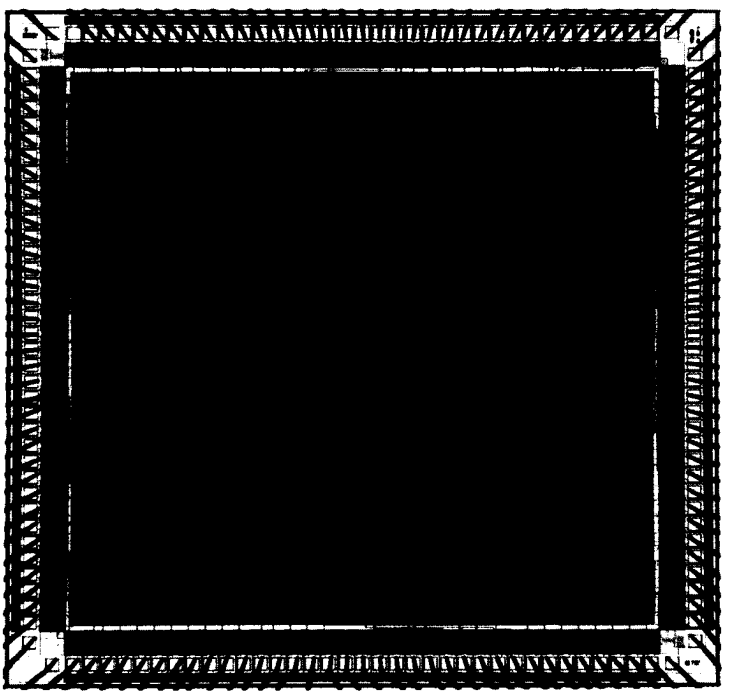
Maximum layout efficiency is achieved in the VGT300 Series, utilizing approximately 30% of the total gates for random logic applications, and up to 75% for memory blocks. With typical effective channel lengths of 0.85 micron and reduced junction area capacitance, the VGT300 gate arrays permit system clock speeds of up to 80 MHz. An internal 2-input NAND gate with a fanout of 2 shows a typical propagation delay of less than 350 picoseconds.

ADVANCED DESIGN TOOLS

The VGT300 Series is fully compatible with the VLSI Portable Library™ and is supported by VLSI's leading-edge ASIC design tools. New capabilities for high-integration, high-performance designs include:

- High-productivity design tools including Logic Synthesizer, datapath, and RAM compilers
- Multi-ASIC simulation and timing analysis
- Interactive floorplanning for better control of chip layout and performance
- Automatic test vector and test program generation including design for testability using SCAN cells and Built In Self-Test (BIST) techniques.
- Distributed RC tree interconnect delay extraction and back-annotation for more accurate timing simulation.

VGT300 DIE PHOTO



VGT300 SERIES GATE ARRAYS

Device Number	Equivalent Gates, Note 1	Estimated Usable Gates, Note 2	Maximum I/O Pads
VGT300030	30,300	9,090	140
VGT300046	46,200	13,860	172
VGT300077	77,400	23,220	220
VGT300110	110,300	33,090	260
VGT300163	163,800	49,140	316
VGT300198	198,800	59,640	348
VGT300246	246,500	73,950	388

ARRAY ORGANIZATION

The general layout of the VGT300 Series consists of electrical components that are organized as structures of continuous arrays of transistor pairs. One or more transistor pairs comprise a macro cell, the basic building blocks of logic design. The same transistor array and I/O cell structures are used in all VGT300 gate arrays, allowing the same macros to be used throughout the VGT300 Series.

The power busing structure of the VGT300 Series is capable of isolating the I/O cells from the internal array. Both the VDD and the VSS buses surround the array in second-level metal and are fed into the internal array through a power rail structure. This power bus structure also allows any pad to be programmed as VDD or VSS.

INTERNAL ARRAY DESCRIPTION

The VGT300 Continuous Gate technology consists of rows of uncommitted P and N transistors, laid out at continuous regular intervals. This internal architecture and global routing scheme provide unique advantages for the VGT300 gate arrays by giving high gate density and gate utilization, as well as faster place and route.

BENT-GATE ARCHITECTURE

A bent-gate architecture allows the poly gate of a device to align with the source and drain area of the transistor, allowing the transistors to be placed two times closer than the traditional channel-free architecture. This compaction minimizes the source and drain areas and greatly reduces stray diffusion capacitance. In addition, source and drain diffusions are metal-strapped, eliminating most diffusion resistance effects, and providing fast gate delays.

GATE ISOLATION

High gate density is achieved through the use of gate isolation, specially contoured poly nodes, and metal-one strapping of source drain diffusion areas. The oxide isolation technique used in traditional approaches isolates active regions from one another by a thick field oxide. In comparison, the gate isolation technique employed in Continuous Gate technology turns off transistors to isolate active regions from one another. Higher silicon efficiency is achieved because the isolation transistors are placed only where needed.

Specially contoured poly nodes are used throughout the array to minimize the vertical metal routing required to connect each of the nodes. This, in turn, allows for more horizontal tracks to be available, thus increasing routing efficiency and silicon utilization.

I/O BUFFERS

A dual power bus structure in the I/O buffer may be used to isolate the output buffer power supply from that of the array core to achieve high noise immunity. Special I/O features are as follows:

- All I/Os are protected against latch-up and static discharge.
- Pullup and pulldown resistors are available for use in combination with each I/O.
- Any I/O location may also be programmed as power or ground.
- The output portion of the I/O buffer contains pre-drive logic as well as programmable output drive.
- The output buffers are designed to source or sink 2, 4, 8, 12, or 16 mA.
- Slew rate control is available for 8, 12 and 16 mA output buffers. This reduces output spike current and system noise by controlling the output rising and falling edge-rate.
- Each input location may be programmed as TTL, CMOS, or Schmitt-Trigger.

Notes:
1. An equivalent gate is defined as one 2-input NAND.
2. Assuming 30% utilization. Actual number of usable gates is design dependent.

ASIC DESIGN TOOLS AND METHODOLOGY

ASIC design tools from VLSI Technology provide all the capabilities necessary for gate array design from concept to silicon. High-level partitioning for single or multiple ASICs allow speed, density, power, and packaging options to be quickly analyzed to determine tradeoffs before detailed design is started. Both top-down and bottom-up design methodologies are supported.

Complex logic and memory functions are efficiently implemented utilizing state of the art compilers. The VLSI Logic Synthesizer creates optimized netlists from random logic or state machine inputs. The Datapath Compiler assists the design of complex bit oriented computational logic such as CPU execution units. The VGTRAM compiler allows implementation of memory on the VGT300 gate array architecture. Support for common design for testability techniques is provided by SCAN cells, a Linear Feedback Shift Registers (LFSR) compiler, Built In Self-Test (BIST) structures for RAMs, and multiplexer isolation for large blocks. The VLSI Clock distribution scheme controls clock skew to no more than 2 ns between any two points on a chip.

An interactive floorplanner allows a designer to place gate array blocks hierarchically. After completion of placement and routing, interconnect delays are accurately modeled using a distributed RC tree model. The delay for each net in the design is calculated based on the actual net topology. With these features, better control of performance, timing, density and routability is achieved.

DESIGN FLOW

Typical design flow is shown in Figure 1. A designer starts with specifications entered in either VLSI design tools or supported third party CAE workstations. The design is captured graphically using elements from the Portable Library, Logic Synthesizer, Data Path Compiler, and VGTRAM Compiler. A netlist screener program then performs an extensive check of logic design rules. Timing verification checks for potential set-up and hold violations or race conditions. Interactive floorplanning may also be performed at this time to obtain more accurate interconnect delay estimates.

Functional simulation is performed using user supplied test vectors and/or automatically generated test vectors. Multiple ASIC systems can be simulated to evaluate overall system performance. Fault coverage of the test vector set is determined by fault simulation. Vectors are added if necessary, and the final test program generated. At this stage, a design review is held with the customer and VLSI Technology for initial design approval.

The design is now ready for placement and routing. The designer has the option of selecting macro placement, specifying critical paths, and determining placement of system clock buffers. The remaining design layout is then completed by VLSI Technology.

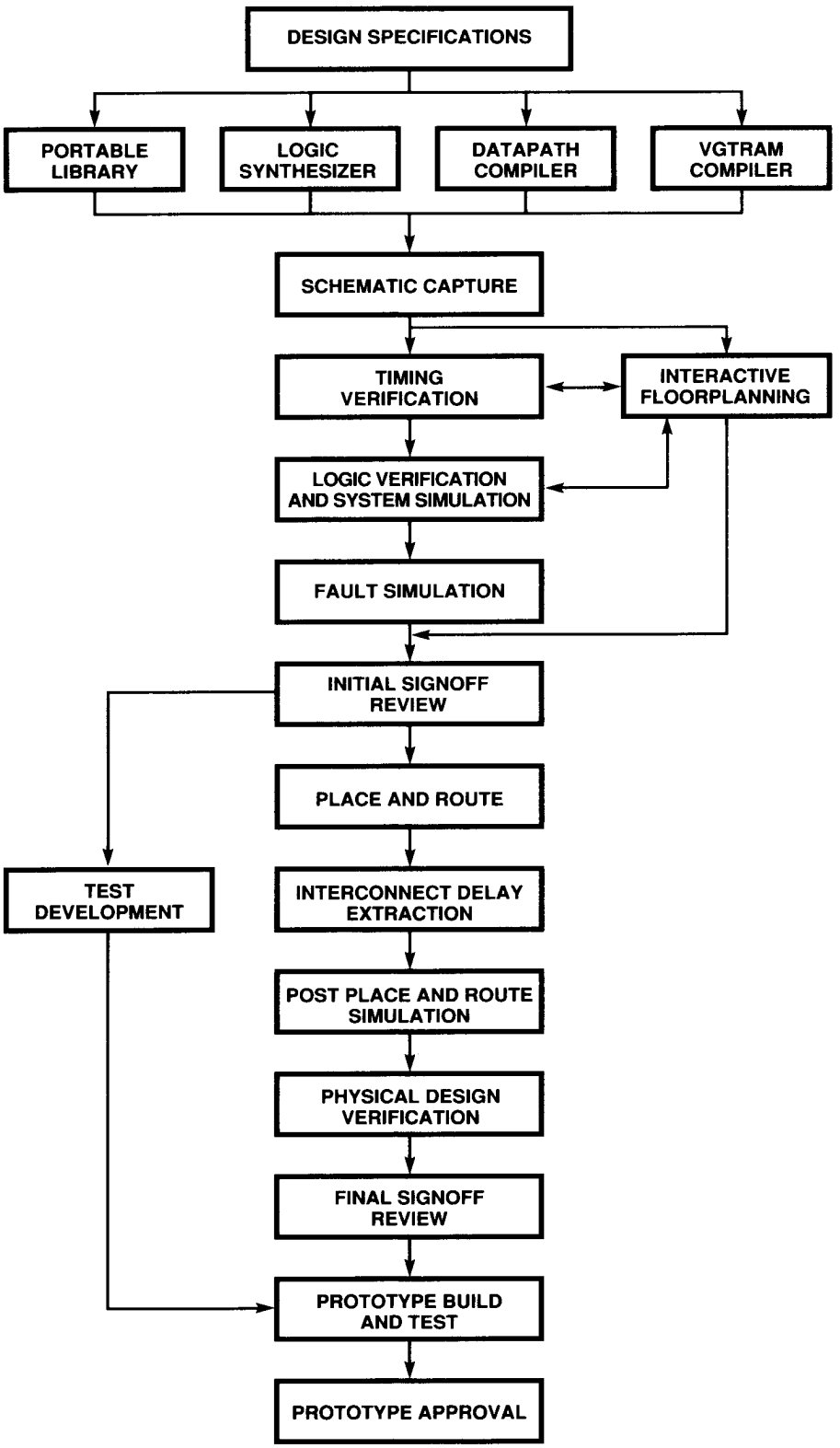
After layout completion, interconnect delay values are extracted from the physical layout and fed back to the simulator for final verification of circuit performance. Upon satisfactory post place and route simulation, physical design verification, and completion of test development, the design is approved by the customer and VLSI Technology. The design database is then released for prototype fabrication, assembly and test.

VLSI Technology Centers offer assistance in performing any step of the design flow. Technology Center services include system partitioning, functional and timing simulation, fault simulation, test vector generation, and special testing services.

WORKSTATIONS

VLSI Technology gate array designs may be developed on popular workstations supported by VLSI Technology. Designers using such workstations are provided with a macro library containing the symbols, simulation models and software for design verification, timing calculations and netlist generation. The design is transferred to a VLSI Technology Center where placement and routing are performed. The final interconnect capacitances are passed back to the workstation for verification of circuit performance.

FIGURE 1. DESIGN FLOW



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature (TA) under Bias, Note 1:

Military	−55°C to +125°C
Commercial	0°C to +70°C
Industrial	−40°C to +85°C

Storage Temperature:

Ceramic	−65°C to +150°C
Plastic	−40°C to +125°C

Supply Voltage	−0.5 to +6.0 V
Input Voltage	−0.5 to VDD +0.5 V
DC Input Current	±20 mA
Lead Temperature	300°C

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of this device under these or any conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS Specified as VDD and ambient temperature over the designated range, Note 2

Symbol	Parameter	Min	Max	Unit	Conditions
VIH	Input HIGH Voltage CMOS Input TTL Input	 0.7 × VDD 2.0	 VDD VDD	V	Guaranteed Input HIGH Voltage
VIL	Input LOW Voltage CMOS Input TTL Input	 −0.5 −0.5	 0.3 × VDD 0.8	V	Guaranteed Input LOW Voltage
VT+	Schmitt-Trigger Positive-going Threshold	2.6		V	
VT−	Schmitt-Trigger Negative-going Threshold		1.8	V	
VOH	Output HIGH Voltage PT6O01 PT6O02 PT6O03 PT6O04 PT6O05	VDD −0.05 2.4 2.4 2.4 2.4 2.4		V	IOH = −1 μA IOH = −2 mA IOH = −4 mA IOH = −8 mA IOH = −12 mA IOH = −16 mA
VOL	Output LOW Voltage PT6O01 PT6O02 PT6O03 PT6O04 PT6O05		0.05 0.4 0.4 0.4 0.4 0.4	V	IOL = 1 μA IOL = 2 mA IOL = 4 mA IOL = 8 mA IOL = 12 mA IOL = 16 mA
IIN	Input Leakage Current	−10	10	μA	VIN = VDD or GND
IOZ	3-State Output Leakage Current	−10	10	μA	VOUT = VDD or GND

CAPACITANCE Specified at VDD and ambient temperature over the designated range, Note 2

Symbol	Parameter, Note 3	Min	Max	Unit	Conditions
CIN	Input Capacitance		5	pF	Excluding Package
COUT	Output Capacitance		5	pF	Excluding Package
CI/O	Transceiver Capacitance		5	pF	Excluding Package

Notes:

1. Junction temperature (TJ) not to exceed ambient temperature by more than 20°C.
2. Military range is −55°C to +125°C, ±10% power supply; industrial temperature range is −40°C to +85°C, ±5% power supply; commercial temperature range is 0°C to +70°C, ±5% power supply.
3. For cell pads only.

AC CHARACTERISTICS FOR SELECTED MACROS 5 Volts, 25°C, Typical Process

Macro	Description	Symbol	Propagation Delay (ns), Note 1 Fanout 1	2	4	8
Logic Gates						
IN01D1	1X Inverting Buffer	tPLH tPHL	0.19 0.14	0.28 0.21	0.46 0.33	0.82 0.57
IN01D2	2X Inverting Buffer	tPLH tPHL	0.10 0.10	0.14 0.13	0.23 0.19	0.41 0.32
IN01D5	5X Inverting Buffer	tPLH tPHL	0.09 0.06	0.11 0.07	0.15 0.10	0.24 0.15
ND02D1	2-Input NAND	tPLH tPHL	0.18 0.30	0.26 0.41	0.42 0.63	0.73 1.07
ND04D1	4-Input NAND	tPLH tPHL	0.30 0.61	0.38 0.79	0.54 1.15	0.86 1.86
NR02D1	2-Input NOR	tPLH tPHL	0.41 0.29	0.59 0.35	0.96 0.49	1.69 0.76
NR04D1	4-Input NOR	tPLH tPHL	0.80 0.60	0.88 0.66	1.04 0.77	1.35 0.99
AN02D1	2-Input AND	tPLH tPHL	0.42 0.44	0.51 0.49	0.69 0.59	1.04 0.79
XO02D1	2-Input Exclusive OR	tPLH tPHL	0.41 0.42	0.48 0.49	0.62 0.62	0.90 0.87
XN02D1	2-Input Exclusive NOR	tPLH tPHL	0.36 0.32	0.42 0.40	0.55 0.54	0.80 0.83
MX21D1	2-to-1 Multiplexer (Input to Output)	tPLH tPHL	0.49 0.62	0.58 0.67	0.78 0.77	1.16 0.98
Flip-Flops & Latches						
DFNTNB	Buffered D Flip-Flop (Clock → Q)	tPLH tPHL	1.21 1.39	1.29 1.44	1.44 1.53	1.76 1.70
LANFNB	Buffered Latch (D → Q)	tPLH tPHL	0.56 0.94	0.64 0.99	0.80 1.11	1.12 1.32
Input Buffers						
LSTC00/ PC6D00	TTL Input Buffer	tPLH tPHL	0.30 0.55	0.32 0.56	0.36 0.58	0.44 0.62
LSCC00/ PC6D00	CMOS Input Buffer	tPLH tPHL	0.23 0.33	0.24 0.34	0.27 0.37	0.32 0.42
Output Buffers						
			Capacitive Load (pF)			
			15 pF	**50 pF**	**85 pF**	**100 pF**
PT6O52	TTL Output Buffer w/4 mA Drive	tPLH tPHL	1.32 2.50	2.54 4.88	3.77 7.27	4.29 8.29
PT6O55	TTL Output Buffer w/16 mA Drive	tPLH tPHL	1.16 2.01	1.61 2.82	2.05 3.64	2.24 3.99
PC6O52	CMOS Output Buffer w/4 mA Drive	tPLH tPHL	2.47 2.31	5.86 4.65	9.25 7.01	10.70 8.01
PC6O55	CMOS Output Buffer w/16 mA Drive	tPLH tPHL	1.69 1.83	3.05 2.64	4.39 3.46	4.98 3.81

Note:
1. Delays through interconnect are not included.

AC PERFORMANCE

AC performance for a given operating condition is a function of fanout, interconnect length, supply voltage, junction temperature, and process variability. The AC Characteristics table illustrates nominal propagation delays (tPDnom) for a set of commonly used macros. Delays for a different set of conditions can be estimated by applying the appropriate set of voltage, temperature, and process derating factors from Figures 2–4.

For example, worst-case commercial propagation delays are calculated with VDD = 4.75 V, Tj = 70°C, and a slow process model. From Figures 1–3, KV = 1.05, KT = 1.15, and KPslow = 1.56. Thus

$$\begin{aligned} tPDmax &= KV \times KT \times KPslow \times tPDnom \\ &= 1.05 \times 1.15 \times 1.56 \times tPDnom \\ &= 1.9 \times tPDnom \end{aligned}$$

PACKAGING INFORMATION

VLSI Technology offers a wide range of package styles and pin counts for the VGT300 Series, as illustrated in Figure 4. Each member of the VGT300 Series is available in a subset of the listed packages, please consult your VLSI Technology representative for specific array/package combinations.

VGT300 SERIES PACKAGES

Package	Pin Count
Plastic Leaded Chip Carrier (PLCC)	68, 84
Ceramic Leaded Chip Carrier (LDCCC)	68, 84
EIAJ Plastic Quad Flatpack (PQFP)	100, 128, 160
Plastic Pin Grid Array (PPGA)	120, 144, 180
Ceramic Pin Grid Array (CPGA)	120, 144, 180
High-Performance Ceramic Pin Grid Array (HPCPGA)	223, 299

FIGURE 2. PERFORMANCE VS VOLTAGE

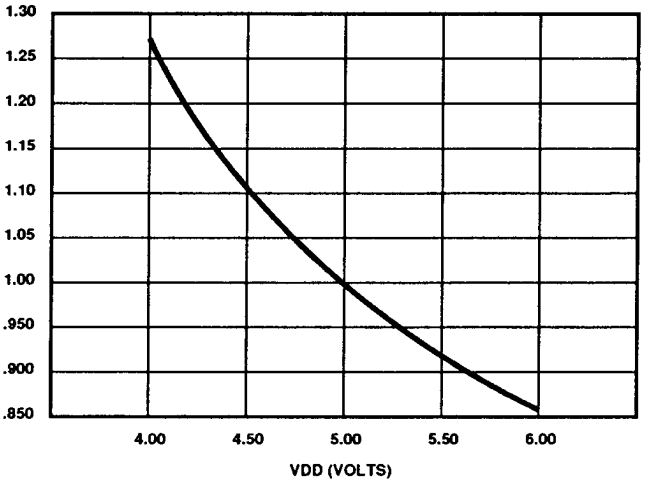


FIGURE 3. PERFORMANCE VS TEMPERATURE

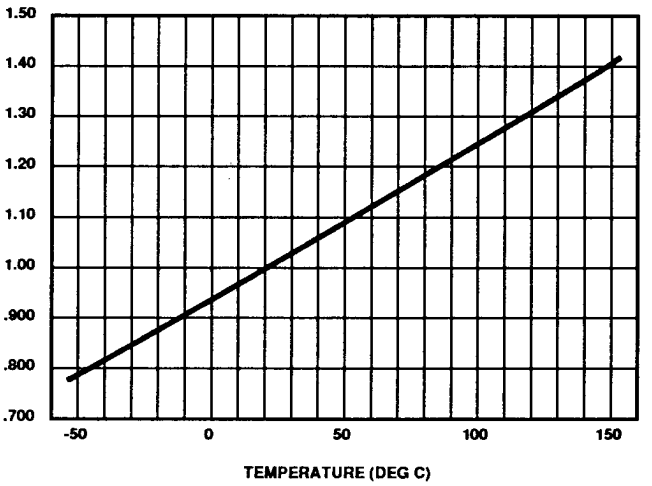


FIGURE 4. PERFORMANCE VS PROCESS

Process Model	Factor KP
Slow	1.56
Typical	1.00
Fast	0.60

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