MOSTEK

INDUSTRIAL PRODUCTS

Six-Decade Counter/Display Decoder

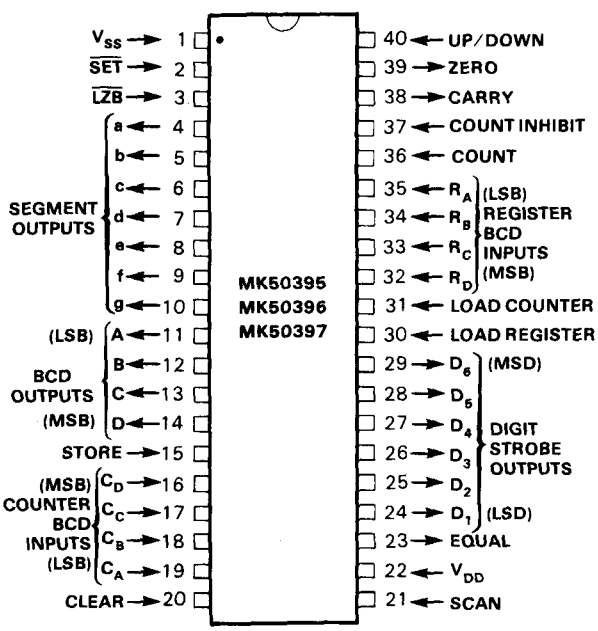
MK50395/6/7(N)

FEATURES

- Single power supply
- Schmitt trigger on the count input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- Leading zero blanking
- MK50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- MK50397 programmed to count time: 59 min. 59 sec. 99/100 sec.

PIN CONNECTIONS

Figure 1



V COUNTER DISPLAY DECODERS

DESCRIPTION

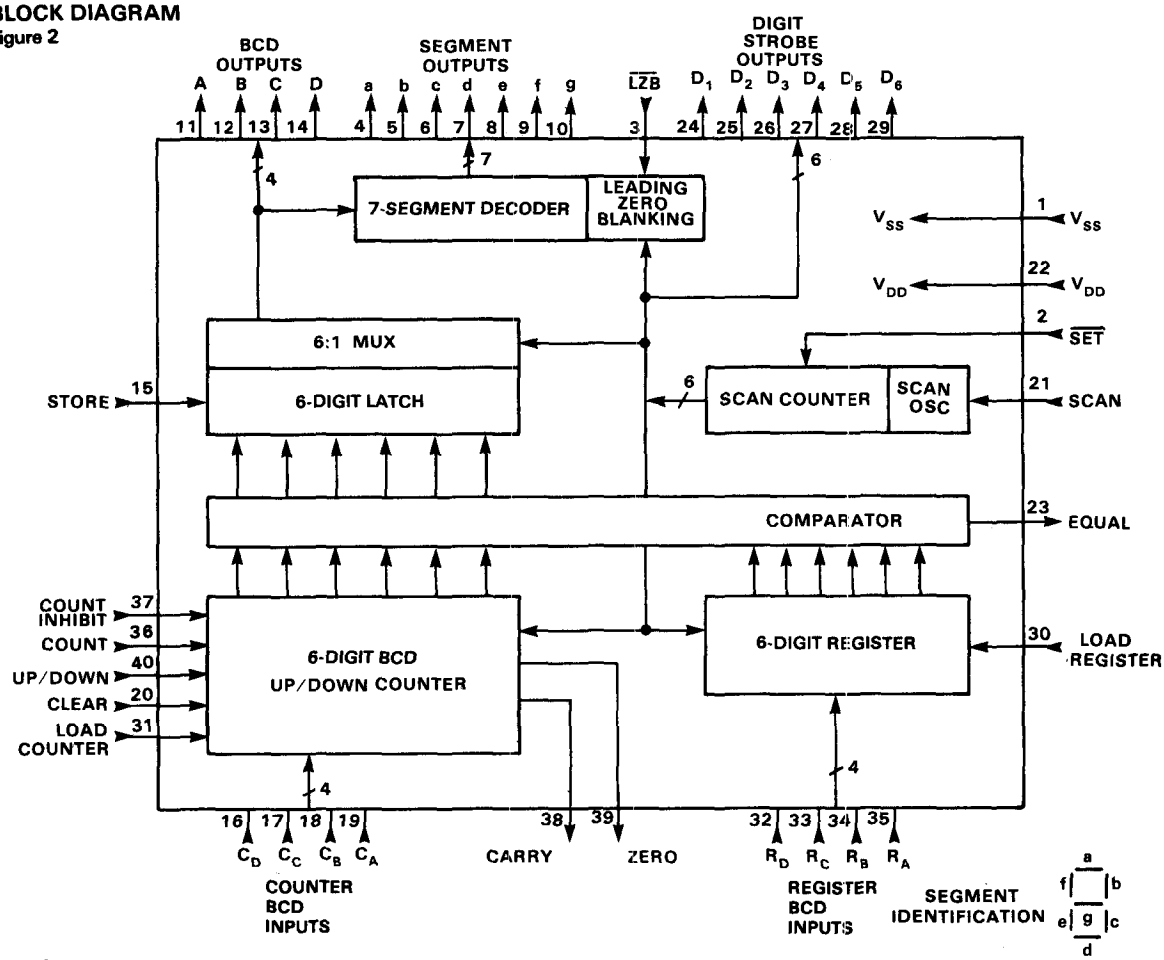
The MK50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down counter/display driver with compare register and storage latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MK50396 and MK50397 operate identically to the MK50395 except that two digits in each were programmed to provide divide-by-six circuitry instead of divide-by-ten. The MK50396 is well suited for industrial timer applications while the MK50397 is best suited for stop watch or real-time computer clock applications. Pin connections are shown in Figure 1.

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION (Refer to Figure 2)

V_{SS}, Pin 1

V_{SS} is the positive supply voltage. It should be maintained between 10 and 15 Vdc with respect to V_{DD}.

$\overline{SET}$, Pin 2

$\overline{SET}$ is used to exercise control over the scan counter. When a logic 0 level is applied to the $\overline{SET}$ input, the scan counter is forced to the MSD decade count. During this time, the SEGMENT OUTPUTS are blanked to protect against display burnout.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying a logic 1 level to $\overline{SET}$ allows normal scan to resume. DIGIT 6 output is active (V_{SS}) until the next scan pulse brings up the DIGIT 5 output.

$\overline{LZB}$, Pin 3

Bringing $\overline{LZB}$ low causes leading zeros in the display to be blanked. Leading zero blanking affects only the SEGMENT OUTPUTS and is disabled by bringing $\overline{LZB}$ high.

SEGMENT OUTPUTS, Pins 4 through 10

The SEGMENT OUTPUTS are open-drain and capable of sourcing 10 mA average current-per-segment over one digit cycle. Segments are on when at V_{SS}. Segment outputs are blanked during interdigit blanking time.

BCD OUTPUTS, Pins 11 through 14

BCD outputs are push-pull and are on when at V_{SS}. BCD output data changes at the beginning of the interdigit blanking time. Therefore, the BCD output data is valid when the positive transition of a DIGIT OUTPUT occurs.

STORE, Pin 15

The STORE input is used to control the transfer of data from the counter to the display. As long as the STORE input is low, data is continuously transferred from the counter to the display latch. Data in the counter will be latched and displayed

when the STORE input is high. STORE can be changed during the positive transition of the COUNT input.

COUNTER BCD INPUTS, Pins 16 through 19

The COUNTER BCD INPUTS are used to load the counter with BCD information one decade at a time. The counter can therefore be preset to any desired value. Loading is most easily done with the help of the DIGIT STROBE OUTPUTS. BCD thumbwheel switches with four diodes-per-decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades. (See Figure 5)

CLEAR, Pin 20

The CLEAR input is asynchronous and will reset all decades to zero when brought high. It does not affect the six-digit latch or the scan counter.

SCAN, Pin 21

The MK50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and the SCAN input (see Table 1). The waveform present on the scan oscillator input is triangular in the self-oscillate mode. Typically, the scan oscillator will oscillate at the frequencies shown in Table 1 with capacitors shown connected between V_{SS} and the SCAN input.

An external oscillator may also be used to drive the scan input.

In the external drive mode, the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self-oscillate blanking time (5-25 μs). Display brightness can be controlled by the duty cycle of the external scan oscillator.

V_{DD}, Pin 22

V_{DD} is the negative supply input and is normally connected to ground.

EQUAL, Pin 23

The EQUAL output goes high for one count period when the contents of the counter and compare register are equal. The EQUAL output is inhibited by a LOAD COUNTER or LOAD REGISTER operation, which lasts until the next interdigit blanking period following a negative transition of LOAD COUNTER or LOAD REGISTER.

DIGIT STROBE OUTPUTS, Pins 24 through 29

The DIGIT STROBE OUTPUTS are push-pull and are on when at V_{SS}. DIGIT STROBES are decoded internally by a divide-by-six Johnson counter. This counter scans from MSD to LSD. The $\overline{SET}$ input exercises control over this counter. The DIGIT STROBES are blanked during the interdigit blanking time.

TYPICAL SCAN OSCILLATOR FREQUENCIES
Table 1

C_{SCAN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

LOAD REGISTER, Pin 30

Applying a logic 1 level to LOAD REGISTER allows the register to be loaded through the REGISTER BCD INPUTS, digit-by-digit, synchronous with the scan counter. (See Figure 4)

LOAD COUNTER, Pin 31

Applying a logic 1 level to LOAD COUNTER allows the counter to be loaded through the COUNTER BCD INPUTS, digit-by-digit, synchronous with the scan counter. (See Figure 4)

REGISTER BCD INPUTS, Pins 32 through 35

The register is loaded identically as described in the COUNTER BCD INPUT paragraph. The register may be loaded independently of the counter. However, the CLEAR input will not remove the register contents. Contents of the register are not displayed by the BCD or SEGMENT OUTPUTS.

COUNT, Pin 36

The six-decade counter is synchronously incremented or decremented on the positive edge of the COUNT input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the COUNT input. A count frequency of 1 MHz can be achieved if the EQUAL output, ZERO output, and CARRY output are not used. These outputs do not respond at this frequency due to their output delay, as illustrated on the timing diagram, Figure 3.

COUNT INHIBIT, Pin 37

A logic 1 level activates COUNT INHIBIT. The COUNT INHIBIT can be changed during the positive transition of the COUNT input.

CARRY, Pin 38

The CARRY output goes high with the leading edge of the COUNT input at the count of 000000 when counting up or at 999999* when counting down and goes low with the

*Carry occurs at 99 59 59 for the MK50396 and 59 59 99 for the MK50397

negative going edge of the same COUNT input. CARRY is a push-pull output.

ZERO, Pin 39

The ZERO output goes high for one COUNT period when all decades contain zero. During a LOAD COUNTER operation, the ZERO output is inhibited. ZERO changes on the leading edge of the count input and is also a push-pull output.

UP/DOWN, Pin 40

The counter will increment when the UP/DOWN input is high (V_{SS}) and will decrement when the UP/DOWN input is low. The UP/DOWN input can be changed 0.75 μs prior to the positive transition of the count input.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... +0.3 V to -20 V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... -40°C to +100°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS
(V_{DD} = 0 V, +10.0 V $\leq V_{SS} \leq$ +15.0 V, 0°C $\leq T_A \leq$ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply Voltage (V_{DD} = 0)	10	15	V	
I_{SS}	Supply Current		30	mA	1
B_V	Break-Down Voltage (Segment only @ 10 μA)		V_{SS} - 26	V	
P_D	Power Dissipation		670	mW	2
V_{IL}	Input Low Voltage, "0"	V_{DD}	0.2 (V_{SS})	V	
V_{IH}	Input High Voltage, "1"	V_{SS} - 1	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30 μA		0.2(V_{SS})	V	4
V_{OH}	Output Voltage "1" @ 1.5 mA	0.8 (V_{SS})		V	4
I_{OH}	Output Current "1" Digit strobes Segment outputs	 3.0 10.0		 mA mA	 5 6
I_{SCAN}	Scan Input Pull-Up Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pull-Down Current @ 15 V	2	40	μA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pull-Up Current @ 0 V	5	60	μA	

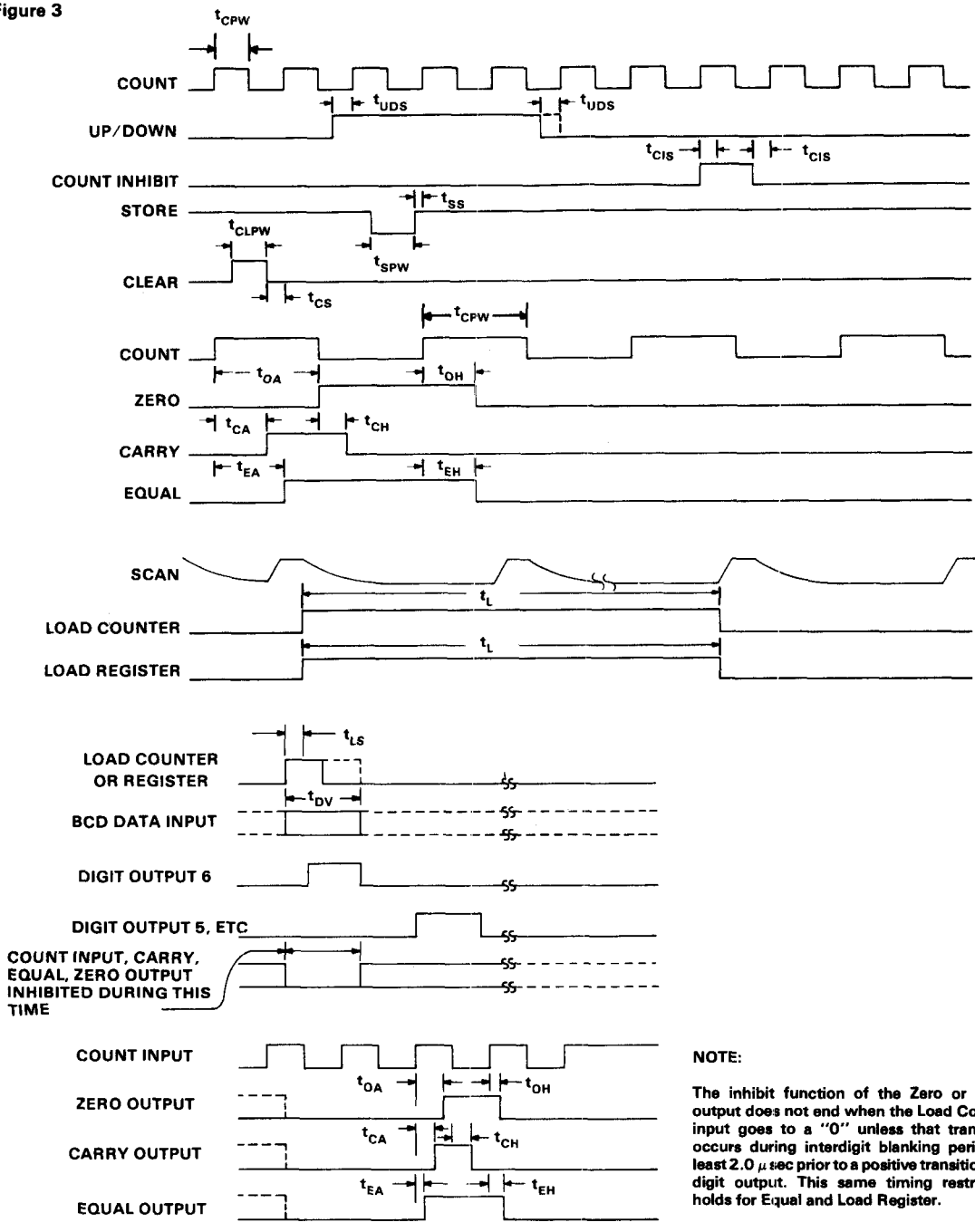
AC CHARACTERISTICS
(V_{DD} = 0 V, +10.0 V ≤ V_{SS} ≤ +15.0 V, 0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	7,8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	400		ns	9
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Set-Up Time	0		μs	10
t_{CIS}	Count Inhibit Set-Up Time	0		μs	10
t_{UDS}	Up/Down Set-Up Time	0.75		μs	10
t_{CLPW}	Clear Pulse Width	2.0		μs	10
t_{CS}	Clear Set-Up Time	0.5		μs	10
t_{OA}	Zero Access Time		3.0	μs	10
t_{OH}	Zero Hold Time		1.5	μs	10
t_{CA}	Carry Access Time		1.5	μs	10
t_{CH}	Carry Hold Time		0.9	μs	11
t_{EA}	Equal Access Time		2.0	μs	10
t_{EH}	Equal Hold Time		1.5	μs	10
t_L	Load Time	$6/f_{SI}$		s	
t_{LS}	Load Set-Up Time	2.0		μs	12
t_{DV}	Data Valid Time	2.0		μs	13

NOTES:
1. I_{SS} with inputs and outputs open at 0°C. 28 mA at 25°C and 25 mA at 70°C. This does not include segment current. Total power per segment must be limited so as not to exceed power dissipation of package. (Θ_{JA} = 100°C/Watt)
2. All outputs loaded.
3. Min V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} -2.5 V. Those inputs have internal pull-down resistors to V_{DD}.
4. This applies to the push-pull CMOS-compatible outputs. Does not include digit strobes or segment outputs.
5. For V_{OUT} = V_{SS} -2.0 Volts. Average value over one digit cycle.
6. For V_{OUT} = V_{SS} -3.0 Volts. Average value over one digit cycle.
7. Measured at 50% duty cycle.
8. If CARRY, EQUAL, or ZERO outputs are used, the count frequency will be limited by their respective output times.
9. The COUNT pulse width must be greater than the CARRY access time when using the CARRY output.
10. Measured from positive edge of COUNT input 10% level.
11. Measured from negative edge of COUNT input 90% level.
12. Measured from positive transition of DIGIT output 10% level.
13. Measured from negative transition of DIGIT output 90% level.

TIMING DIAGRAMS

Figure 3

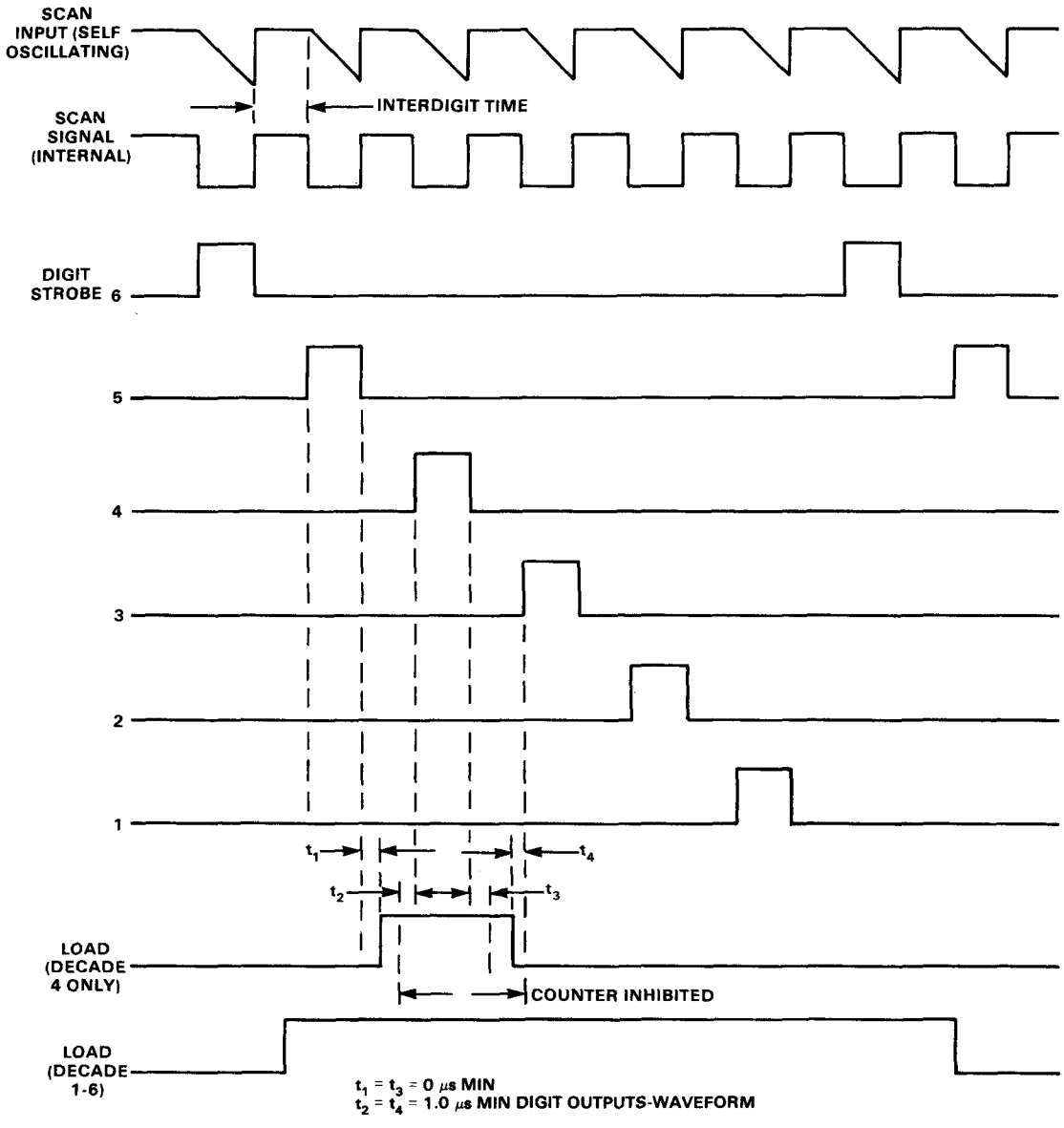


NOTE:

The inhibit function of the Zero or Equal output does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 μsec prior to a positive transition of a digit output. This same timing restriction holds for Equal and Load Register.

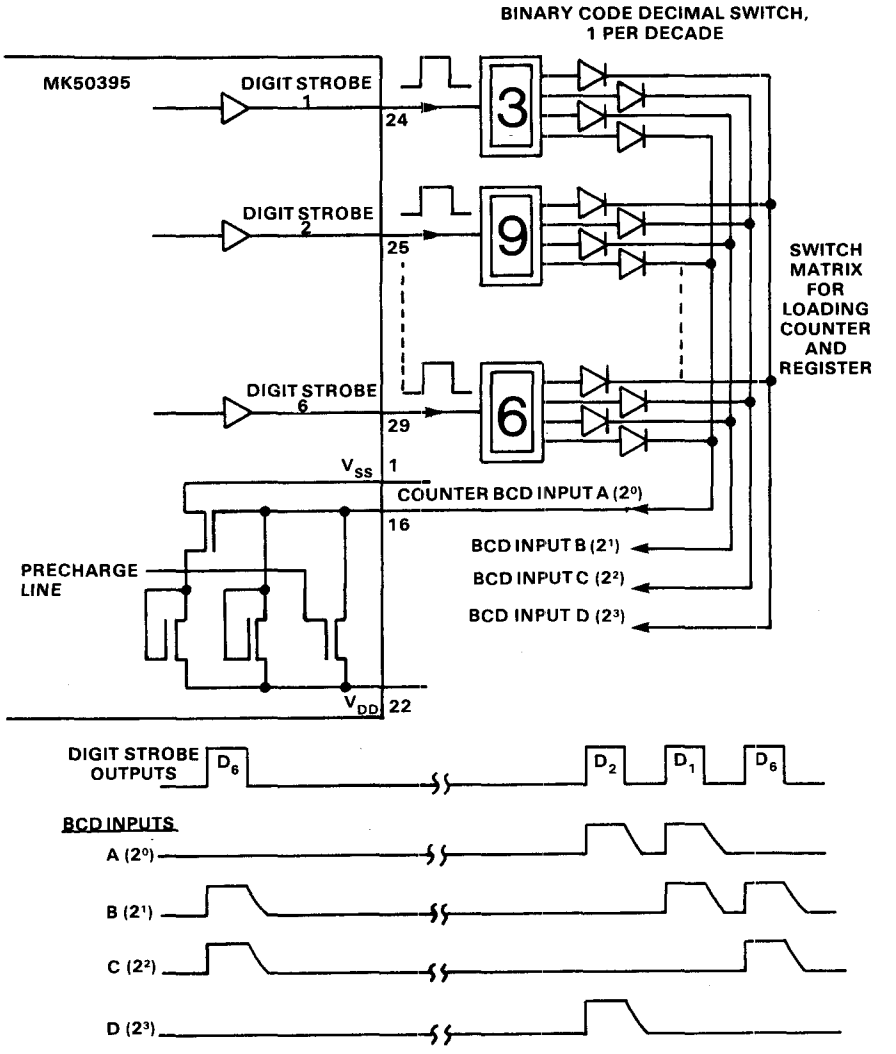
LOAD COUNTER, REGISTER TIMING

Figure 4



BCD SWITCH MATRIX

Figure 5



NOTE THAT ALL INPUT LINES ARE ALL PULLED TO V_{DD} DURING INTERDIGIT BLANKING

DARK ROOM TIMER
TYPICAL APPLICATION
Figure 6