BLAST

A BLAST (Board Level Application Scalable Technology) is a very small form factor component that offers a platform for add-on functionality to FPGA cards. Designed as an independent PCB module to enhance 4DSP's FPGA product family, BLAST provides the opportunity to add a variety of functions to programmable platforms using a common electrical interface, high-speed signaling, and a small footprint (21x25mm). Several BLAST sites are available on most 4DSP FPGA-based products. This gives the user more control over the configuration of their FPGA board without complicating the design and manufacturing processes or extending lead times.

With BLAST, it is possible for users to easily and cost-effectively optimize their hardware with different types of memory, signal processing, or onboard storage to ensure that the application or algorithm runs efficiently. 4DSP's emphasis on delivering not only high performance, but flexibility as well is at the core of our design philosophy. This approach contrasts with the way that typical hardware platforms from other vendors are designed. By recognizing that one size does not fit all, we are able to deliver COTS products that can adapt to the requirements of a particular application while accelerating time to market.

Technical Characteristics of BLAST

A BLAST site can be configured for a variety of purposes including high-speed SRAM, large density SDRAM, non-volatile memory, dedicated signal processor, microcontroller, video codec (JPEG2000, H-264, MPEG-4), or non-volatile flash memory. BLAST sites connect directly to the FPGA as a 160-pin Ball Grid Array (BGA) component, offering up to 100 single-ended I/O pins. Measuring less than one inch square, BLAST sites are available in two dimensions that have been carefully designed for compact board form factors such as XMC and 3U VPX. The recommended footprint is shown below.

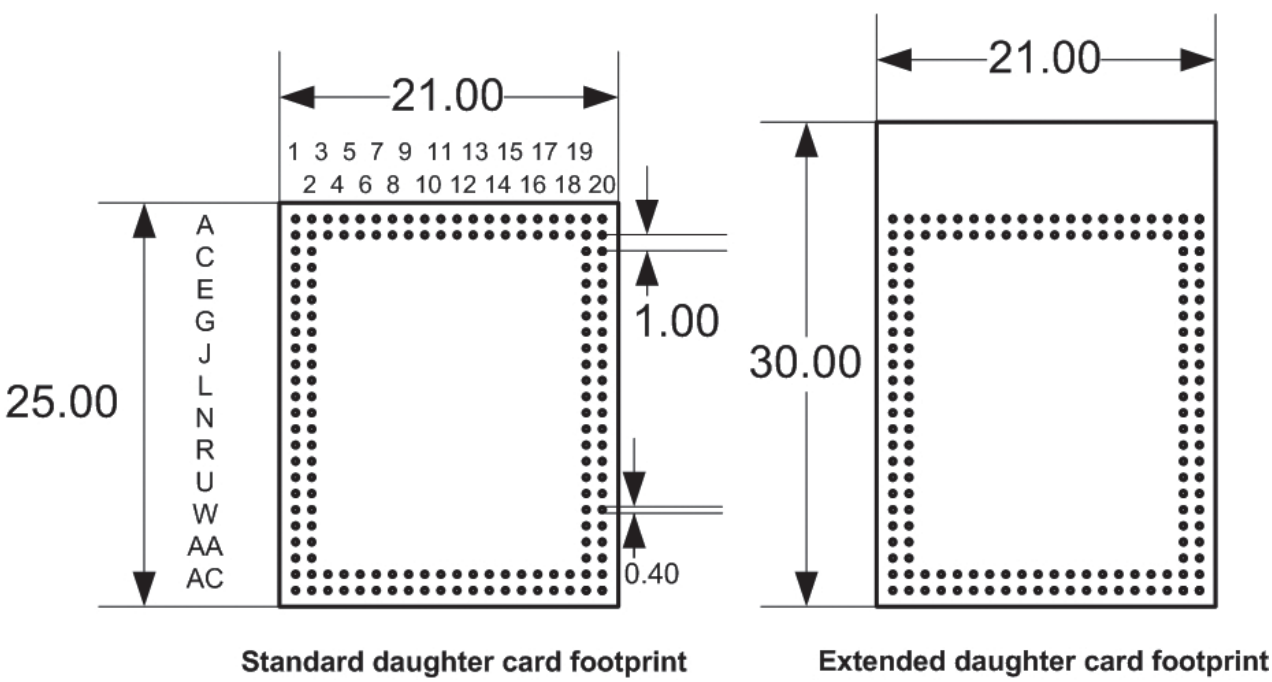


Figure 1 : BLAST recommended footprint (top view)

Features

- 160 balls (100 dedicated to user IO / 100 IO lines connected to FPGA)
- 60 Power connections (GND, Vcore, Vio, Vref) for devices requiring multiple voltage levels
- Ruggedized – sound electrical and mechanical interface because the modules are mounted on the board like a component using BGA (ball grid array)
- Compact footprint (21x25mm or 21x30mm)
- Conduction or convection-cooled usage possible

BLAST Options

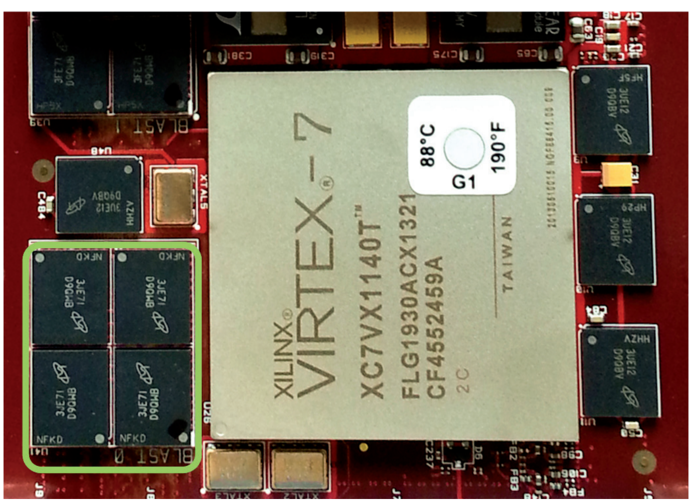
- High-density memory options (DDR2/DDR3 SDRAM, QDR2+ SRAM, NAND FLASH)
- Onboard storage (SSD)
- Real-time image compression (JPEG2000, MPEG4)
- DSP (AD SHARC, TI C5X)
- ASICs

BLAST for High-Speed Memory

System designers must resolve complex issues related to architecture, algorithms, and the features of all components when designing for high-performance applications. A fundamental problem is the implementation of memory architecture, because it can be a bottleneck for system performance. However, the need to use higher-speed external memories can make it difficult to maintain signal integrity. Modern FPGAs such as the Xilinx Virtex and UltraScale devices used by 4DSP offer such features as dedicated I/O circuitry, support for various I/O standards, and specialized IP that mitigate this problem and enable them to reliably interface with external memory. These programmable devices are therefore able to buffer data when their internal memory capacity is insufficient.

While external memory can greatly boost performance for many data processing applications, implementing a high-efficiency memory controller in an FPGA can be a challenging task. The memory interface has a direct impact on the performance of the entire system because it must provide the necessary read/write bandwidth to support the flow of data. This means that higher memory interface bandwidths are necessary for every new generation of programmable devices.

For an FPGA to get the most out of external memory, it is crucial that the memory interface controller be flexible, efficient, and easy to use. 4DSP solves this problem for customers by providing a proven IP core that places a FIFO wrapper around Xilinx's MIG (Memory Interface Generator), a tool that simplifies the design process by generating unencrypted Verilog or VHDL design files, UCF constraints, simulation files, and implementation script files. This reference design offers a straightforward method for an FPGA to access BLAST memory resources without the need for addressing. 4DSP's customized IP eliminates the need for users to spend time developing their own memory controller, but modifications or new reference designs can be easily be made using StellarIP, the intuitive firmware design environment that 4SDP includes with its boards.



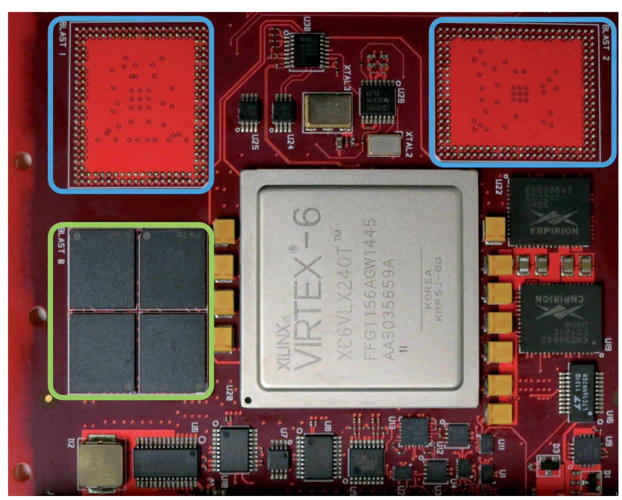


Figure 2: BLAST sites configured as DDR3 SDRAM (green) 3U VPX boards. Empty BLAST sites are marked in blue.

BLAST Memory Applications

Today's sensors can collect large amounts of data at very high rates. It is now commonplace for gigabytes per second to be digitized by analog-to-digital converters. In applications that rely on high-speed data acquisition, the limitations of both the host, such as a PCIe bus, and the FPGA's memory resources can restrict performance. It is therefore necessary to buffer incoming data in memory, such as DDR3/DDR4 SDRAM or QDR2+ SRAM, where it can be accessed and processed by the FPGA until the host is ready to receive it. Different types of memory devices are better suited for certain applications, and the BLAST sites on 4DSP FPGA boards provide the option of adding the best memory choice for a particular device and application.

Designs for high-speed data acquisition applications can exploit the parallel processing capabilities of FPGAs when provided with enough memory bandwidth. DDR3 or DDR4 SDRAM is desirable as a high-speed memory option for FPGAs because of its low power consumption, large density, increased data rates, and burst capabilities. The real-time processing required for RADAR systems on board unmanned aerial vehicles (UAVs), for instance, can be achieved with a hardware system that links SDRAM directly to the FPGA via BLAST to deliver the necessary processing power and memory capacity.

A video processing system is another example of an application that requires maximum bandwidth performance from a DDR3 or DDR4 SDRAM interface. FPGAs are a good choice for video because multiple video processors can be implemented inside one FPGA. The challenge becomes moving the data in and out of the FPGA as quickly and efficiently as possible. A BLAST site populated with DDR3 or DDR4 SDRAM can deliver sufficient bandwidth for such stream-oriented data processing systems.

BLAST sites can also be configured as QDR2+ SRAM, which offers independent read and write buses with higher random access performance than DDR3 or DDR4 SDRAM. This makes it possible to maximize bandwidth with separate read and write ports per memory device. The simultaneous operation of these two data ports increases efficiency by eliminating the need for the data bus turnaround cycles required by other I/O devices. Bandwidth-intensive applications benefit greatly from the performance increase that this architecture enables. QDR2+ SRAM is therefore an effective option for very high-speed data communications systems that use ATM switches and routers operating at data rates above 200 MHz. For these networking applications, which require fast processors and high-speed interfacing peripheral components, QDR2+ can serve as the main memory for controller buffer memory, packet memory, lookup tables, and linked lists.

Wireless telecommunications, RADAR, and SONAR applications also use FPGA and external memory architectures to enable the efficient Fast Fourier Transform (FFT) methods that are central to many real-time signal processing applications. FFT lengths in excess of 128k-points typically exceed FPGA memory resources, so incorporating comparatively inexpensive external QDR2+ SRAM into a system design helps to maximize silicon performance and efficiency while making continuous real-time processing possible.

Why Choose BLAST?

4DSP created BLAST to accelerate the manufacturing process for customer-specific configurations that normally delay the production cycle. The key benefit of using BLAST sites is that an FPGA card can be customized for a particular application without having to redesign the card, saving months of engineering time and resources that would otherwise be necessary to build a specialized design for a short-term project deadline. Additionally, BLAST is not just a technology for prototyping, its sound mechanical and electrical interfaces make it a choice of reference for ruggedized applications where flexibility and reliability meet great performance.
The combination of Xilinx Virtex-7 or UltraScale performance with BLAST sites on FPGA carrier cards such as the FM780 (XMC) and VP780 (3U VPX) provides more customization choices for customers while allowing for rapid production.

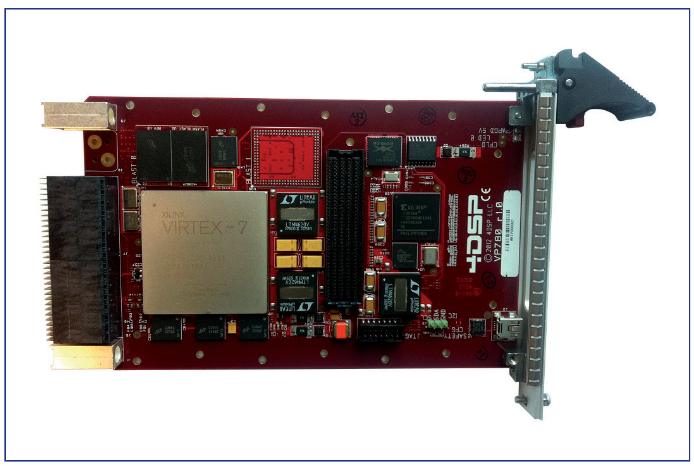


Figure 3 :
VP780 3U VPX card with Virtex-7 FPGA & two BLAST sites