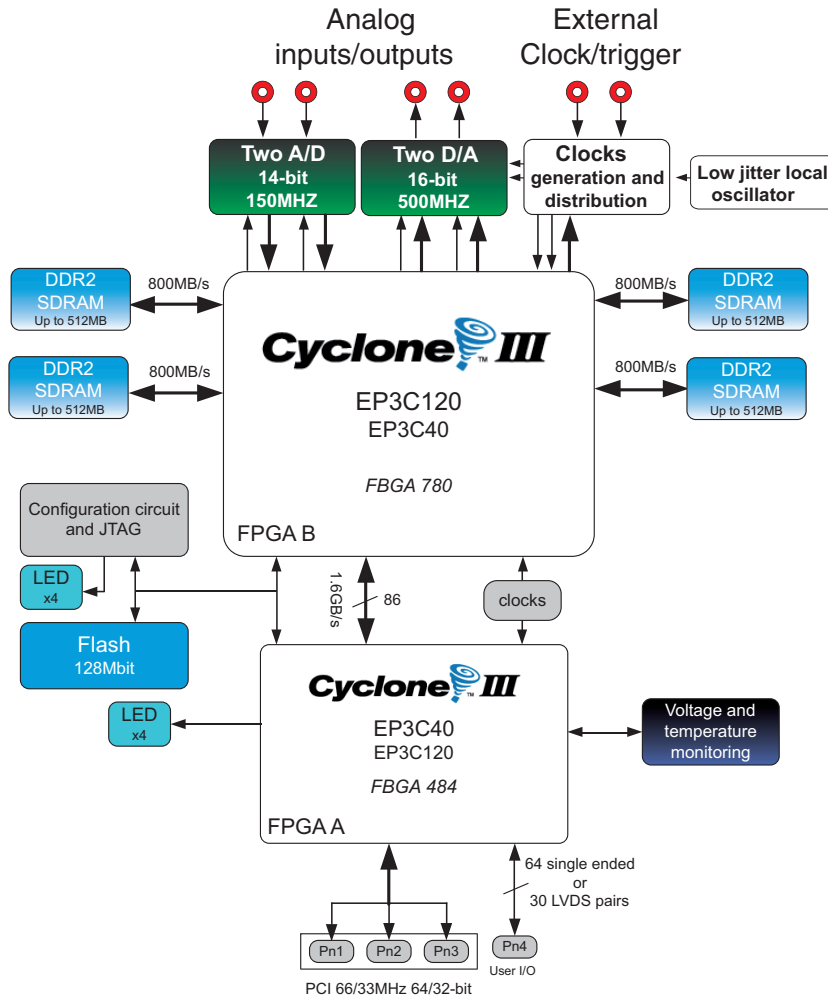


## AD350 - Dual A/D 14-Bit@150Msps / Dual D/A 16Bit@500Msps Altera Cyclone-III Based PMC-X

### Description

The AD350 is a PMC-X expansion card designed for wireless base stations and MIMO test-bed systems. The AD350 features two 14-bit A/D channel inputs sampling up to 150MSPS, and a dual-channel 16-bit 500Msps high-speed D/A converter. The AD350 is the ideal prototyping system to implement flexible and scalable multi-input and multi-output antenna transmitter systems. It can also be used in synchrotron systems to regulate amplitude voltages, phase and resonant frequency of accelerator's RF cavities.



### Applications

- Software defined radio (SDR)
- Wireless communication receivers
- Test and measurement instruments
- Precision Motor Control
- Aerospace measurement instruments
- Video and imaging algorithms (DVB-C...)
- Low-power medical MRI equipments
- GPS Time Synchronization
- Telemetry Instrumentation

### Features

- Dual 14-bit, 150MSPS A/D converter
- Dual 16-bit, 500MSPS D/A converter
- Dual Cyclone III FPGA architecture
- 512MBytes of DDR2 SDRAM, expandable to 2GBytes in total.
- External FPGA clock input and output
- External 1pps synchronization clock input
- FPGA voltage and temperature sensors
- PCI 32/64-bit 33/66MHz bus interface

### Software Support

- Board control and monitoring tools
- Flash programming utility
- Confidence tests
- Host side API
- Software program example
- Quartus II project for both FPGAs
- Test firmware and VHDL source code
- Drivers for Windows, Linux, VxWorks (pending), Lynx OS (pending)

### Ordering information

**AD350-40-120-1-8-C-AC**

Altera Cyclone III Device-A 40 = EP3C40 120 = EP3C120	Altera Cyclone III Device-B 40 = EP3C40 120 = EP3C120	Memory Size (standard) 512 Mbytes -1 2 Gbytes -2	Cooling CC = not available AC = Convection cooled	Cyclone III Temperature range C = Commercial (0° to + 85°C) I = Industrial (-40°C to + 100°C)	Cyclone III Speed Grade -8 (lowest), -7 or -6
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## AD-DA Section General Description

The analog to digital conversion section of this board is provided on a daughter card isolating the design for better SNR performance. This section of the board provides two 14-bit 150MSPS A/D channels and two 16-bit 500MSPS D/A channels. There is 1 external trigger, 1 external clock plus an on-board generated clock. The AD350 is mechanically and electrically compliant to PMC standard and specifications (IEEE P1386.1).

### Input Analog Channels

The Input Analog Channels are connected via SMA connectors on the front panel. Both channels are 50Ω terminated and are connected to the A/D circuit using a double balun configuration in order to reduce the amplitude and phase distortion of the signal. Connection is via AC coupling with wideband transformers which operate very efficiently in the 4.5MHz to 650MHz band.

### Output Analog Channels

The output analog channels are also AC coupled via wideband transformers (4.5MHz to 3GHz). The connectors on the front panel are of SMA type.

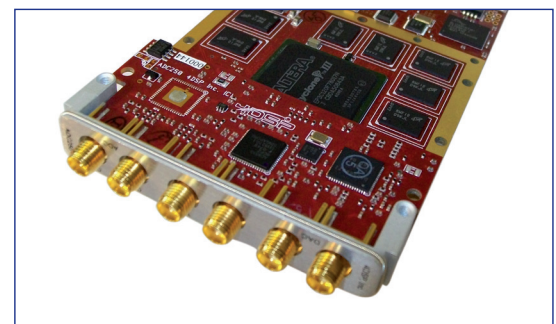
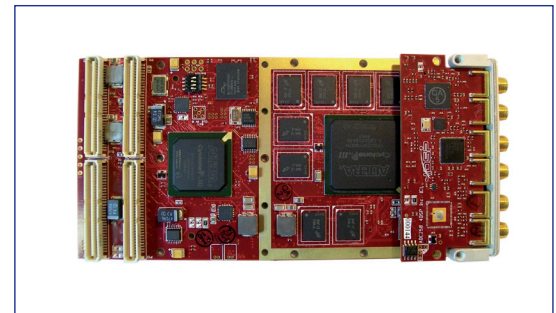
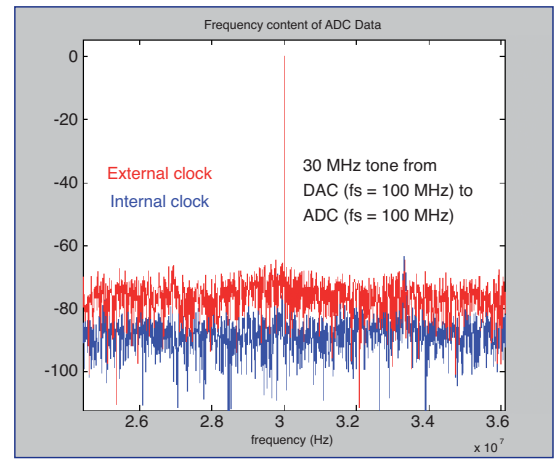
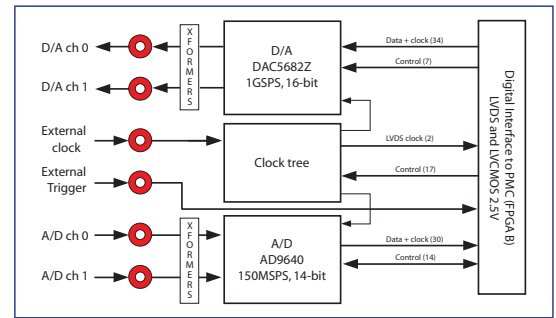
### External Clock

The clock architecture is a combination of flexibility and high performance. User may choose to use the external clock (single ended) or the on board clock. Clock components have been carefully selected to minimize jitter and phase noise that can lead to a degradation of the A/D and D/A devices performances. The external clock is routed to both a buffer and a voltage comparator. The buffer output is used exclusively by the FPGA to detect the presence of an external clock. All clock signals (except the external clock) are routed as differential pairs.

### External Trigger

An external trigger is available on the front panel (SMA connector). The trigger signal is single ended and compatible with LVTTTL and TTL. GPS receivers generating a 1pps signal can be interfaced to the external trigger if required.

Environmental	Level A	Level B
Operating Temperature	0°C to 70°C	-40°C to 85°C
Storage Temperature	-50°C to 125°C	-50°C to 125°C
Humidity-Operating	0 to 100% non-condensing	0 to 100% non-condensing
Storage Humidity	0 to 100%	0 to 100%
Vibration Random	0.1 g <sup>2</sup> /Hz 10 - 3kHz	0.1 g <sup>2</sup> /Hz 10 - 3kHz
Shock	30g peak	30g peak
Coating	none	Conformal



Talk to us about your algorithmic requirements, 4DSP is a full-service firmware and software development house. We are a specialist at high performance FFT and Video Processing. Check with us, we may have IP Cores that meet requirements for your application, right off the shelf.