JESD204B on FMC

Originally released as JESD204 in 2006 and since revised, the JESD204B serial interface standard was created through the JEDEC committee to meet market demand for a more efficient interface as the speed and resolution of converters has increased. JESDS204B provides a more reliable, more efficient, and more flexible alternative to the traditional method of interfacing data converters with FPGAs or DSPs using LVDS or CMOS. Additional functionality includes harmonic clocking which enables converters to be clocked using a multiple of the sampling rate such as two, four or eight.

From a design standpoint, the JESD204B interface simplifies board layout for most applications by reducing the number of digital lane connections compared to traditional digital parallel interconnects. Minimizing the number of interconnects required to interface high-speed (>10 MSPS) analog-to-digital (ADC) and digital-to-analog (DAC) converters on an FPGA Mezzanine Card (FMC) to an FPGA on a carrier card makes it possible to design for smaller form factors while maintaining system performance.

Function	Serial LVDS	JESD204B
Max Lane Rate	1.0 Gbps	12.5 Gbps
Multiple Lanes	No	Yes
Lane Synchronization	Yes	Yes
Multi-device Synchronization	Yes	Yes
Deterministic Latency	Yes	Yes
Harmonic Clocking	No	Yes

Table 1: Comparison of Serial LVDS and JESD204B

Applications

These characteristics make JESD204B a good match for high-speed ADC applications that have rigid constraints on system size and cost, including software-defined radio (SDR), portable instruments, medical imaging equipment, and secure military communications.

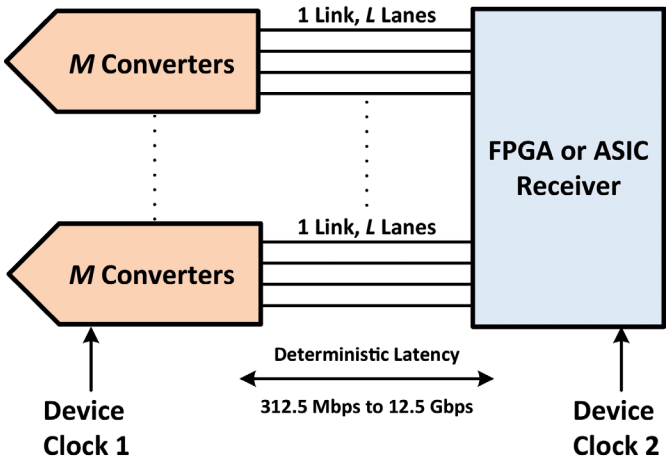

Figure 1: JESD204B Serial Data Link

The standard is also better suited for demanding system designs that require multiple ADC channels to be synchronized, such as those found in mobile telecom base stations, microwave backhaul, and RADAR.

Wireless telecommunications transceivers based on OFDM (orthogonal frequency-division multiplexing), such as those use in today's mobile networks, implement DSP blocks on FPGAs or SoC devices to drive antenna array elements as they generate beams that target individual mobile devices. Each array element can require the movement of hundreds of megabytes of data per second between FPGAs and data converters in both transmit or receive modes. JESD204B is therefore an excellent choice for mobile network transceivers. Additionally, software defined radio (SDR) is essential to the transceiver infrastructure of multimode wireless networks supporting LTE, GSM EDGE, W-CDMA, CDMA2000, and WiMAX standards. SDR implementations in modern cellular antennas achieve unprecedented wireless data rates because of increasing channel bandwidths and advanced modulation methods that can be rapidly reconfigured. JESD204B is ideal as an efficient FPGA-to-data converter interface for high-performance SDR due to its low power requirement and low pin count.

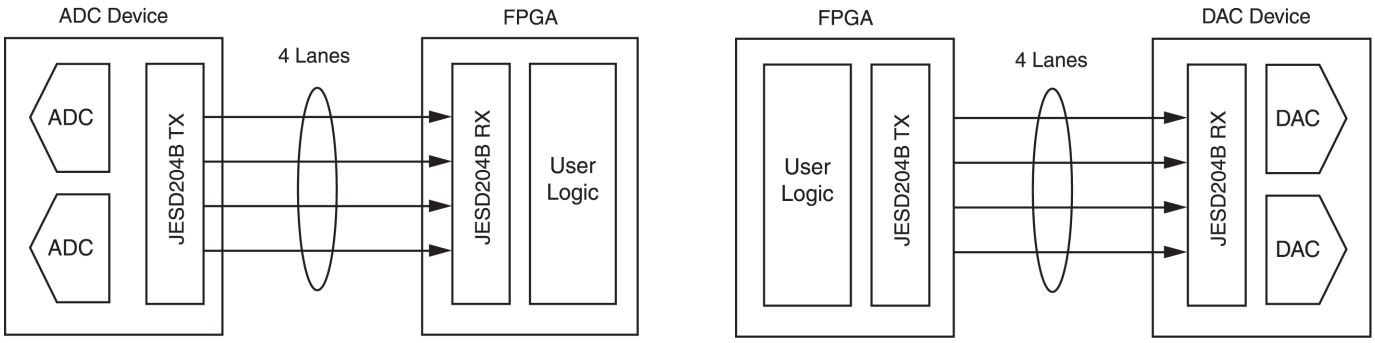

Figure 2: Typical Data Converter to FPGA Configurations Using JESD204B Interfaces (Source: Xilinx)

There are also opportunities to use JESD204B in aerospace and military systems. Advancements in radar receivers have resulted in increasingly complex pulse processing that can rely on signal bandwidths of 1GHz and above. Active electronically scaled array (AESA) radar systems, for example, may employ thousands of elements and require a high-bandwidth SERDES-based serial interface such as JESD204B to connect data converters in the array elements to FPGAs or DSPs that process and generate data.

Medical imaging is another area in which the efficiency of JESD204B can help to reduce the cost and complexity of system designs. Computational tomography (CT) scanners, magnetic resonance imaging (MRI) systems and ultrasound instruments can generate multiple channels of data that must be sent through data converters to FPGAs or DSPs. As the number of input and output channels on these systems increases, PCBs become more complex to accommodate more components. The JESD204B interface helps to mitigate this problem.

4DSP FMC144

4DSP's FMC144, a VITA 57.1-compliant FMC module, exemplifies the use of JESD204B as a high-speed serial interface between data converters and an FPGA. The high-performance Texas Instruments (TI) DAC38J84 D/A and ADC16DX370 A/D converters on the FMC144 have low power requirements and readily support RADAR and such wide-bandwidth test applications as mobile testing devices and arbitrary waveform generators because of the JESD204B interconnections.

The FMC144 provides four 16-bit A/D channels with speeds up to 370MSPS and four 16-bit D/A channels up to 2.5GSPS. This daughter card is capable of digitizing data over multiple channels required for beamforming and direction finding which makes it well-suited for multi-antenna arrays used in wireless networks. 4DSP and TI showcased the FMC144 in combination with the Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit at the Avnet X-Fest series of training events held throughout North America, Asia, Europe and Japan in 2014 and 2015.

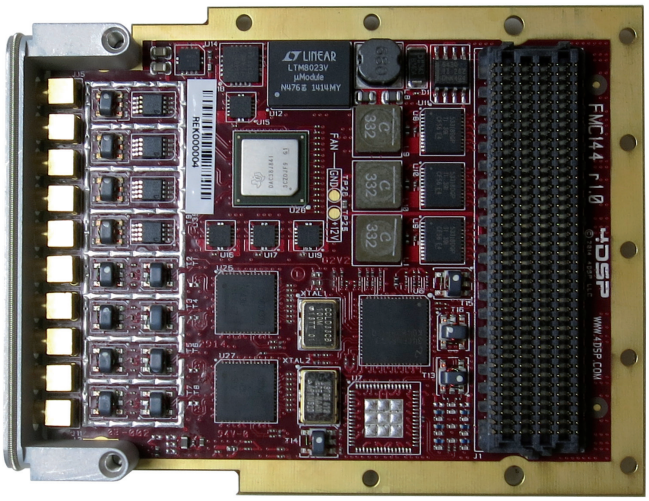

Figure 3: FMC144