RF-Sampling ADCs for Software-Defined Radio

Software-defined radio (SDR) uses software to replace the hardware components of a radio communication system to offer greater flexibility and security, particularly for military communications. By moving many of the previously inflexible signal processing features from analog circuits to software, it is possible to modify their characteristics during radio operation. Instead of using a single radio to receive a particular carrier frequency, bandwidth, and modulation for instance, a flexible digital solution can perform receiving functions over a wide range of frequencies. SDR therefore allows a variety of communications formats and protocols to be supported by one hardware design while enabling MIMO (multiple input/multiple output) solutions. SDR architectures can also be dynamically reconfigured and adapted to multiple air interfaces, enabling active antennas and beamforming for defense electronics, radio frequency (RF) instrumentation, and communications infrastructure purposes, among others.

FMC and FPGA SDR Solutions

The leading approach to defining an SDR application involves coupling flexible digital signal processing (DSP) algorithms with powerful embedded processing capabilities. This means that field-programmable gate array (FPGA) technology plays an important role in the development of SDR platforms. This is due in no small part to the native parallel computational resources available in FPGAs that allow for a programming approach which leverages parallel dataf-low. 4DSP relies on such high-performance, low-power FPGAs from industry-leader Xilinx to power its COTS carrier cards and systems in small form factors such as VPX, PCIe, XMC, and CES.

In an SDR solution, it is important to provide an integrated analog front end to receive the signal from the radio air interface. This functional block sits between the antenna and the FPGA, and is subject to complex and stringent demands as it delivers the signal from the real world to the digital domain. When designing an effective SDR system, it is therefore essential that the interfaces between the FPGA and the analog portion of the board be optimized to realize the best performance in demanding applications.

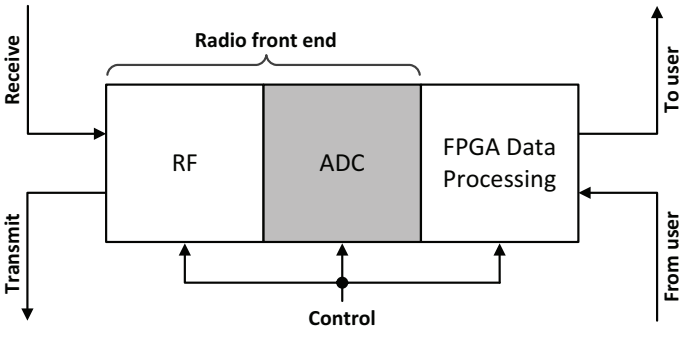

Figure 1: SDR Transceiver

The ideal SDR architecture connects a high-performance analog-to-digital converter (ADC) to the antenna and moves many of the typical RF functions such as filtering, demodulation, and other processing to the digital realm. Due to previous hardware limitations, the analog front end for such a versatile radio historically required an array of overlapping parallel channels. Each channel was dedicated to a particular segment of the RF spectrum, with its bandwidth matched to the required signal format. This approach was costly because of the high PCB footprint and power requirements.

Fortunately, compact and powerful transceiver modules, such as 4DSP's 5Gsps 10-bit FMC170 FPGA mezzanine card (FMC – VITA 57.1), are made possible by modern wideband ADCs and DACs which vastly improve the Size, Weight, and Power (SWaP) profile of SDR systems. A key feature of these powerful converters is that they eliminate several stages of intermediate frequency (IF) downconversion that include mixers, filters, and other components. A Gsps-capable ADC makes it possible to combine multiple narrowband and wideband channels into one ultra-wideband channel. This moves formerly analog channelization onto the FPGA, where frequencies and bandwidths can be dynamically controlled with software to maximize system flexibility and reconfigurability.

Today's transceiver designs rely mainly on a heterodyne architecture in which the RF input signal falls between 700 MHz and many gigahertz before being downcoverted. This drives demand for

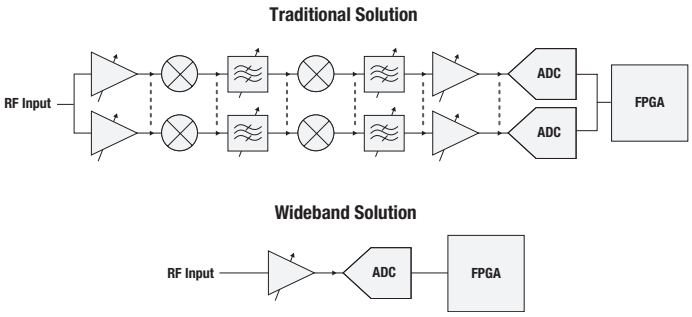

Figure 2: Comparison of a traditional ADC architecture for SDR and a modern wideband SDR solution

the use of SDR in cellular base stations and backhaul point-to-point radios used in wireless network infrastructure, for instance, where the RF bands span from 700 MHz to 3.8 GHz, and allows for the successful implementation of smaller, more efficient form factors that offer higher channel density. Opportunities have also opened up in military applications such as radar, where the 1 to 3 GHz frequency range is used as a secondary IF when downconverting from higher RF bands in 10 GHz to 40 GHz range. Other data acquisition systems and test equipment also benefit.

The obvious advantage of RF-sampling ADCs is their ability to capture large amounts of signal bandwidth directly at radio frequencies, thereby simplifying the signal chain. Another, less apparent advantage is the option to choose a sample rate that is in some cases many times faster than the signal bandwidth. This oversampling capability enables SDR designs to allow for in-band interference that passes through the receiver's filter, thereby improving dynamic range despite low signal-to-noise ratio in some applications. Faster ADC sampling rates also provide ample unused frequency spectrum where a band-limited dither can be placed when it is necessary to boost gain for the purpose of detecting unwanted signals that may fall below the noise floor. RF-sampling ADCs also reduce the amount of anti-alias filtering necessary for the driving amplifier.

Military Applications

There are some fundamental differences between the methods for implementing SDR technology in the commercial, government, and military wireless-market segments. Wireless base stations for commercial cellular services handle heavy traffic in a restricted frequency range while supporting multiple air-interface modes with infrequent system changes. On the other hand, military tactical and battlefield radio systems involve a wide range of frequencies, numerous waveforms, rapid software reconfiguration requirements, and highly dynamic RF environments. Additionally, the necessity for extremely low latency signal processing in military and aerospace applications demands higher performance from COTS hardware and DSP algorithms.

The expanding use of different, incompatible radios poses a significant challenge in military and aerospace settings, where devices or systems may be required for airborne use, satellite communications, and emergency transmitters. Omitting any of these essential radio links can limit effectiveness and potentially safety, but each radio has SWaP requirements that tax the limited available resources. For this reason, SDR has become the go-to solution for military radio designs by enabling universal full-duplex radio systems that can be used across many platforms and reconfigured as needed in the field. This lightens the physical load while providing flexibility, versatility, and increased efficiency.

SDR is a key component of the communications systems of unmanned aerial vehicle (UAV) and, increasingly, unmanned ground vehicle (UGV) platforms. These represent significant areas of growth for the defense industry. Notably, FPGAs rather than conventional processors are becoming a more common choice for handling the demanding real-time processing required by the secure communications systems on UAVs and UGVs because of their ability to provide low latency while maximizing data throughput.

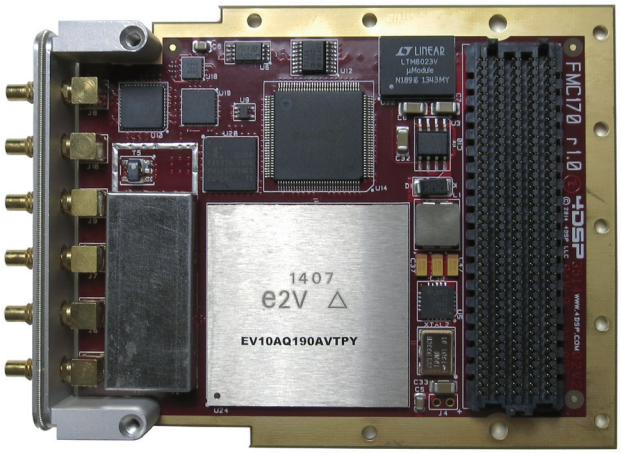

Figure 3: 4DSP FMC170

When combined with wideband ADCs in multiband and cognitive radio systems, they can enable the frequency agility necessary to account for atmospheric effects on RF signals and to contend with interference and jamming.

Additionally, data security and encryption pose real challenges for defense communication systems. Standard wireless protocols are insufficient in this context, so custom waveform modulation techniques must be combined with strong encryption to ensure secure transmissions on the battlefield. This has contributed to the pervasive deployment of SDR in defense and combat scenarios and the development of ever-smaller and faster wideband COTS designs capable of delivering additional functionality as new waveforms are developed and migrated across applications. SDR allows radio equipment makers to more quickly deliver new products that can be reprogrammed and upgraded in the field while remaining compatible with older narrowband platforms.

Commercial Applications

In the commercial and public safety communication segments, mobile device manufacturers are packing more methods of wireless connection into their designs (Bluetooth, WLAN, WiMAX, and GPS, in addition to 3G and LTE broadband) to satisfy the demands of the marketplace. Similar to the military space, this creates increasingly challenging architectural requirements that place a premium on reconfigurability and programmability. While the implementation of multiple wireless standards in a single mobile device presents challenges, the biggest hurdles are found in the mobile network terminal where managing power dissipation and energy use with compact and cost-effective equipment is paramount for an effective design.

The ADC interface is a primary design consideration for mobile terminals because many wireless standards impose requirements that are often more stringent for the receiver chain than the transmitter chain. Data acquisition architectures using modern wideband ADCs can therefore greatly improve the performance of wireless systems, because their high-input bandwidth allows signals to be digitized directly at radio frequency and fast sampling rates reduce filter requirements. In this way, SDR provides a highly flexible and effective wireless testbed for developing mobile communication standards and applications using high-performance wireless transceivers that enable effective designs for next-generation networks.

SDR benefits for network operators:

- Maximize equipment lifespan to minimize costs by ensuring forward compatibility with future wireless standard revisions
- Enable rapid deployment of new services
- Optimize Quality of Service (QoS) by allowing dynamic resource allocation
- Provide advanced spectrum management through flexible spectrum allocation

SDR benefits for wireless base-station equipment makers:

- Enable economies of scale by consolidating product variants onto reconfigurable platforms
- Simplify bug fixes and software upgrades
- Reduce time to market by minimizing the amount of new IP required
- Enable adaptive-antenna support for mobile broadband

4DSP SDR Solutions

Software-defined radio platforms have programmable hardware and software, so a basic SDR architecture can be straightforward, pairing flexible software with a receiver consisting primarily of a low-noise amplifier, a filter, and the ADC. The amplified RF signal is digitized directly without the need for downconversion, a local oscillator, or hardware-reliant tuning. The data can then be processed using different algorithms. The challenge for hardware and software engineers is assembling the best hardware and software for the job. FPGA-based SDR research and development provides a cost-effective way to quickly develop, test and refine new product designs in the laboratory, and ruggedized, low-power boards are ideal for use in the field. 4DSP's FPGA carrier cards, RF-sampling analog transceiver FMC modules like the FMC110, FMC160, and FMC170, as well as an extensive library of proven IP simplify the rapid development of algorithms during SDR system prototyping and field deployment for electronic defense systems, communications infrastructure equipment, and radio frequency instruments.