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A Novel Technology for Soft Recovery High Voltage Diodes

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Abstract

In this paper we present for the first time a newly developed high voltage diode technology, exhibiting soft recovery performance under all operating conditions. The new diode structure is capable of providing the necessary charge for soft recovery behavior by employing the new Field Charge Extraction (FCE) technology. Experimental results obtained from initial prototype samples demonstrate a clear breakthrough in soft recovery performance especially for high voltage diodes rated up to 6500V.

Introduction

One of the main challenges in the design of HV diodes for IGBT applications is to ensure a soft recovery behavior especially under extreme operating conditions. Previous work has shown that under adverse combinations of high commutating di/dt, large circuit stray inductance, low forward current and low junction temperature, it is likely that all fast power diodes produce excessive current and voltage oscillations due to snappy recovery (1). These studies have shown that the depletion of the remaining stored charge during the recovery period results in a current discontinuity (snap-off) with very high di_R/dt and resulting large voltage overshoots. This may produce high levels of EMI in the system or result in the destruction of the device. The soft recovery performance of high voltage diodes degrades significantly as compared to the low to medium voltage class devices. This downtrend is mainly caused by the design trade-off between the need for a high immunity against cosmic ray induced failures and the static and dynamic losses of the diode. In high voltage diode structures, such trade-offs will result in silicon designs having a high resistivity base region combined with the smallest possible thickness. This leads to a low punch-through voltage making the diode more prone to snappy recovery. In state-of-the-art HV diode designs, the only possibility to improve the softness is therefore to increase the diode thickness. Especially in HV diodes, the losses increase very rapidly with the device thickness without resulting in a diode with a clear immunity against snappy recovery when operated under extreme conditions (2). The use of N+ soft punch through (SPT) buffer layers combined with a controlled graded stored charge profile, which results in a soft field punch-through action in the NN+ interface, helps to some extent. Nevertheless, also these designs have limitations in terms of soft recovery. It is obvious that a new design, which breaks the trade-off between recovery losses and softness is needed.

In this paper, we report for the first time, a remarkable breakthrough achieved by combining our SPT technology with a novel cathode emitter design having a combination of N+ and

P+ layers where the electric field is capable of extracting additional carriers from the cathode to maintain a soft recovery performance under all operating conditions. This new technology is therefore termed Field Charge Extraction (FCE). By applying the FCE concept, we believe that future HV diodes can be designed using a significantly thinner wafer specification than what is the case today. This is possible because snappy reverse recovery will no longer present a boundary to the silicon thickness, as is the case by conventional diode structures. In this way, it will be possible to further reduce the diode losses and provide a new performance leap for high voltage fast recovery diodes employed in IGBT applications. In this paper we present the new FCE technology concept, simulations results and experimental results obtained from some initial 6.5kV prototype samples employing the new FCE cathode design.
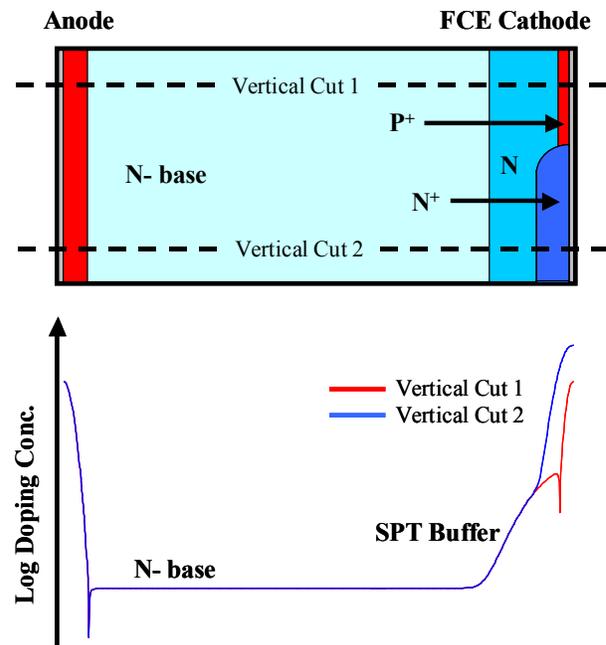

Figure 1: Cross section of the FCE diode structure

The FCE-Diode Concept

A. The FCE Diode Structure

A cross section of the new high voltage FCE diode is shown in fig. 1. The anode design employs a highly doped P+ emitter where the emitter efficiency is adjusted by local lifetime killing using He++ irradiation. The lifetime in the N-base region was homogenously adjusted using electron irradiation. The FCE structure on the cathode side consists of an SPT-buffer and a combination of P+ and N+ contact areas on the

semiconductor surface. The P+ and N+ areas are electrically connected (shorted) to each other by the cathode metallization. Electrically, the N+ areas thereby function as the cathode emitter of the PiN diode, whereas the P+ areas act as the emitter of a PNP bipolar transistor. The N-buffer underneath the P+ emitter acts as the base and finally, the PiN-diode anode represents the collector of the PNP transistor. In this way, a hybrid structure consisting of a PiN diode in parallel with a PNP bipolar transistor is created. In simple terms, when compared to a conventional diode, the FCE cathode structure has additional P+ islands in the cathode contact area. It is important to point out that the FCE structure is based on a combination of diffusion profiles and does not depend on any external controlling.

B. The FCE Diode Operation Principle

During forward conduction in a conventional PiN diode, the N-base gets flooded with excess carriers. The concentration will depend on the emitter efficiency of the anode and cathode emitters. In the FCE diode the current can only flow in the N+ contact areas of the FCE cathode. In the areas underneath the N+ contact areas, the excess carriers in the N-base will reach the same level as in a standard diode. In the areas underneath the P+ regions, the excess carriers will only reach levels corresponding to the concentration of the SPT-buffer. The average excess carrier concentration on the cathode side of the FCE diode will therefore be lowered and hence the on-state voltage drop will be higher compared to a standard diode. In spite of this, the overall trade-off between on-state and reverse recovery losses will be better in the FCE diode as will be shown in the next sections. The on-state voltage of the FCE diode will depend on the SPT buffer concentration, and the area ratio of the P+ and N+ cathode regions.

During the recovery phase, electrons initially stored in the N-base, will flow towards the FCE cathode and thereby preferably pass into the cathode contact through the N+ regions. At the end of the recovery phase, when the electric field starts coming close to the cathode, the gain of the internal bipolar transistor will increase and trigger an injection of holes from the P+ areas. This hole current will add to the reverse recovery current originating from the stored excess carriers and in addition slow down the depletion of the excess carriers underneath the P+ areas of the FCE cathode. In conventional diode structures, the stored charge eventually gets too small to keep up a continuously decreasing reverse current as the electric field propagates towards the cathode resulting in a current snap off. In the FCE cathode, the current from the stored charge will additionally be supported by the current injected by the P+ emitter and in this way a soft recovery will be achieved. For the recovery characteristics of the FCE diode, it is important that the average excess carrier concentration increases from the anode to the cathode side of the diode. This is to prevent a space charge region from building up at the cathode side in the beginning of the reverse recovery phase. This would inevitably lead to undesirable reverse recovery characteristics with a large reverse recovery peak current (I_{RR}) as presented in a previous article (3). In the case of the FCE diode the anode emitter efficiency was adjusted using a local lifetime killing with He++ ions.

C. Trade-off Between Softness and Electrical Losses

For any diode technology, the reverse recovery softness has to be traded off against the total electrical losses. At a first glance, the FCE cathode concept has two disadvantages in terms of losses as compared to a standard diode technology. Firstly, the on-state voltage drop will be higher and secondly the P+ areas will inject additional holes at the end of the recovery phase, both adding to the total losses of the diode. On the other hand, the big reduction of the excess stored charge near the cathode side during the conducting state will significantly reduce the reverse recovery losses of the FCE diode. During reverse recovery, the carriers near the cathode are extracted at a later stage, which means that they contribute the most to the recovery losses. Different techniques have been developed to control the stored charge near the cathode (4), (5), (6). However, in conventional diodes, lowering the cathode side plasma inevitably leads to snappy reverse recovery behavior. Thanks to the hole emitting P+ areas, the FCE diode does not depend on the remaining excess carriers to support the reverse recovery current. Therefore, the FCE diode can have a low excess carrier concentration on the cathode side without suffering from snappy recovery. Device simulations show that an optimized FCE diode will have lower total losses under nominal switching conditions than a diode with a conventional cathode. The biggest advantage of the FCE diode is, however, the fact that it can be made even thinner than a normal diode without losing any softness. In this way, it will be possible to further improve the trade-off relationship between losses and softness in future diode designs using the FCE concept.
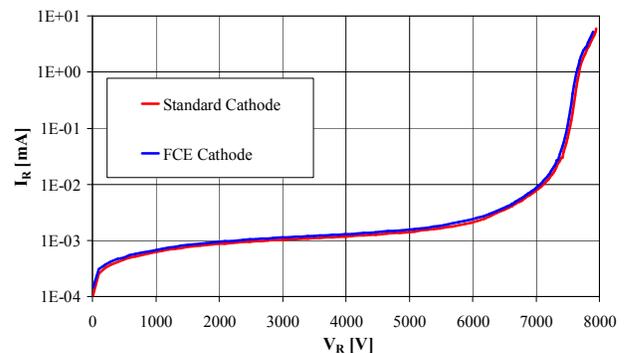

Figure 2: Measured blocking characteristics of a standard 6.5kV diode and a 6.5kV FCE diode

D. Blocking Voltage and Leakage Current

The FCE cathode was carefully designed to prevent the P+ areas from becoming active under static blocking conditions when no significant current is flowing in the diode. Therefore, the FCE diode has normal blocking characteristics as the measured blocking waveforms in fig. 2 show.

E. Simulation Results

Fig. 3 shows a simulated recovery current waveform of a 6.5kV FCE diode. As a comparison, a standard diode is shown as well. The simulation was made at a low forward current (5A) and a high DC-rail voltage (4400V). The stan-

dard diode shows a clear snap-off at 3.1us, whereas the FCE diode shows a continuously decreasing recovery current. The reverse recovery of the FCE diode can be divided into three phases. In phase 1, from t=0.0 to 2.4us, the reverse recovery current of the FCE diode is similar to the standard diode's one. The level of the current tail is slightly lower, which reflects the lower excess carrier concentration of the FCE diode. In this stage, the electric field penetrating edge is still far from the SPT buffer and therefore, no significant hole current is injected by the P+ regions. In phase 2, the bipolar transistor starts to become active. During this phase, the reverse recovery current consists of two parts: The current from the removal of the excess carriers and an additional current injected by the FCE cathode. In the third phase, the stored charge underneath the N+ contact areas has been completely extracted and the electric field "punches through" to the SPT buffer layer in the N+ contact areas. Normally at this stage, a conventional diode would "snap-off" and cause extensive oscillations. In the FCE diode this does not happen thanks to the injected hole current and the remaining stored carriers underneath the P+ areas, which both enable the recovery current to smoothly decrease to zero. A small current discontinuity at t=3.2us marks the transition into this third phase.
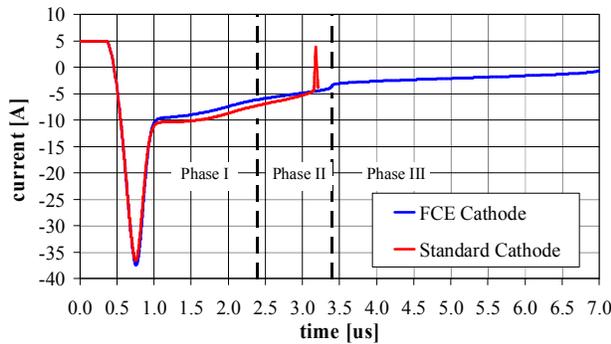

Figure 3: Simulated reverse recovery current waveforms. Comparison between a standard diode and an FCE diode

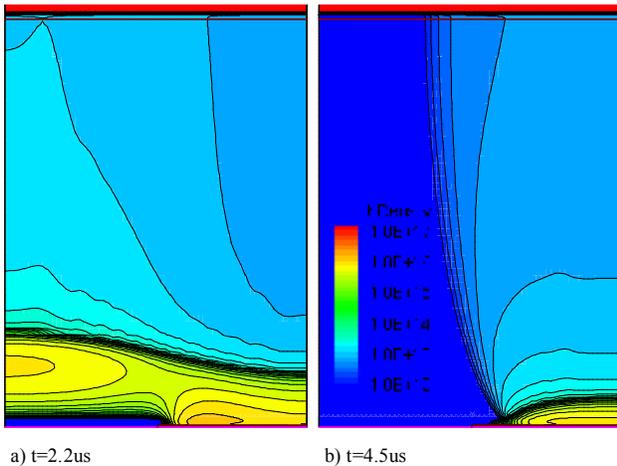a) t=2.2us   b) t=4.5us

Figure 4: Simulated hole concentration during reverse recovery in the FCE diode

Fig. 4 shows the simulated hole density in the FCE diode in the first recovery phase (fig. 4a) at t=2.2us as well as in the third phase (fig. 4b) at t=4.5us. At t=2.2us, a large mountain of remaining excess carriers still exists underneath the N+ contact. On the other hand, at t=4.5us, the area underneath the N+ contact has been completely depleted and the electric field has reached through to the SPT buffer layer. The reverse recovery current is now only supported by the remaining carriers underneath the P+ emitter and the slowly decreasing bipolar injection of the P+ areas.

Electrical Results

To demonstrate the FCE concept experimentally, 4.5kV and 6.5kV FCE diodes were fabricated. Fig. 5 shows the reverse recovery waveforms of a 6.5kV FCE diode. As references a standard diode, having a strong, continuous (unstructured) cathode and a diode with a weak continuous cathode are shown as well. The test was conducted using a high DC-rail voltage and a low forward current, conditions critical in terms of snappy recovery. All three diodes were fabricated using the same silicon specification and anode-side processing. It is clear, that the FCE diode shows a softly decaying current tale at the point where the other two diodes tend to snap-off.
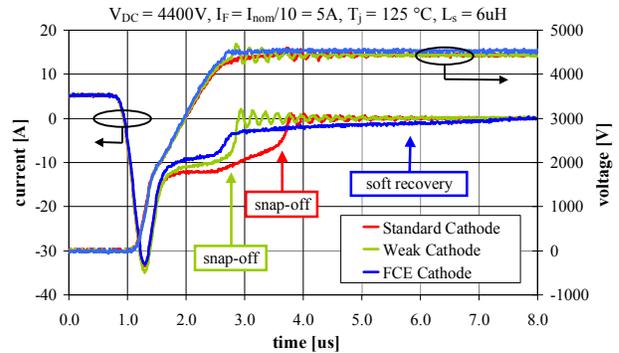

Figure 5: Comparison of the softness of a 6.5kV FCE diode, a standard diode and a diode with a weak cathode

Fig. 6 shows the reverse recovery waveforms of the three diodes under nominal switching conditions. Compared to the standard diode, the FCE diode shows a significantly lower current tail and therefore lower recovery losses. This effect is due to the fact, that the excess carrier concentration is reduced on the cathode side of the FCE diode during the forward conducting state because of the P+ areas. Normally a high charge mountain on the cathode side should prevent snappy recovery. It is however clear that the FCE diode has a much softer behavior than the standard diode although the stored charge on the cathode side is much lower. The diode with the weak cathode has similar reverse recovery losses under nominal conditions as the FCE diode. However, without the supporting P+ islands this diode shows a very snappy recovery under adverse conditions (fig. 7).

Although the P+ areas of the FCE diode inject some holes even under nominal switching conditions, thanks to its better excess carrier distribution, the FCE diode still has 40% lower recovery losses than the standard diode.
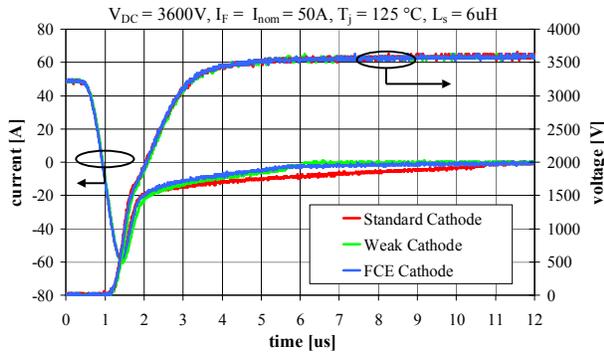
Figure 6: Reverse recovery under nominal conditions

The on-state characteristics of the FCE diode are shown in fig. 8. The FCE diode exhibits a strongly positive temperature coefficient of V_F, a feature that the standard diode does not have. This is yet another advantage of the FCE cathode compared to the standard technology. The on-state voltage drop at 50A and 125 °C of the standard diode and the weak cathode diode is 4.0V and 4.3V respectively, as compared to 5.0V for the FCE diode. Clearly, the FCE diode has a significantly higher on-state voltage drop than the standard diode. However, the recovery losses are much lower and altogether, the FCE diode ends up on a slightly better technology curve than the standard diode.
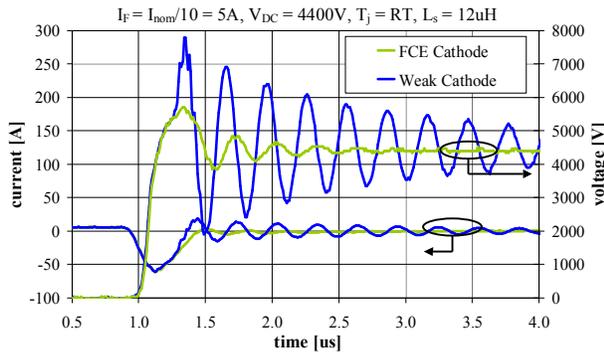

Figure 7: Reverse recovery under worst-case conditions in terms of snappy diode recovery
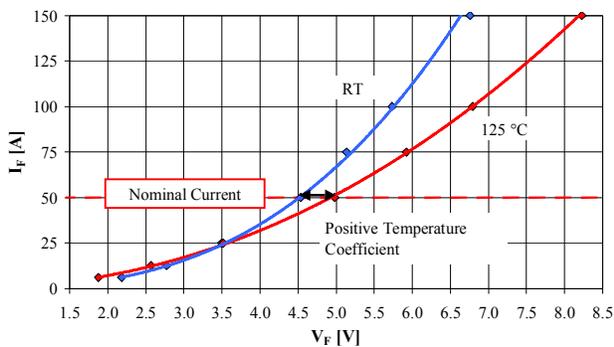

Figure 8: Forward characteristics of the 6.5kV FCE diode

Finally, in fig. 9 a reverse recovery waveform of the 6.5kV FCE diode under SOA conditions is presented. It is clear that the FCE diode does not suffer from any inherited design weakness when compared to its conventional counterpart (7),

(8). A high SOA performance was obtained even when the diode was tested under extreme conditions. It must nevertheless be pointed out that second breakdown of the internal bipolar transistor can be a possible SOA detractor if the P+ areas of the FCE cathode are not designed properly. On the other hand, the injected holes can possibly prevent failures associated with the distortion of the electric field as reported in (7).
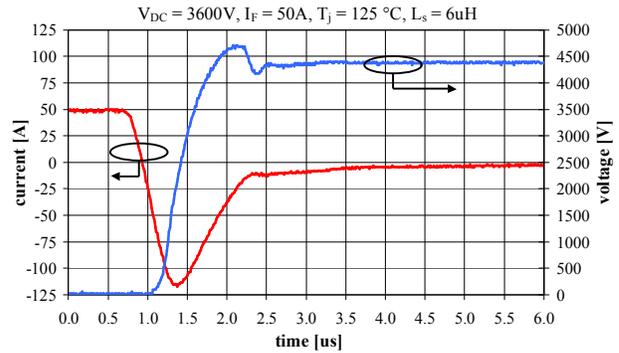

Figure 9: Reverse recovery SOA of the FCE diode

Conclusions

In this paper we presented the newly developed FCE (field charge extraction) diode concept, which allows a soft reverse recovery behavior under all operating conditions. The FCE structure comprises N+ and P+ islands on the cathode side of the diode. Especially at the end of the reverse recovery phase, the P+ islands start to emit holes, which support the reverse recovery current and prevent a snap-off. The presented new soft recovery behavior will provide a new performance advantage long awaited by system designers especially for high voltage fast recovery diodes employed in IGBT applications.

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