SECTION 4

RELIABILITY AND TESTING

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RELIABILITY AND TESTING

4.1 Semiconductor Component Reliability

High Power Semiconductors are normally used in applications where high reliability is a must. Power electronic circuits for industrial drives, locomotives, and energy transmission and distribution systems are just the most prominent examples of such demanding environments.

A widely used reliability criterion is the component **hazard rate** (or failure rate). System designers often require a component failure rate in the range of 10 to 100 FIT (1 FIT = 10^{-9} h^{-1}). Evaluating field experience with GTOs, failure rates between some 10 and some 100 FIT for equally designed and processed devices have been observed, depending strongly on the environmental and operational load conditions.

Thus, for the purpose of reliability planning or prediction, it should be understood that the failure rate is not just an attribute of the component itself, similar to an arbitrary data-sheet parameter. To achieve a low failure rate always requires close technical co-operation between component supplier and user, in the system development phase, aiming for a robust relation between component strength and operational load.

Basic Concepts of Component Reliability

One of the essential paradigms is the distinction between **intrinsic** and **extrinsic failures**:

- *Intrinsic failures occur after component delivery, they are related to component design and manufacturing, and are provoked in circumstances within the component's design specification.*
- *Extrinsic failures are typically related to static or dynamic overload events (electrical, thermal, mechanical, radiative), during the component life cycle, or due to misapplication (wrong component for the job).*

The distinction between intrinsic and extrinsic failures is important, because it points to possible causes of failure, and therefore indicates the direction of corrective actions.

The other important paradigm used in describing failures is a **lifetime pattern**, identifying three phases according to the evolution of the failure rate over time:

- *the **early life**, with an essentially decreasing failure rate,*

- *the **useful life**, with a relatively constant failure rate,*
- *the **long-term wearout**, with a (rapidly) increasing failure rate.*

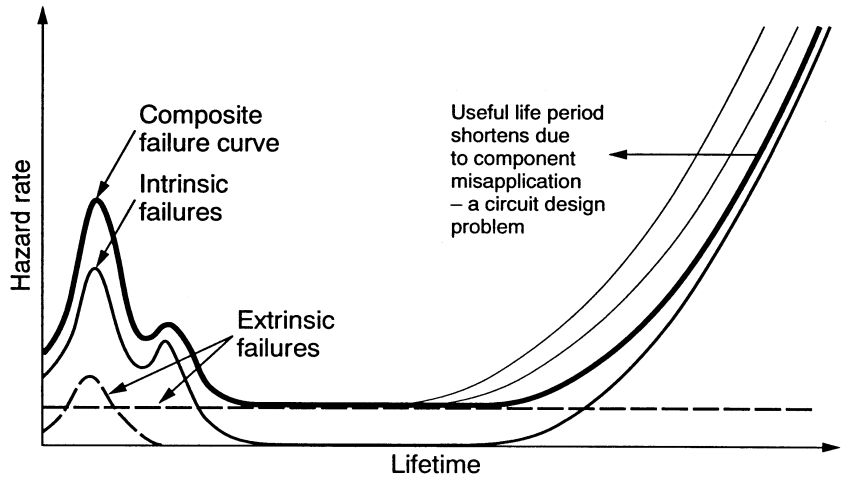
This pattern is well known either as bath-tub curve or as **roller-coaster curve** (if one or more humps occur during the early life, which is often the case with electronic components).

The field failure classification scheme used at ABB Semiconductors combines both concepts:

Infant Mortality Failures Decreasing failure rate	**Useful Life Period Failures** Constant failure rate	**Wearout Failures** Increasing failure rate
Intrinsic failures, i.e. component failed in service due to macro-defects (caused by manufacturing flaws). <u>Examples for GTOs:</u> Embedded particles leading to gate-to-cathode shorts Weak passivation leading to degradation of blocking capability (voids, scratches, particles, ionic contamination, partial discharge) Structural inhomogeneities (segments, p-base, anode shorts) leading to failures during switching **Extrinsic failures**, i.e. component failed in service due to mechanical, thermal or electrical overload. <u>Examples for GTOs:</u> Inhomogenious clamping Incorrect operation of gate-drive Control algorithms leading to operational states outside the SOA	**Extrinsic failures** dominate, i.e. component failed in service due to transient overload (electrical, thermal, mechanical, radiative). <u>Examples for GTOs:</u> Transient situations with voltage V, dv/dt Transient situations with current I, di/dt Transient situations with temperature T, ΔT, dT/dt Cosmic ray induced voltage break-down EMI related noise signals on gate terminal, leading to unwanted triggering	**Intrinsic failures** dominate, i.e. component failed in service due to wearout failure mechanisms. <u>Examples for GTOs:</u> Fatigue of finger metallisation, raising the risk of gate-to-cathode shorts Degradation of the high voltage insulation properties (e.g. change in the inner atmosphere due to loss of hermeticity, induced damages in silicon due to repeated surge current or di/dt events) Contact electromigration (at Ni-Al interface to heat-sinks) Degradation of oxide between gate and cathode contacts, drift of trigger current Solder joint fatigue (leads) Corrosion

The time range for infant mortality failures is up to about a thousand hours, 100 days being a reasonable first approximation. An useful life period of more than 20 years is achievable for GTOs, however this period may shorten significantly, if components are misapplied.

In summary, the implications of intrinsic and extrinsic reliability can be illustrated as shown in the following figure. The solid thin line indicates the intrinsic reliability in a particular field environment. The dotted lines show the extrinsic failures (additional infant mortality plus freak loads generating a constant hazard rate). The solid heavy line illustrates the resulting pattern of field failures, i.e. the **composite hazard rate**, including those situations where misapplication of the component moves the wearout period to the left.



Intrinsic, extrinsic and composite reliability curves for component hazard rate in a field operating environment (after: Jensen F., Electronic Component Reliability, John Wiley & Sons, 1995)

4.2 Reliability in Development

Quality and reliability of semiconductor devices are determined to a large extent during the design stage: accordingly these aspects are of primary focus in the development cycle. This has been reflected in the *Development Process Model,* established and followed at ABB Semiconductors.

Thus, at design stage, thorough *Planning for Quality and Reliability* is executed and documented, and all design results are subject to formal, systematic and critical *Design Reviews* at the conclusion of each design phase.

Verification by appropriate experiments and routine testing according to standardised *Inspection and Test Requirements* (see 4.6), are performed in the course of the development cycle.

Design for Reliability and *Design for Manufacturability* are the two main concepts and methodologies applied.

Design for Reliability

When reliability problems turn up during the system qualification phase at a customer's site, this engenders not only a loss of confidence and image, but also represents a loss of precious time to market.

ABB Semiconductors strives to avoid this situation by proactive engineering at early stages of development. This includes:

- *use of well documented and standardised process steps;*
- *use of "predictable" technologies in, for instance, junction termination, doping, passivation etc.;*
- *adequate safety margins in design rules based on root cause analysis of failure modes;*
- *use of state of the art methodology and analytical equipment;*
- *use of state of the art modelling and simulation tools to compute electrical, thermal and mechanical stresses;*
- *Failure Mode and Effect Analysis (FMEA) at an early stage of development.*

High power semiconductors are often used in products with an extremely long product lifetime. This means that not only failure rate, but also product lifetime, must be factored into the product design criteria. The systematic investigation of wearout mechanisms, and the use of wearout resistant designs and technologies, is thus of utmost importance. The study of wearout mechanisms and their modelling often require special know how in materials science, which is not universally available. In this domain, ABB Semiconductors co-operates with ABB Corporate Research, and with other leading academic groups.

Design for Manufacturability

A key design goal is to have *one basic process sequence* for each product group (PCT, GTO and diodes). The main product-to-product variables are then masks, silicon specification, implantation dose, e-doping dose etc. The generic processes, however, remain fixed and standardised (e.g. lifetime control with e-doping only, standardised diffusion temperatures).

Simulation, modelling and statistical tools are used to perform a sensitivity analysis of electrical performance versus process variation, in order to define design rules and required process capabilities.

Theoretical cycle time is an important criterion in any new product design. Minimising theoretical cycle time not only brings cost-reduction, but also reduces the complexity of process and logistics, and increases reliability.

Theoretical yield has to be maximised, by setting specs such that there is a sufficient margin between typical values and specified values. A high theoretical yield is a prerequisite for a stable and predictable production process, and thus is a necessary condition for product quality and reliability.

4.3 Reliability in Manufacturing

Based on a master schedule and backlog, the manufacturing department commits to meet a customer's requirements regarding product quality, costs and service quality. Materials, wafer fabrication, assembly, final testing, environmental condition, and production facility are all carefully controlled. Whenever possible, statistical methods of control are applied.

Material Control

After thorough evaluation and qualification, all materials are purchased according to ABB Semiconductors in-house specifications. All suppliers have to be approved. Suppliers for key materials (e.g. silicon, ceramic housings, molybdenum) have to participate in a certification process, and thus be committed totally to ABB Semiconductors success. This includes periodic auditing of the suppliers quality management system, facilities and product quality.

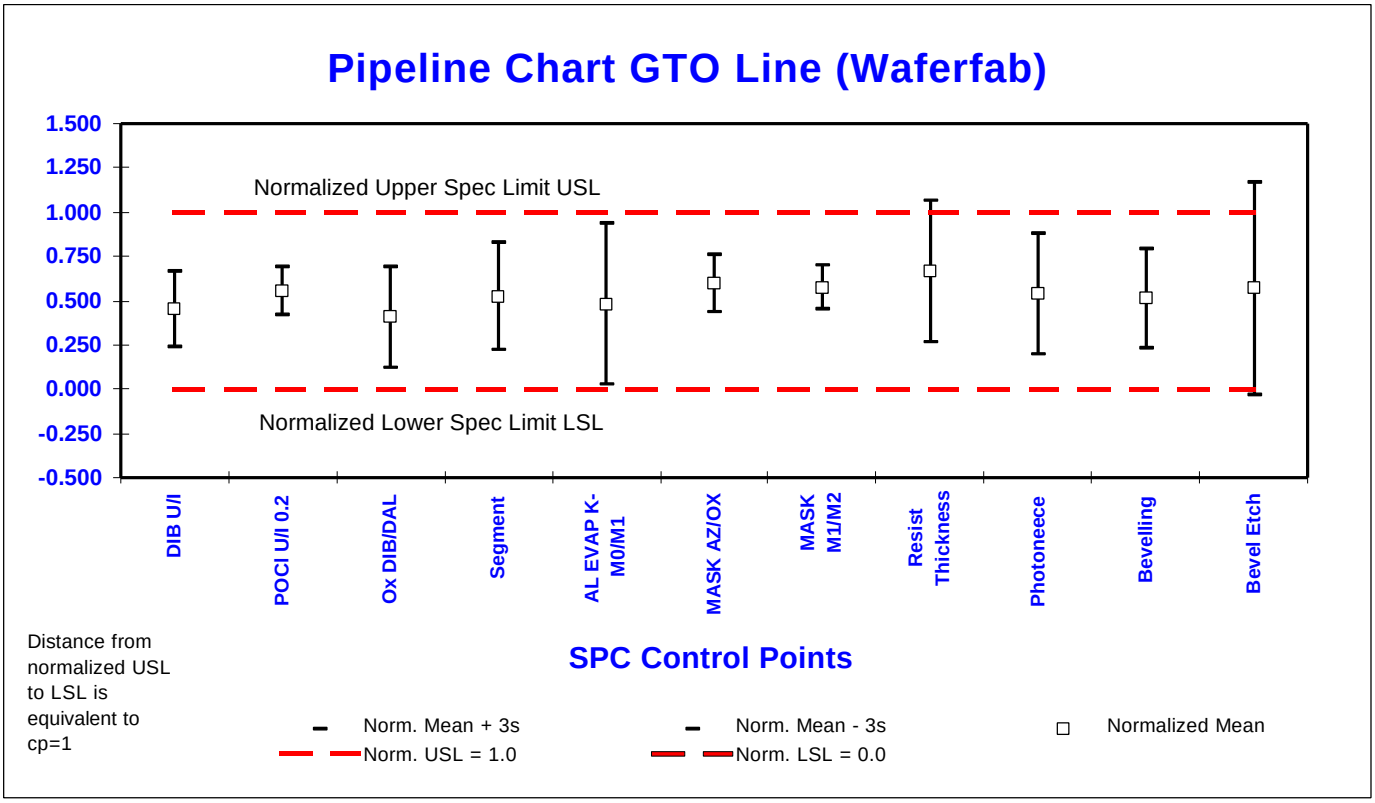
In-Process Control

The quality of a product is built-in during the manufacturing and assembly stage. The basis for each lot run sheet is a type-generic product flow chart, where all operations and control points are

specified. Inspection results at the control points are plotted at the work station on xbar/-R-charts. This data is the driver for continuous improvement in the process capability. The following table shows the most important manufacturing steps, and the corresponding SPC measurement and/or monitors:

Process Steps	**In-Process Inspections/Monitors**
Oxidation	- visual - thickness
Photolithography	- mask and wafer cleanliness - alignment and focusing accuracy - critical dimensions
Etching	- quality of etching and wafer cleanliness - critical dimensions
Doping by Implant and/or Diffusion	- sheet resistance
Metallisation	- wafer cleanliness - thickness - visual
Passivation	- wetting - passivation integrity (pores) - adjustment
Edge contour	- critical dimensions
Wafer Inspection	- visual (microscope surface inspection)
Electrical Characterisation	- R-Test - VGR Inspection

For relevant product lines, SPC measurement results, and process capability indices for all Critical-to-Quality parameters, are entered into monthly **Pipeline Charts**, in order to indicate the control status of the manufacturing processes (see below).



Environment Control

Particles, humidity, temperature and water purity are statistically controlled. Material used and material wasted respect both Swiss and the customer's country legislation. ABB Semiconductors Environmental Management System is certified according to ISO 14001 (since July 1996)

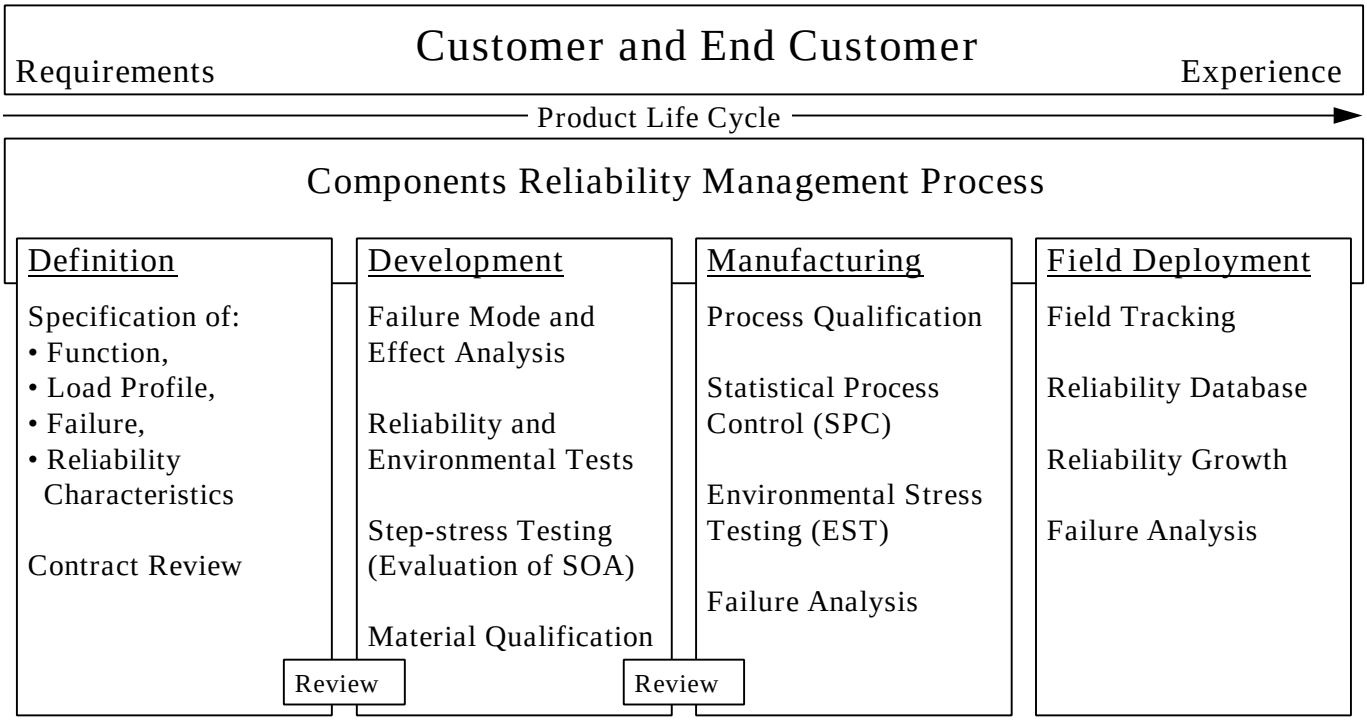
Equipment Control

Equipment, facilities, and instrumentation are statistically controlled. Preventive maintenance is executed according to a predefined plan. Periodically, a Measurement System Analysis is performed for all equipment used for electrical testing, in order to guarantee accuracy, repeatability and reproducibility. If an equipment breakdown occurs, recovery and re-qualification follows a predefined process.

4.4 Reliability Management Process

ABB Semiconductors' Reliability Management Process is designed to cover the entire life cycle (up to 30 years) of a product, starting with the initial checklist of requirements, and finishing with the final evaluation of field experience.

As illustrated in the Fig. below, the Reliability Management Process is orthogonal to other company processes, like Product Definition, Development, Manufacturing and Customer Service (Field Deployment). The process utilises individual sub-processes from other processes, but at the same time adds or superimposes unique and challenging elements (e.g. stringent qualification and test procedures for materials, products, and processes, as well as advanced methods and tools for failure analysis).



Effective Reliability Engineering demands special skills and knowledge, acquired from a plethora of different engineering sciences. To fulfil this requirement, special reliability training is given

in-house, and a close co-operation has been established with the Reliability Laboratory of the Swiss Federal Institute of Technology in Zürich, one of the leading European institutes in this field.

ABB Semiconductors' Reliability Management Process reflects the guidelines contained in International Standard IEC 300-1 (also published under ISO 9000-4).

Communication, Quality Indicators

Reliability Management requires an effective system of communication, between the supplier (design and manufacture), and the customer (application). Quality indicators monitor the progress and efficiency of all kinds of improvement activities. ABB Semiconductors uses the following indicators for product quality and reliability:-

Feed forward:

- SPC information on Critical-to-Quality parameters (Pipeline Charts),
- Parameter spreads (electrical performance),
- Component strength distributions (vs. mechanical, thermal and electrical loads)
- Product qualification status reports (results of characterisation, environmental and reliability testing).

Feedback:

- Customer's incoming inspection results,
- Line fall-off rates,
- Field failure rates,
- Customer complaints.

Traceability

Traceability, from semiconductor production, assembly and test, to the customer and into service, is guaranteed by relating all manufacturing and test data to the unique and individual batch and device number. This number is engraved on the surface of each component.

Failure Analysis

Should anomalies be detected at the customer's receiving inspection, in his production line (test of sub-systems or systems), or as field failures, ABB Semiconductors' Quality and Reliability Department focuses the company's resources on identifying the root cause of failure, and in implementing corrective actions. Using circumstantial information from the customer, together with state-of-the-art analytical techniques, such as electron beam microscopy and EDX analysis, the Failure Analysis Lab establishes a failure analysis report, which is sent to the customer and circulated internally to initiate corrective actions, where required.

Design or Process Changes and Customer Notification

Changes to product, or process, can only be implemented after a change proposal is formally approved (part of the Engineering

Change routine). Normally, sample products are evaluated, to confirm that they conform to the quality and reliability specifications. Where such changes are significant, with respect to performance and/or reliability, the customer will be notified.

Product Qualification Status Reports

ABB Semiconductors' Quality and Reliability Department reports annually on the actual qualification status of all generic products, with respect to Group D test and inspection requirements (see 4.5). Results can be communicated to customers through the Sales Organisation.

4.5 Electrical Testing in Production

The basic test methodology at ABB Semiconductors (refer to "General Quality Specification for High Power Semiconductors" and to IEC 747-6) is based on four generic test levels:

Group A Testing:	100% Routine Test for all manufactured devices
Group B Testing:	Lot Control Test (scheduled product audit)
Group C Testing:	Qualification Maintenance (bi-annual) (see 4.6)
Group D Testing:	Qualification Approval Test (see 4.6)

Group A Testing

Electrical parameter testing is performed at the wafer level, on a sample basis, before and 100% after electron irradiation.

After having completed all assembly operations, the devices go into a severe final test sequence, as defined in the table below:

Examination or Test		Reference Documents or Test Conditions	Inspection Requirements	
Sub-group	**Description**		**Level or AQL**	**Note**
A1	Final Electrical Test (static and dynamic parameters)	Individual test specification per article (5SYH 5xxx series)	100%	
A2	Environmental Stress Test (frequency test)	Individual test specification per article (5SYH 5xxx series)	100%	
A3	Endurance: DC blocking	V_{DC} = 0.8 V_{DRM}, T_{case} = 90°C, t = 3 h	100%	Traction only

Parametric testing uses state-of-the-art test automatic equipment. The following parameters are tested:-

- Static at 25°C: V_{GR}, V_{DS}, V_{GT}, I_{GT}, V_T
- Static at 125°C: I_{GR}, I_{DS}, V_{GT}, I_{GT}, V_T
- Dynamic (turn-on) at 125°C: t_d, t_r, E_{on}, di/dt
- Dynamic (turn-off) at 125°C: I_{GQM}, I_{tl}, t_s, t_f, t_{tl}, V_{DSP}, E_{off}, V_{DM}, di_{GQ}/dt

Parametric testing can be customised, incorporating special or additional test conditions required for the application.

Test Data Management

The usage of SPC in Wafer Fab (see 4.3), and the need to link electrical data from device testing to manufacturing process data, for the purpose of modelling and understanding cause-and-effect relationships, led to the implementation of SyQua™ (a company-wide Quality Data Management System). The system stores all relevant data in a common database, which represents a powerful tool to improve, and shorten, the feedback loop from electrical product characteristics to manufacturing process parameter settings. All relevant GTO test equipment is connected to SyQua™ enabling data retrieval and statistical analysis.

Frequency Testing

In the *frequency test*, GTOs are stressed under life-like conditions, as would be found in a locomotive, or in an industrial drive. In contrast to parameter testing, where devices are exposed to single shots for measuring turn-on and turn-off parameters, the frequency test, as its name implies, switches DUTs *repetitively* on and off at rated current, with a switching frequency of 150 to 300 Hz, depending on the type of GTO and its specific load profile.

By repetitively stressing GTOs with turn-on, on-state, turn-off and off-state losses, it is possible to detect device weaknesses, like the appearance of hot-spots, which cannot be found in single-shot or endurance testing. Also, since the gate-to-cathode voltage is repetitively driven into avalanche breakdown during turn-off, the cathode segment gate-to-cathode pn-junctions are stringently tested with respect to their blocking performance. This stress, furthermore, occurs over the wide temperature range of approximately 20 °C, at the beginning of a test cycle, to near the maximum junction temperature, at the end of the test cycle.

Thus, since it is performed on *every* device leaving the factory, the frequency test is a very effective means to screen out GTOs which would probably fail either during equipment commissioning, or when operated at their maximum ratings.

Typical load profile for a 3 kA GTO:

- Snubber circuit: Undeland, $C_{s(eff)}$ = 4.9 µF
- Test duration: 3 min
- Mounting force: 32 kN
- Pulse mode: double pulse
- Frequency: 180 Hz (switching)
- I_{TGQ1}, I_{TGQ2}: 2800 A, 3000 A
- V_{DM1}, V_{DM2}: 4500 V, 4500 V
- V_{DC}: 3900 V
- t_{on1}, t_{on2}: 300 µs, 350 µs
- di/dt1, di/dt2: 10 A/µs, 550 A/µs
- di_{GQ}/dt: 40 A/µs

From a test methodology point of view, frequency testing has proven to be the most appropriate implementation of EST (Environmental Stress Testing) for GTOs.

Group B Testing

Lot Control Tests are performed on a regular basis, in order to monitor ongoing production from a reliability perspective.

Examination or Test		Reference Documents		Inspection Requirements		
Sub-group	**Test Category**	**IEC** ***MIL 750C*** ***JIS C 7021***	**Conditions**	**n**	**c**	**Notes**
B1	Endurance: AC blocking	Internal Ref.	24 h at $T_C = T_{vj}$ max Sine wave 50 Hz V_D = 0.7...0.8 V_{DRM}	8	0	Note 1
B2	Endurance: DC blocking	Internal Ref.	24 h at T_C = 80°C...T_{vj} max V_D = 0.7...0.8 V_{DRM}	8	0	Note 1

4.6 Qualification Testing

Qualification testing is performed during product development (Group D or *Qualification Approval Testing*), and over the whole product life cycle (Group C or *Qualification Maintenance Testing*).

Group D Testing

Examination or Test		Reference Documents		Inspection Requirements		
Sub-group	**Test Category**	**IEC** ***MIL 750C*** ***JIS C 7021***	**Conditions**	**n**	**c**	**Notes**
D1a	Characteristics inspection	Internal Ref.	Parameters and quantities see applicable test specification			
D1b	Complementary characteristics inspection	Internal Ref.	Parameters and quantities see applicable test specification			
D1c	Verification of maximum ratings	Internal Ref.	Parameters and quantities see applicable test specification			
D2	Endurance: Storage at high temperature	68-2-2 *1031.4* *7021 B-10*	1000 h at T_{stg} max	10	0	Note 1
D3	Endurance: Storage at low temperature	68-2-1 Aa *7021 B-12*	500 h at T_{stg} min	10	0	Note 1
D4	Endurance: AC blocking	747-6 V	1000 h at T_{vj} max Sine wave 50 Hz V_D = 0.7...0.8 V_{DRM}	8	0	Note 1
D5	Endurance: DC blocking	*1048* *7021 B-20*	1000 h at 90°C...T_{vj} max V_D = 0.7...0.8 V_{DRM}	8	0	Note 1
D6	Endurance: DC blocking	Internal Ref.	1000 h at T_C = 25°C $V_D = V_{DRM}$ (or derated voltage)	30	Calculated	Note 4
D7	Endurance: Thermal cycling load (Thermal fatigue)	747-6 IV, 4 *1037.1* *7021 B-18*	ΔT_{vj} = 80°C ... 100°C $1 \cdot 10^5$ cycles (Traction) $0.2 \cdot 10^5$ cycles (Industry)	12	0	Note 1
D8	Operating life	Internal Ref.	$1 \cdot 10^6$ on/off cycles with I_{TGQM} and V_D max, specific drive and snubber circuits	10	0	
D9	Rapid change of temperature	68-2-14 Nc *1056.2* *7021 A-3*	0°C to 100°C, 15 cycles, liquid to liquid	10	0	Note 1
Examination or Test		**Reference Documents**		**Inspection Requirements**		

Sub-group	Test Category	IEC *MIL 750C* *JIS C 7021*	Conditions	n	c	Notes
D10a	Shock	68-2-27 Ea *2016.2* *7021 A-7*	Components in stack a = 30 gn, 18 ms, 3 shocks per direction	4	0	Note 2
D10b	Vibration (random)	WG 21 9-335-CD	Components in stack 5 to 20 Hz, a ≤ 1.034 g^2/Hz 5 to 150 Hz, a ≤ 5.9 g_{RMS} 300 min	4	0	Note 2
D10c	Vibration (sinus)	68-2-6 Fc *2056* *7021 A-10*	Components in stack 10 to 500 Hz, d ≤ 0.35 mm, a ≤ 5 gn, 10 cycles per axis, 120 min	4	0	Note 2
D11a	Shock	68-2-27 Ea *2016.2*	Components in transport box a = 30 gn, 18 ms, 3 shocks per direction	4	0	Note 2
D11b	Impact Shock (Bump)	68-2-29 Eb	Components in transport box a = 15 gn, 6 ms, 4000 shocks per direction	4	0	Note 2
D11c	Vibration (sinus)	68-2-6 Fc *2056*	Components in transport box 10 to 500 Hz, d ≤ 0.35 mm, a ≤ 5 gn, 10 cycles per axis, 120 min	4	0	Note 2
D12	Salt mist	68-2-11 Ka *1046.2*	35°C, 5% NaCl, 7 days	4	0	Note 3
D13	Robustness of terminations	68-2-21 *2036.3 A* *7021 A-11*	Tension, 40 N, 10 s	4	0	

Notes:

1.) Failure criteria for Diodes: I_{RRM} (T_{vj} max) < 1.1 USL
V_{FM} < 1.1 USL

Failure criteria for Thyristors: I_{RRM}, I_{DRM} (T_{vj}max) < 1.1 USL
I_{GT}, V_{GT} (25°C) < 1.1 USL
V_{TM} (T_{vj} max) < 1.1 USL

2.) Failure criteria for all Press-pack devices: Integrity of package materials, wafers, sealing, lead connections. The device must meet requirements listed under note 1.

3.) Failure criteria for all Press-pack devices: No significant corrosion.

4.) Purpose of this test is the verification of a predicted failure rate according to cosmic ray induced voltage breakdown.

Group C Testing

Group C Testing is performed bi-annually for all generic products. It is essentially specified as a subset of Group D Testing.

4.7 View on Field Reliability Data

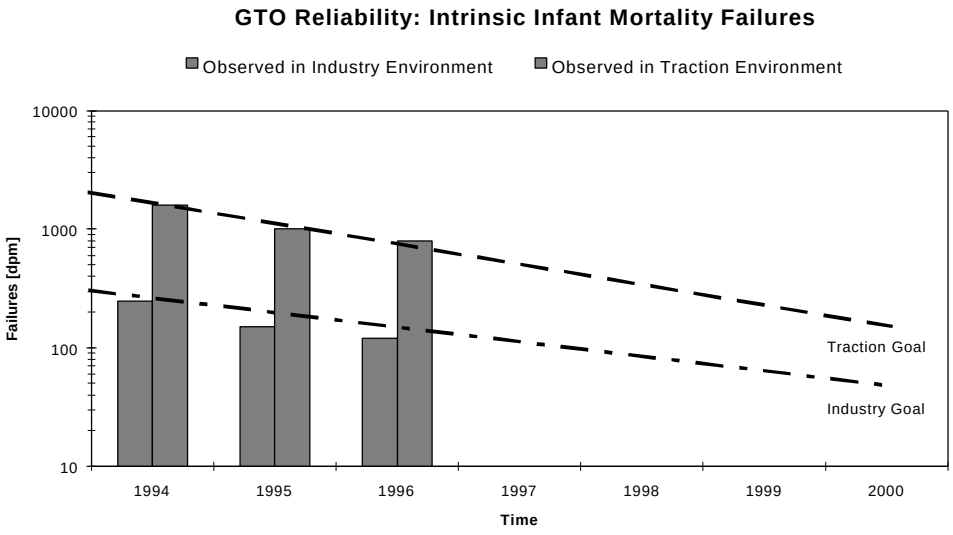
Conforming to the field failure classification scheme outlined under 4.1, at ABB Semiconductors the following reliability data are collected and evaluated continuously:

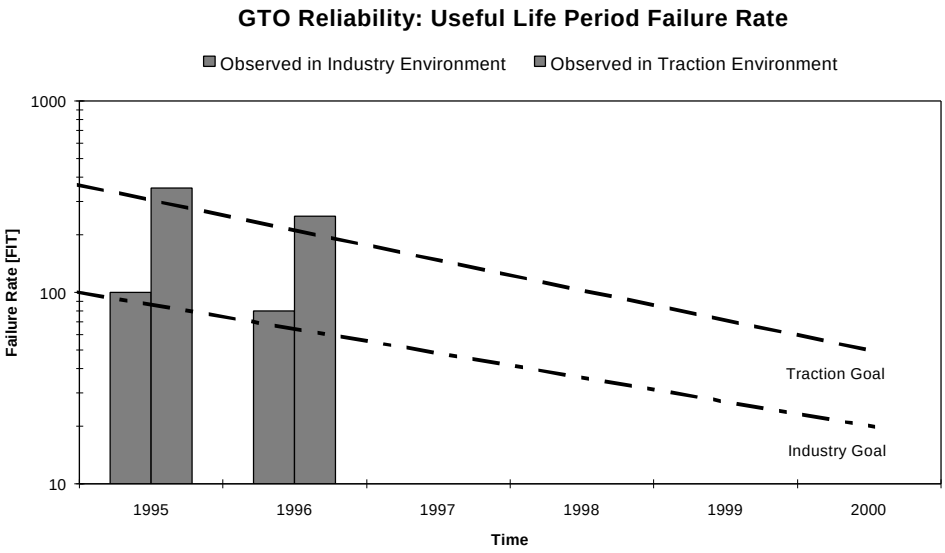
- Infant Mortality Failures (measured in dpm = defectives per million)
- Useful Life Period Failures (measured in FIT)

The examples below are provided for a unique GTO type (identical design, identical manufacturing process), differentiating between two application environments only:

- Industrial Environment = Converters for industrial drives
- Traction Environment = Converters for heavy locomotives.

For each environment, the observation period is more than two years, and the number of components in service at least 20,000. All failures and their circumstances have been analysed carefully, in order to understand root causes. In this joint effort between customers and ABB Semiconductors, the goal is to be able to chart a continuous improvement in relevant reliability results (reliability growth).





4.8 Note on Fatigue-life Predictions

With functional power cycling (see 4.6 Subgroup D7 “Thermal cycling load“), the specific failure mechanism addressed is the plastic deformation of cathode metallization over the GTO fingers. If this deformation exceeds a certain limit, the risk of gate-cathode shorts is significantly increased.

The aim of functional power cycling is to provide data for predictive behaviour of the device in service, and it is therefore necessary either to simulate service conditions as closely as possible, or to understand the relationship between accelerated test conditions and service conditions. Unfortunately, in relatively complex mechanical systems like GTOs with free-floating silicon technology, the accelerated effects arising from raising the temperature, increasing the strain rate or strain range, etc. are multi-parametric and inter-related. As a consequence, the use of accelerated testing, even in a qualitative manner, must be viewed with some caution.

Nevertheless, the user of high power semiconductors wants assistance in being able to judge device life time (i.e. number of cycles to failure), under the load conditions defining his application. The following method has proven to be a useful first approach:

Relating Test Conditions to Service Conditions

First all relevant service conditions must be quantified. A typical load profile for GTOs in traction converters could be:

N° of cycles $N_{Service}$	Temperature excursion $\Delta T_{J;Service}$ [°C]
$4 * 10^6$	40
$3 * 10^5$	55
$2 * 10^4$	75

For an 85 mm junction device, qualification test conditions are $N_{Test} = 10^5$ cycles, with an imposed temperature excursion of $\Delta T_{j;Test} = 80°C$, with a typical cycle time of around 90 s.

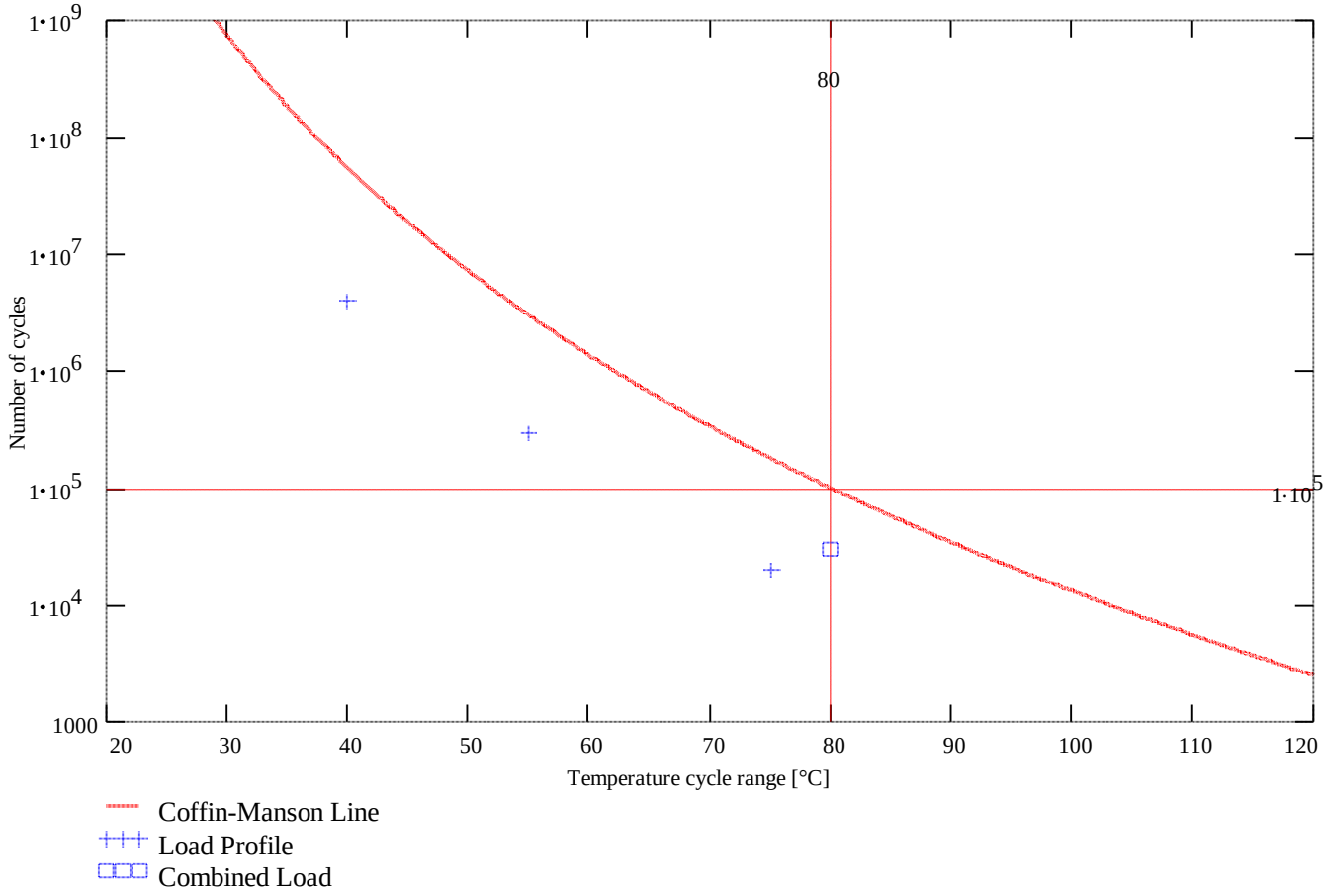
Extrapolation of test-to-service conditions is realised with a Coffin-Manson type of relationship:-

$$N = [C * \Delta T]^{-c}$$

N is the number of cycles to a certain percentage of failures. Parameters C and c have been established experimentally in multiple test set-ups. Values of $C = 3.5 * 10^{-3}$ and $c = 9.1$ mirror the Coffin-Manson curve to the above mentioned qualification point.

The prediction scheme now proceeds as follows: Recalculate C for each individual service condition ($N_{Service}$, $\Delta T_{j;Service}$), then solve the above equation for the equivalent number of cycles at the test condition $\Delta T_{j;Test}$. These results are then summed to yield the total equivalent number of cycles. If this number (the combined load) is significantly less than the number of test cycles, reliability problems due to plastic deformation should not occur.

Converting the load profile example into equivalent cycles at $\Delta T_{j;Test}$ = 80°C yields $2.8 * 10^4$ cycles, which is well on the safe side. The results are illustrated in the following figure:



Load Cycle Test System

4.9 Related Documents and Standards

- IEC Publication 68, Basic environmental testing procedures
- IEC Publication 747-6, Semiconductor devices, Discrete devices and integrated circuits, Part 9: Thyristors
- IEC Publication 749, Semiconductor devices, Mechanical and climatic test methods
- US Military Standard MIL-STD-750C, Test methods for semiconductors devices
- Japanese Industry Standard JIS C 7021
- IEC 300-1 (ISO 9000-4), Dependability management - Part 1: Dependability programme management
- 5SYS 0050-02, General Quality Specification for High Power Semiconductors, ABB Semiconductors AG