Application-Specific Fast-Recovery Diodes: Design and Performance

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Abstract

The number of fast recovery applications in high power systems continues to grow leading to various dynamic constraints and hence different diode designs and behaviours. Along with conventional *RC* ("SCR-type") and *C* ("GTO-type") snubber conditions, *snubberless* conditions in both IGBT and IGCT applications are gaining ground at ever higher currents and voltages (presently 6 kV). Within these two groups, the further distinctions of "inductive" and "resistive" commutation di/dt must be made for an optimal diode design. Diodes capable of high reverse di/dt and dv/dt can today be realised thanks to controlled life-time profiling which will be described here with both measured and simulated results. As will also be explained, such "robust" designs, though essential for snubberless operation, may be "less robust" under snubbered conditions so that a clear understanding of the application *(Snubber, Free-Wheel, Clamp, Resistive or Inductive di/dt)* is required for the correct choice or design of a fast recovery diode. The different diode commutation conditions will be described and categorised and the optimal diode design identified with supporting measurements and simulations.

1. Introduction

In order to judge the behaviour of diodes during turn-off, the circuit conditions needs to be taken into consideration notably with respect to "inductive" and "resistive" switching.
The areas of application of fast diodes will first be described and definitions of the commutation conditions given.

1.1 Inductive Commutation

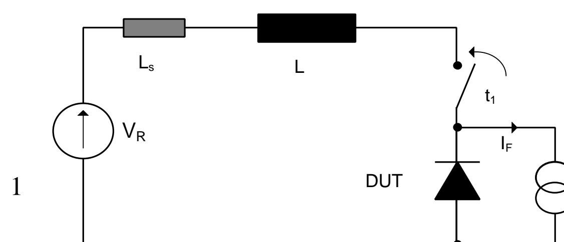


Fig. 1 "Inductive" turn-off circuit

Fig 1 shows the equivalent circuit of a diode undergoing turn-off by turn-on at t_1 of a "perfect switch" (S_1) whose di/dt is determined by the external inductance L.
Traditionally the diode under consideration (in this case a Free-Wheel Diode (FWD)) is fitted with a snubber and may also be fitted with a clamp as shown in Fig. 2.

Thus for the inductive commutation circuit, we can define the additional sub-conditions consisting of permutations of the snubbered/unsnubbered & clamped/unclamped conditions whereby the snubber controls the Duet's dv/dt whereas the clamp controls its peak voltage.

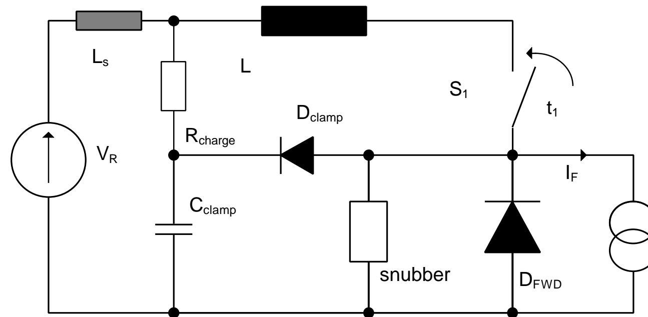


Fig. 2 "Inductive" commutation circuit fitted with snubber and clamp

1.2 Resistive Commutation

In this mode of commutation, the turn-off di/dt is controlled by the active switch which is then "not perfect" in that is does not switch instantaneously but progressively over a (short) period of time. In practice the "switch" may be a transistor operating in the linear mode which allows di/dt control via base or gate.

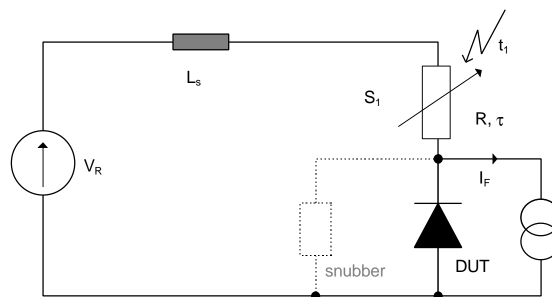


Fig. 3 "Resistive" turn-off circuit

This is illustrated in Fig. 3 in which the active switch S_1 can be considered a time dependent resistance of constant τ and initial value R. If the resultant circuit di/dt is determined by τ rather than L then the circuit is said to impose "resistive" switching and L degenerates to the stray inductance L_s. This kind of circuit is encountered in McMurray or Undeland snubbers where the active switch is typically a GTO, or in FWD circuits where the active switch is an IGBT. Such circuits rarely use additional snubbers or clamps because if the inductance L_s is really negligible, the DUT voltage is ultimately clamped by the source voltage (V_R) and dv/dt is determined by the characteristics of the active switch. An additional snubber across the DUT would be an additional stress (and loss) for S_1.

1.3 Clamp Diodes

In Fig. 2, a clamp diode D_{clamp} is used to limit the peak voltage to a pre-determined maximum (in this case V_R obtained via D_{charge}). When the peak FWD voltage is reached this diode is called upon to conduct quickly (low forward recovery time, t_{fr}) and to stop a further increase of voltage. Depending on the value of C_{clamp}, clamp voltage will rise above V_R and D_{clamp} will block under a small voltage $\Delta V = V_R - V_{clamp}$. However, clamp diodes are not used only to clamp FWDs but also to clamp active switches such as IGBTs and IGCTs. Fig 4 shows an IGCT inverter phase-leg with clamp and FWDs in which a far more severe commutation mode may appear for D_{clamp}.
In the clamp circuit of Fig. 4, D_{clamp} limits voltage from the recovery of D_{FWD2} (S_1 conducting) and recovery of D_{FWD1} (S_2 conducting). Conversely, it clamps the turn-off of S_1 (D_{FWD2} conducting) and of S_2 (D_{FWD1} conducting). D_{clamp} also acts as a FWD for the di/dt snubber L but should S_1 or S_2 (complementary diodes conducting) be fired while D_{clamp} is still in conduction, the turn-off circuit of

D_{clamp} degenerates to that of Fig. 3 where only clamp stray inductance L_{s_clamp} and the turn-on speed of S_1/S_2 determine the diode's recovery di/dt. Thus the constraints of clamp diodes tend to be the same as those of snubber diodes.

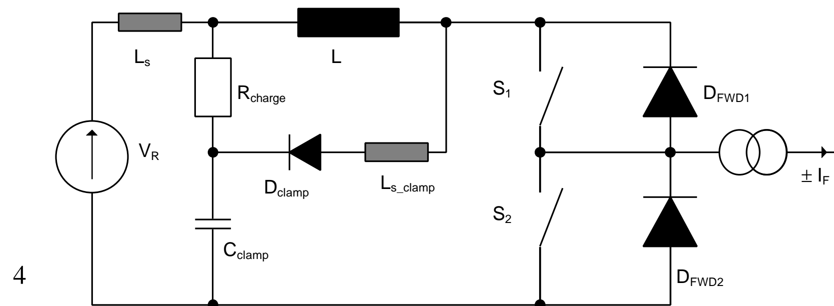


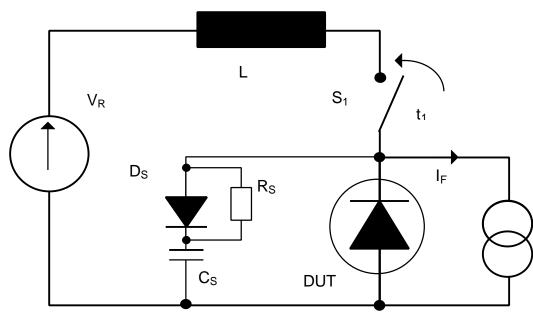
Fig. 4 Universal Clamp Circuit [1]

1.4 Snubbers and Commutation Modes

Snubber circuits are commonly used on main switches and FWDs (less so on clamp and snubber diodes) to reduce turn-off/recovery losses and/or enhance Safe Operating Area (SOA). They do so essentially by controlling reapplied dv/dt which in turn strongly affects the recovery behaviour of diodes as will be shown later. The types of possible *snubbers* which will be described here, in combination with the types of *applications* seen above, determine both diode technology and design to be adopted.
The various snubbers and commutation types are summarised in Fig 5 below. The main configurations of Fig. 5 will be discussed later with reference to measurements and simulations since the former represent most of the dynamic diode constraints found in high power applications. It will be seen that no single diode technology covers all the possible applications but firstly the available technologies and their impact on performance will be reviewed to allow a better understanding of the measured and simulated results.

2. Diode Design & Technology

In order to reduce conduction losses at a given blocking capability the thickness of the diode's low doped region (distance between anode and cathode emitters) must be minimised and the resistivity of the base material must be increased [2]. Thus the shape of the space charge region in the static blocking state changes from triangular to trapezoidal and „punch through" of the space charge region occurs at comparably low voltages. A depletion of the device at voltages lower than the maximum voltage (V_{RRM}) during turn off usually results in snap-off of the diode's recovery current and consequent oscillations in the circuit due to parasitic inductances. This is generally overcome by the use of snubbers but the trend in power electronics is towards the snubberless operation of active switches (IGBTs, IGCTs) and snubberless operation of the diode is equally demanded. Under turn-off at high di/dt this is complicated by the formation of a second space charge region at the cathode side, which leads to a virtual reduction of the usable low doped region [2].



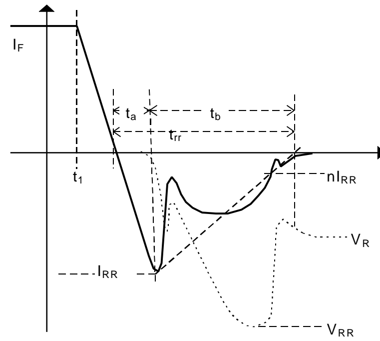
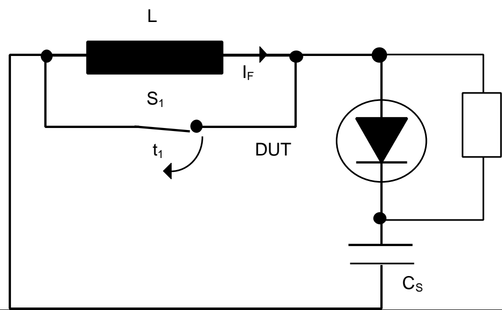


Fig. 5a) RCD-snubber for FWD, inductive switching



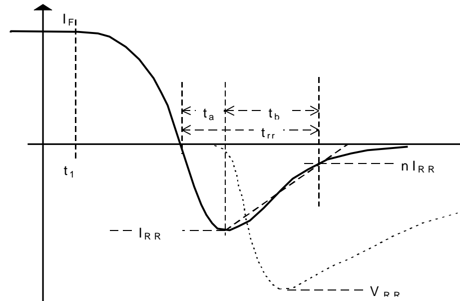
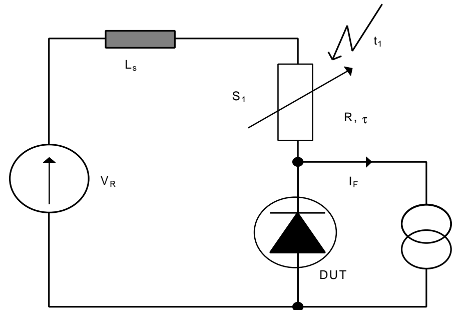


Fig. 5b) R-snubber for RCD, snubber-diode, inductive switching



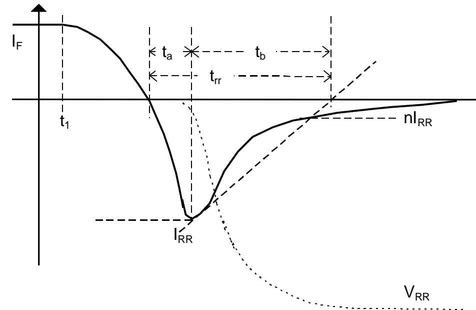
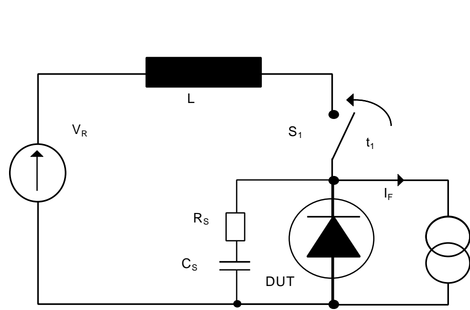


Fig. 5c) Snubberless Undeland/ McMurray snubber-diode, resistive switching



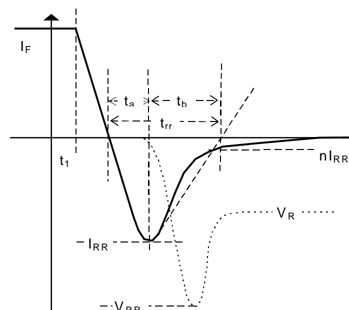
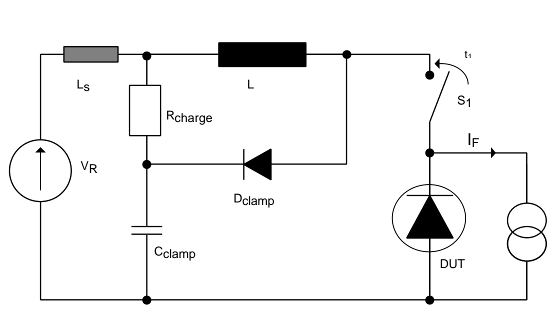


Fig. 5d) RC-snubber, inductive switching



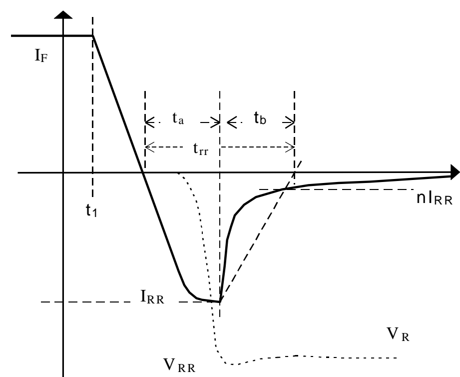


Fig. 5e) Snubberless, clamped inductive switching

Choosing the low doped region wide enough to avoid punch through at $V_{RR} = V_{RRM}$ is not sufficient. The formation of this second space charge region can be effectively suppressed by appropriate tailoring of the carrier distribution during conduction.
In order to obtain a beneficial spatial carrier distribution and to optimise the dynamic diode behaviour for both high di/dt and high dv/dt applications, various approaches have been taken but, it will be shown later that different solutions are required for the different circuits outlined above and in Fig. 5.
Shaping the on-state carrier distribution in a diode can be realised using either of the following approaches or a combination of them:

a) adjusting the efficiency of the emitters (anode emitter usually) by their doping profile (*emitter engineering*)
b) adjusting the carrier lifetime in the high and/or low doped region of the device (*lifetime engineering*).

In principal, both approaches are suitable to ensure good device behaviour but manufacturing process requirements are very different.

2.1. Emitter Engineering

Various concepts have been suggested and investigated in the past. The main idea is to reduce the amount of carriers injected on the anode side in the conduction state by reducing the anode emitter efficiency.
The transparent anode emitter [3] technology is well known from its applications to IGBTs, GTOs and GCTs. It can also be used on diodes to obtain a low carrier concentration on the anode side.
This goal is achieved when a large amount of electrons can move through the p-doped surface emitter layer and reach the metal contact without undergoing recombination.
Low recombination results when the thickness of the p-emitter is of the order of the electron diffusion length. For the typical, highly doped emitters in power devices, electron diffusion lengths are very short, the recombination in the emitter is high and their injection efficiency is correspondingly high.
Transparent emitters with long electron diffusion lengths are characterised by extremely thin p-doped layers and low surface concentrations. Both, surface concentration and thickness impose technological limitations on the lowest achievable emitter injection efficiency.
Therefore the thickness of the anode border layer is kept in the order of the electron diffusion length. Thus the anode emitter efficiency is reduced.
Since emitter efficiency can only be reduced within limits, lifetime doping becomes indispensable [4].
In the self-adjusting p-emitter efficiency diode (SPEED) [5, 6] the desired carrier distribution is obtained by laterally interrupting the high-doped p-emitter zone. Thus the neighbouring low doped p-zone acts as a week emitter during conducting, while the highly doped regions enable good surge current capability. This structure is obtained by masked implantation, requiring photolithography and subsequent diffusion. A similar design has been realised by a Static Shielding Diode [6] but also in these cases additional lifetime doping is required.
Still more exotic approaches are possible such as the merged PiN-Schottky diode [6] which has been suggested in order to combine the advantageous features of PiN and Schottky diodes, namely low on-state drop due to conductivity modulation of the drift region and a faster turn-off normally associated with Schottky rectifiers.
The hybrid diode concept combines snappy (thin) and soft (thick) diodes monolithically on one wafer, thus obtaining low on state voltage drop and soft recovery behaviour [7]. These concepts require significant technological efforts. In contrast to the concepts briefly described above where only the anode structure has been considered, there are also concepts which are based on or are supported by modified cathode emitter structures. A cathode buffer-layer, which acts as a charge reservoir at the end of the diode’s recovery phase when the S-C-R approaches the cathode, is frequently used to support soft recovery.

An interesting concept has been suggested by [8], whereby cathode (and anode) shorts are introduced, thus clamping the diode over-voltage by a controlled „punch through“. However this concept is valid only for an extremely narrow operating range and requires very well controlled diffusion processes.
A MOS controlled diode adds a third electrode to the device thus providing the possibility of controlling diode behaviour [9]. The MOS controlled diode uses the concept of controlling the injection of minority carriers by adding an extra MOSFET in parallel or in series with the main PN-junction. A number of possible combinations exist with or without trench. Unfortunately this technology requires very costly processing.

2.2. Lifetime Engineering

Lifetime control is based on the introduction of recombination centres by electron or particle irradiation or by heavy metal diffusion.
Introduction of heavy metals (platinum or gold) requires diffusion at elevated temperatures (above 700°C) before completion of the device fabrication. These metals are fast diffusants making it difficult to control the final defect distribution and cross-contamination in the production line is a constant risk. Due to gettering effects by phosphorous, a lifetime gradient within the device from the anode to the cathode results which can be more pronounced by employing modern techniques such as Implantation, RTA (rapid thermal anneal) or low temperature diffusion [10, 11, 12].
Electron irradiation requires an electron accelerator (energy typically in the range of 2 - 10 MeV). The process is easy to control, clean and is employed at the “back-end” of the production process, providing very reproducible results. It also can be used for fine tuning device characteristics in back end processing or even after testing. It may also be used in combination with any of the techniques mentioned above. A subsequent anneal is required for thermal stabilisation of the defects. The recombination centres resulting from electron irradiation are uniformly distributed within the whole device volume.
Ion-irradiation (protons or helium) is also a so-called “off-line“ process requiring a high energy (MeV range) accelerator. The nature of the defects created during ion-irradiation is similar to that of those created by electron-irradiation. A subsequent thermal treatment for defect stabilisation is also required.
Ion-beam irradiation allows localisation of lifetime control to a very narrow depth zone in the device structure because high-energy ions deposit energy most efficiently near the end of their penetration range. The depth of this zone (defect peak) is defined by the ion energy.
Repetitive application of more energies and doses or variation of the ion energy during irradiation may be used to shape the defect profile. Ion-beam irradiation in combination with electron beam irradiation [14, 15] or heavy metal diffusion [13] may be used for further device optimisation. Ion-irradiation is accepted as a reliable tool and commercial ion sources are available.

ABB Semiconductors favours local lifetime control by ion beam irradiation on fast diodes and GCTs, because of its good reproducibility and its versatility. Together with the Technical University of Prague and with the help of Silvaco, the possibility of precise simulation of ion-irradiated devices has been introduced allowing the reduction of development costs and cycle times in the tailoring of devices for new applications. These will be discussed in the following.

2.3 Static and Dynamic Carrier Distribution

The dynamic behaviour of diodes is determined by the carrier distribution in the device, *just prior to commutation* [4]. In the following it will be briefly shown that local lifetime control provides a powerful tool for influencing the dynamic carrier distribution during turn-off. In contrast to *emitter-efficiency controlled* diodes, where the control over the carrier distribution is lost at an early stage of the recovery phase as soon as injection is stopped, the *carrier lifetime technique* provides control of

the plasma distribution as long as the treated area is flooded with carriers. Fig. 6 shows the open-circuit carrier decay of differently treated devices. Fig 6a depicts the carrier distributions of a proton-doped diode while Fig. 6b shows that of a uniformly doped transparent emitter device.

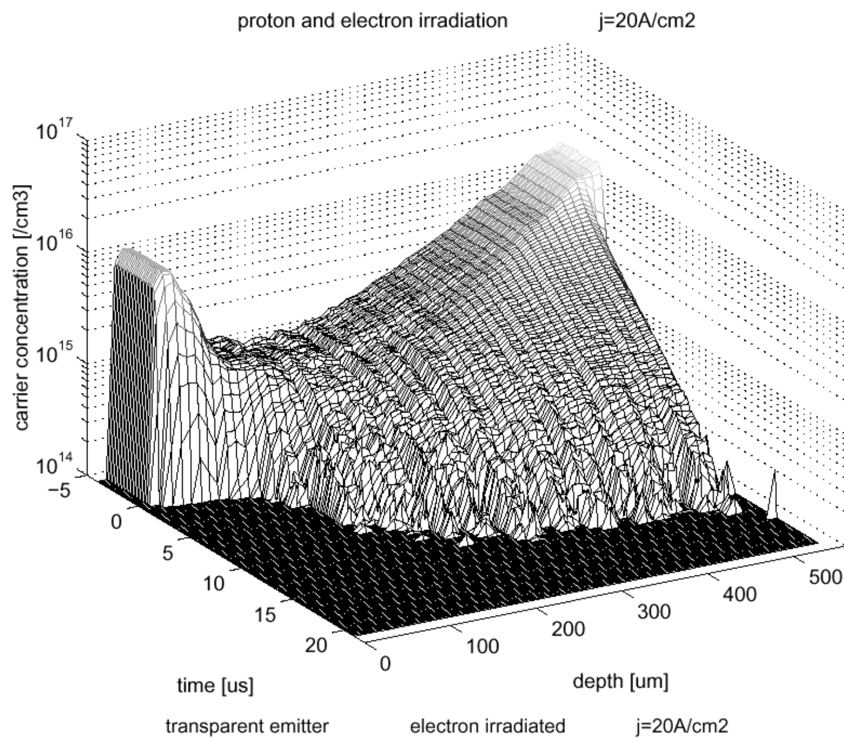


Fig. 6a
Carrier distribution of profiled lifetime diode.

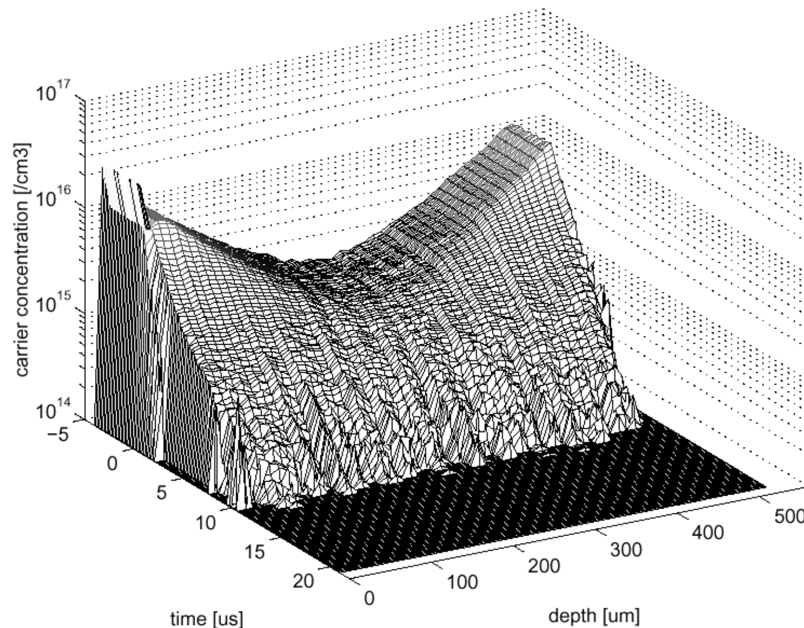


Fig. 6b
Carrier distributions of uniform life-time diode

Fig. 6 Open circuit carrier decay of differently irradiated devices measured by Free Carrier Absorption (FCA)

Fig. 7 shows that the depletion velocity at low voltage is much faster (Fig. 7a, Points 2 & 3) in the proton irradiated device than in the transparent emitter diode which results in a reduced $I_{RR.}$ However at high voltage, towards the end of the recovery phase (Fig. 7a, Points 5 and above), the space charge region moves more slowly in the irradiated-diode than in the emitter efficiency controlled-diode resulting in a softer recovery. Despite the same carrier distribution during conduction (Fig. 7a, Point 1) the device behaviour during turn-off is different.

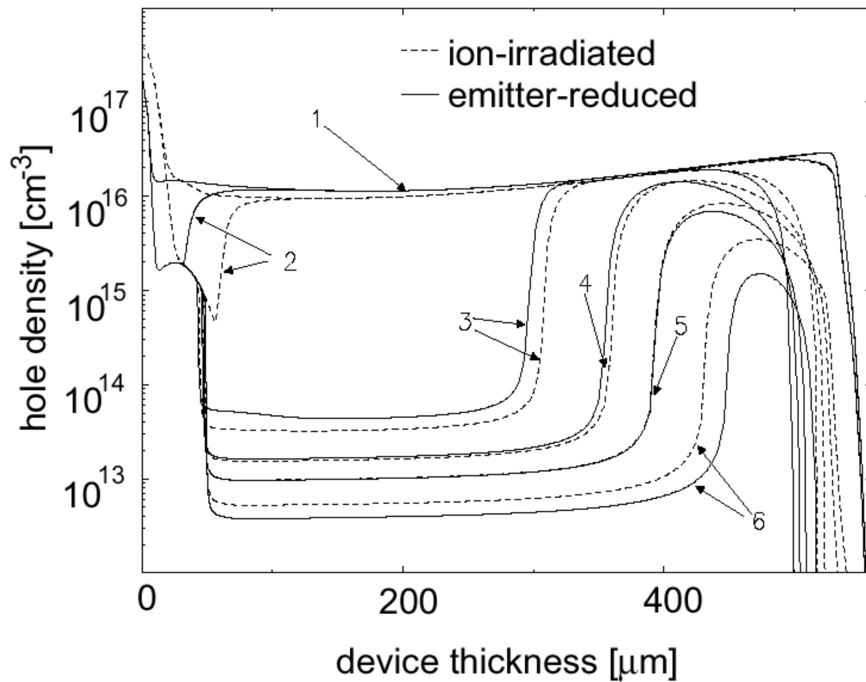


Fig. 7a
Simulated hole density distribution during reverse recovery

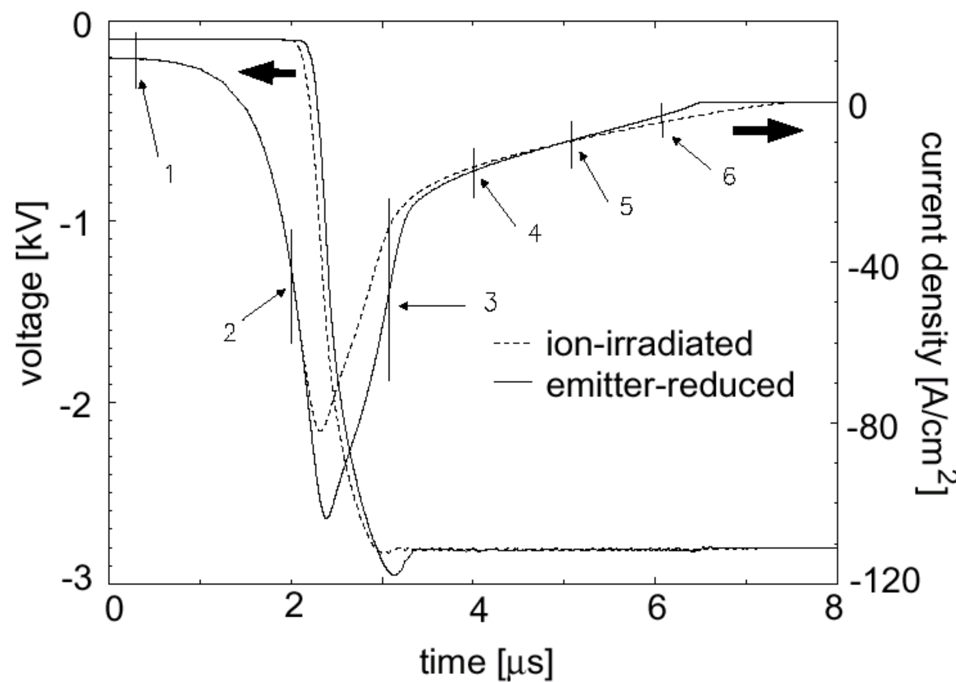


Fig. 7b
Simulated recovery waveforms

Figs. 7a and 7b compare uniform life-time (reduced anode efficiency) and profiled life-time diodes (proton-irradiated) at different instants in the recovery phase, normalised to 10 A/cm^2, T_j = 110 °C, on-states set to 1.5 V at 10 A/cm^2 and 0.9 V at 10 A/cm^2 for both types. The dotted lines represent the non-uniform lifetime diode and the solid lines the uniform lifetime device.
Table 1. shows the comparison of some key parameters of diodes produced with different technologies. The low dynamic voltage overshoot and low leakage current of the combined proton-electron irradiated device diode in comparison with a gold doped device are striking.

Table 1

Lifetime	On-state	Blocking	Turn-off @ di/dt = 100 A/µs, V_{dc} = 1000 V, I_F = 1000 A			Turn-on @ 1000 A/µs	
Technology	V_F @ 3000A, 125°C	leakage current @ 4.5 kV, 125 °C	I_{rr}	Q_{rr}	s-factor	V_{fr} @ 25°C	V_{fr} @ 125°C
gold (1)	6.5 V	24 mA	185 A	615 mC	1.2	90 V	145 V
electrons (2)	6.8 V	6 mA	235 A	585 mC	0.7	55 V	120 V
protons (1)	6.5 V	11 mA	175 A	620 mC	1.4	52 V	115 V
(1) - non-uniform life-time diode, (2) - uniform life-time diode							

3. Measurements and Simulations

Simulations and measurements were based on the configurations of Fig. 5 or more generally on that of Fig. 2. The current source I_F is used to set the on-state current. Inductance L may be varied to determine the switching conditions from resistive to inductive. Switch S_1 (either GTO or IGBT) is represented by time-dependent resistor R of constant τ but was in fact a GTO with adjustable gate drive in the measurements. The DUT is conducting while R is high and reverse recovery of the device is initiated by its exponential decrease. The commutating voltage is supplied by the DC voltage source V_R. A di/dt limiting choke and clamp consisting of D_{clamp}, C_{clamp} and L per Fig 4 is connected as required (inductive switching) and τ is varied to emulate a “perfect” (inductive) switch or an “imperfect” (resistive) switch. A snubber may be added to the DUT. Simulation tools are “ATLAS” from Silvaco.

3.1 Resistive Switching

The following conditions were investigated on a 38 mm, 4.5 kV diode: I_F = 100 A, L_s = 200 nH and V_R = 3000 V. In the simulations, the rate of current change is adjusted by the decay of R (Fig. 5b) in order to obtain a di/dt of 50A/µs/cm^2 at zero crossing, resulting in a maximum di/dt of about 200A/µs/cm^2 prior to reaching I_{RR}. As the di/dt of the diode is determined by the non-linear change of the resistance R, the commutation di/dt of the diode is also non-linear (Fig. 5b).
Due to the small value of L_s, the dynamic voltage overshoot is low (V_{DUT} is quasi clamped to V_R). The major problem encountered in such applications is “snap-off” of the reverse current near the end of the recovery phase. Fig. 8 illustrates this with the recovery waveforms of the irradiated diodes of Table 1. It can clearly be seen that this snap-off may be avoided by profiling the carrier recombination centres with proton irradiation.
Fig. 9 compares measured and simulated results. Calibration of the Silvaco device simulator was performed using unirradiated, electron-irradiated, single-energy proton-irradiated and electron-plus-proton irradiated devices.

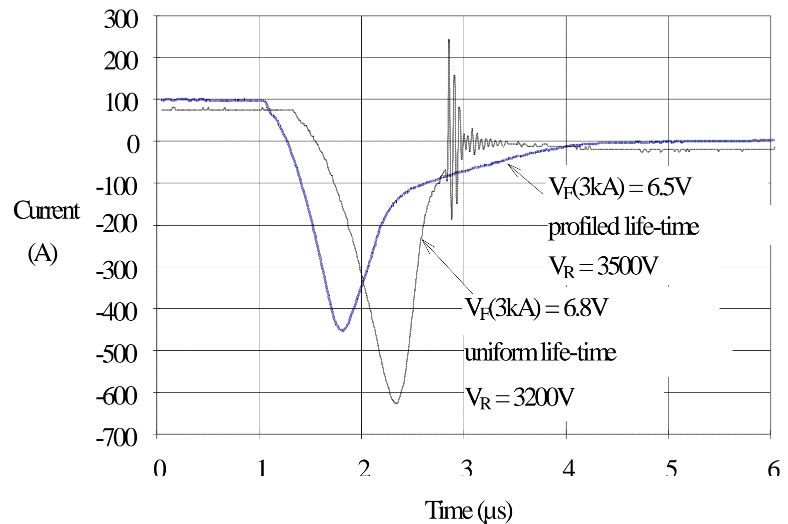


Fig. 8
Comparison of uniform and profiled lifetime control. 38 mm, 4.5 kV diode at 110°C

Fig. 9b shows the simulated waveforms of electron and combined proton and electron irradiated structures. Although the simulation shows snap-off and subsequent oscillations in both cases, this behaviour in reality only occurs on the electron irradiated device. The simulation nevertheless reveals much softer recovery of the proton-irradiated device compared to the electron-irradiated device as confirmed by measurement (Fig. 9a). The oscillations in the case of the simulated proton-irradiated diode are damped by parasitic losses and do not appear in reality.

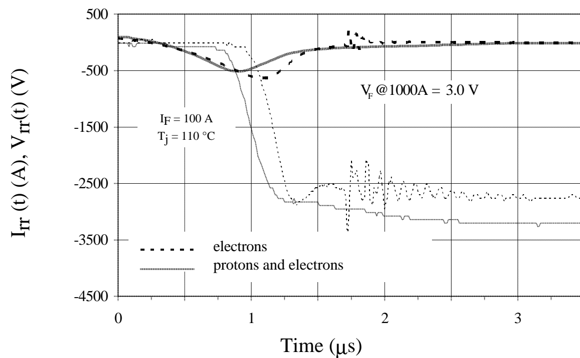


Fig. 9a Measured

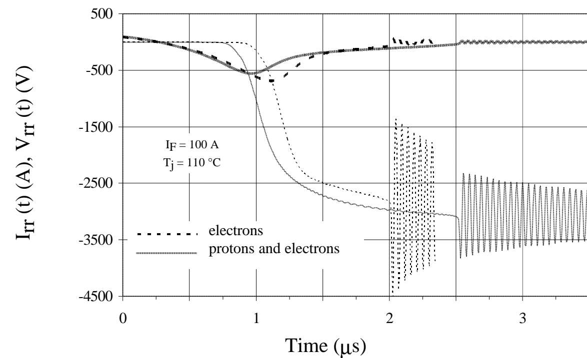


Fig. 9b Simulated

Fig. 9 Measured and simulated recovery of 38 mm, 4.5 kV diode under resistive switching, T_j = 110 °C

Snap-off is most likely to occur at low forward current densities (1 A/cm^2 ...3 A/cm^2) but may be avoided by further tailoring of the defect distribution. Fig. 10 compares the measured current and voltage waveform of a *single-energy* to a *double-energy* proton and electron-irradiated diode turned off at a current of 1A/cm^2 and at a voltage of 3.5 kV (nominal DC-voltage = 2.8 kV). This shows that replacing the electron-irradiation by a second proton-irradiation, soft recovery may be further enhanced under even harsher conditions; the second irradiation serving to prevent dynamic avalanche. This illustrates the fine profile tailoring allowed by ion-irradiation.

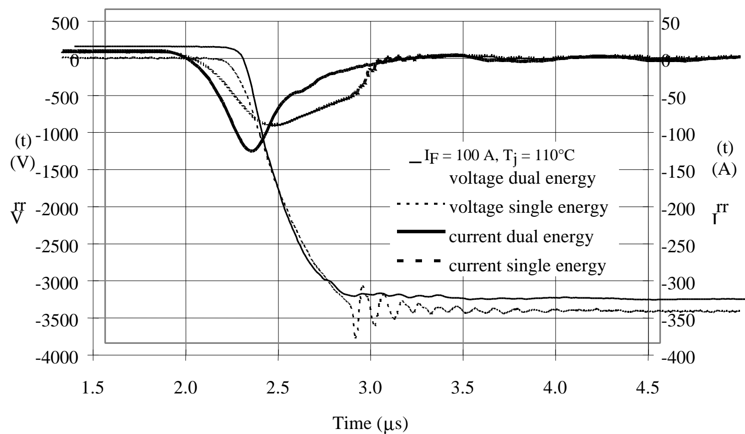


Fig. 10
Measured waveforms of **combined proton and electron irradiated** diodes compared to **double-energy proton irradiated** diodes having the same on-state voltages. (4.5 kV, 38 mm, 110 °C)

3.2 Inductive Switching

In contrast to resistive switching, the commutation di/dt is determined by circuit inductance in the case of inductive switching.

From the viewpoint of the diode, four different inductive conditions can be distinguished:

- RCD-snubbered inductive switching (e.g. GTO-FWDs per Fig. 5a)
- R-snubbered snubber diodes (RCD-snubbers on GTO FWDs in VSIs per Fig. 5c)
- RC-snubbered inductive switching (e.g. GCT commutation diodes in CSIs per Fig. 5d)
- snubberless inductive switching with clamped inductance (e.g. GCT-FWDs in VSIs per Fig. 5e)

(NB: The condition of 5c is not treated here.)

3.2.1 Snubberless-Clamped Switching

This type of operation is of growing importance in Voltage Source Inverters (VSI) where snubberless IGCTs demand equally unsnubbered FWDs and Neutral Point Clamping (NPC) diodes (multi-level inverters).
The test and simulation circuit is shown in Fig. 5e for a 38 mm, 6 kV proton-irradiated diode. For both simulation and measurement the conditions are: $I_F = 250$ A, L = 16.8 µH and $V_R = 3500$ V, di/dt = 200 A/µs.
The measured and simulated waveforms are shown in Fig. 11. The peak power dissipated by the diode during turn off may be approximated by multiplying peak reverse recovery current with clamp voltage: $V_R * I_{RR} \approx 0.9$ MW for about 7.2 cm^2 of active silicon area.
The voltage across the diode increases to its maximal value while the full reverse current flows. Diode current I_{RR} from current source L cannot decline until $V_{cl} = V_R$ is reached. Once the clamp starts, recovery current declines whilst diode voltage remains constant.
To optimise diode recovery, I_{RR} must be minimised and snap-off avoided. Both can be achieved by either maintaining a wide neutral region at V_R or preferably by appropriate life-time tailoring as this results in lower conduction losses. Figure 11 shows that the chosen lifetime profile achieves this while allowing an SOA of 125 kW/cm^2. (The max. SOA for this device was found to be greater than 250 kW/cm^2.)
Again the simulation shows pessimistic snap response resulting in a small oscillation not present in reality.

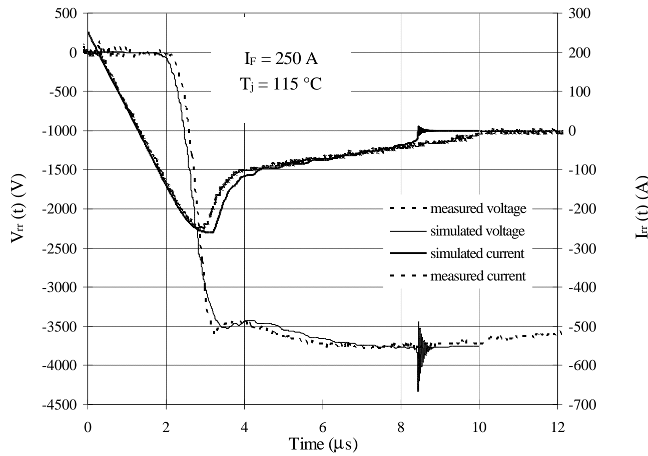


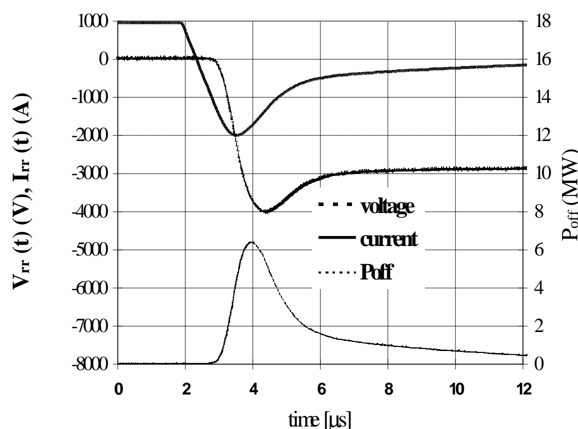
Fig. 11
Measured and simulated recovery of snubberless clamped inductive switching of 6 kV diode (38 mm)

3.2.2 Snubbered Inductive Switching

In general, inductive switching requires either a clamp or a snubber to absorb some of the energy stored in the discrete inductance L. RCD snubbers (undamped) generate low dv/dts high peak voltages (Fig. 5a) whereas RC snubbers (damped) generate high dv/dts and lower peaks. As indicated earlier, the dv/dt value dictates the kind of lifetime profiling required.

3.2.2.1 RC Snubber

This type of snubber might be used in series-connected VSIs where snubberless operation is complicated by gate unit jitter (both at turn-on and turn-off) or in CSIs where no free-wheel path is available at active-switch turn-off (no conduction overlap) but where cumbersome RCD snubbers are to be avoided.
Fig 12 compares the recoveries of 91 mm, 6 kV proton and electron irradiated diodes undergoing commutation at 2200 A/µs at V_R = 3000 V, I_F = 1000 A, R = 9 Ω, C = 0.5 µF. The electron-irradiated diode fails under this condition.



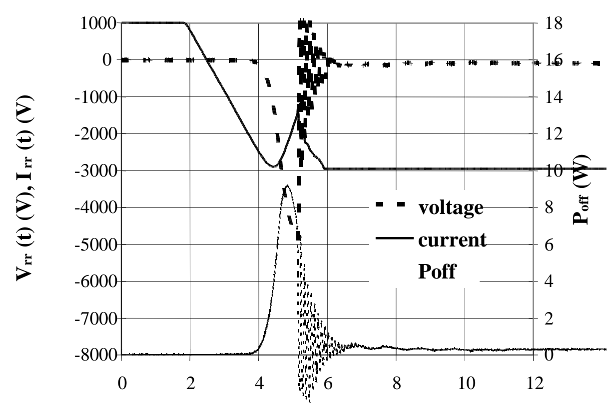


Fig. 12a Proton-irradiated diode T_j = 125 °C

Fig. 12b Electron-irradiated diode T_j = 125 °C

Fig. 12 Comparison of RC-snubbered turn-off of 91 mm, 6 kV proton-irradiated and electron irradiated diodes

3.2.2.2 RCD Snubber

This type of snubber reduces dv/dt to very low values and is commonly used with GTOs or GCTs in low frequency or very high current applications. Fig. 13 compares proton and electron-irradiated devices under such conditions.
It can be seen from Fig. 13a that the proton-irradiated device produces a much lower I_{RR} than its electron-irradiated counterpart and due to the low dv/dt, very little power is initially dissipated. As the voltage rises however, the proton-irradiated device produces a large “rucksack” which coupled with the higher voltage results in a high power dissipation over a long period. The peak power dissipated by the proton device is twice that of the electron device and its energy loss is nearly three times greater. Clearly the electron-irradiated device is the better choice for this type of application even though both devices are “soft” in this test and recovery current is lower for the proton device.

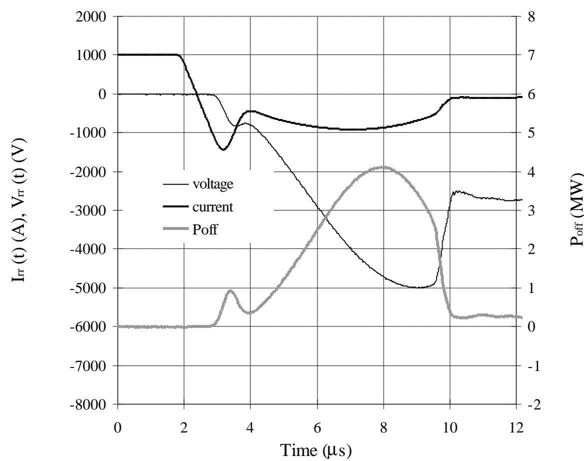


Fig. 13a Proton-irradiated diode, $T_j = 125$ °C

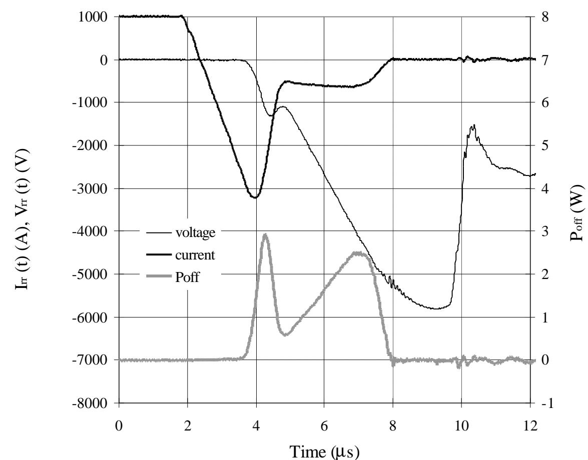


Fig. 13b Electron-irradiated diode, $T_j = 125$ °C

Fig. 13 Comparison of RCD -snubbered turn-off of 91 mm, 6 kV proton-irradiated and electron irradiated diodes

4 Production Testing

These new devices for snubberless and quasi-snubberless operation are now designed to operate at much higher SOAs than was previously deemed possible. For this, a new Production Test philosophy is required more akin to the testing of GTOs and IGBTs than that of diodes and SCRs. The former have always been 100% tested for their turn-off capabilities (ratings) along with their turn-off losses (characteristics) whereas the latter were normally tested for characteristics only and selected into groups of Q_{rr}, t_{rr} etc. A new generation of diode testers has been developed [16] to allow the five test conditions of Fig. 5 to be met up to 6 kV, 6 kA and 2 kA/µs with and without clamps and snubbers. This testing ensures that diodes for all functions undergo the full stress of the final application so that both snap and SOA can be guaranteed along with the usual characteristics. This equipment also allows rapid feedback of test results under diverse and stressful conditions allowing accurate calibration of the simulation tools.

5 Conclusions

A new generation of high power diodes is now becoming available to complement recent advances in snubberless switches. Three powerful tools have been combined to achieve soft-recovery, high SOA and optimal application-oriented designs: combined electron and proton lifetime profiling, Silvaco simulation and application-oriented Production Testing. Much of the laborious experimentation has been eliminated from power diode design allowing the concurrent engineering of both devices *and* equipment thus permitting new generations of equipment to be designed with drastically reduced components count with consequently enhanced reliability and reduced cost. As predicted with the introduction of the IGCT at PCIM ‘96, the fast diode - traditionally the “weak-link” in power electronics is rapidly approaching the SOA capabilities of GCTs.

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