A Landmark in Electrical Performance of IGBT Modules Utilizing Next Generation Chip Technologies

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***Abstract*-The aim of this work is to demonstrate that future high power IGBT modules will be capable of providing electrical performance not matched to date in terms of low losses, soft turn-off characteristics, square RBSOA, and full over-current and over-voltage self-protection mechanisms under fault conditions. First ever prototype modules were fabricated incorporating heavily paralleled 3300V chips employing the next generation *Enhanced-Planar* IGBT (EP-IGBT) technology and the *Field Charge Extraction* Diode (FCE) concept. In this paper, we show that the two technologies will provide the module with outstanding characteristics, therefore promising higher levels of performance in tomorrow's applications. In addition, we present a set of results where two 3300V IGBT modules were tested in parallel under extreme RBSOA conditions with a forced temperature difference of up to 100 °C. The modules were capable of turning off 6000A at a DC-link voltage of 2600V in spite of the temperature induced current mismatch and associated redistribution mechanisms.**

Introduction

The power electronics community upholds a long wish list of improvements targeted at the power semiconductor device electrical performance. Despite the fact that the IGBT offers the user a wide range of attractive electrical characteristics, a number of drawbacks still exist and superior characteristics are continuously required. Lower losses, higher SOA, softer reverse recovery behavior and a chip inherent overshoot voltage protection normally appear on top of the wish list. Recent developments have resulted in the introduction of novel concepts, enabling both the IGBT and the diode to take a step towards the desired higher level of performance.

The introduction of SPT-buffers, weak anode concepts, and new planar cell designs allowed lower losses, while still maintaining soft turn-off, high RBSOA and SCSOA especially for high voltage IGBTs. Extreme ruggedness also enabled Switching-Self-Clamping-Mode (SSCM) resulting in a square SOA and an over-voltage protection mechanism for eliminating clamps and snubbers [1]. Therefore, the next milestone was to reduce the total losses of the IGBT without sacrificing the above mentioned performance advantages. This was recently achieved for the 3300V IGBT employing a new *Enhanced-Planar (EP)* cell design. The new technology provides more than 25% reduction in on-state voltage drop for the same turn-off losses, hence resulting in a new technology benchmark for this voltage class. In diode design, the *Field Charge Extraction (FCE)* concept was demonstrated at chip level last year [2]. This new technology confirmed that soft recovery performance under all conditions combined with low losses, high ruggedness and SSCM capability could be achieved while having no drawbacks on other electrical parameters. In this paper, we will present a high power module, which combines these two technologies employing 24 parallel IGBTs and 12 anti-parallel diodes. The prototype 1500A/3300V modules were subjected to a series of static and dynamic tests to demonstrate their electrical capability.

In the second part of this paper we will present a set of results treating parallel operation of 3300V modules tested under extreme RBSOA conditions with a forced temperature induced current mismatch. Parallel operation of IGBTs remains an important topic, due to the inherent nature of MOS controlled devices to operate in parallel in order to achieve the required average current as demanded by power electronic applications. The circuit layout and spread of device parameters will always result in an imbalance in current sharing between the devices under static and dynamic conditions. Therefore, the device and circuit designer has to deal with a number of issues depending on the application to make the system reliable. The effect of the circuit and device parameters on the dynamic performance has been thoroughly investigated in the past [6]. The negative effects of the gate drive design, stray inductances, temperature variations and the spread of device parameters have been shown to be the main cause of unbalanced current sharing in paralleled IGBT modules. The benchmark module results presented will provide a new outlook for high voltage system designers aiming for an all-around performance improvement in future applications.

Modules with EP-IGBTs and FCE-diodes

A. IGBT and Diode Chip Technologies

In fig. 1, cross-sections of the EP-IGBT and the FCE-diode can be seen. The new IGBT cell-design exploits an N-enhancement layer, which improves the carrier concentration on the cathode side of the IGBT, thus lowering the on-state losses without significantly increasing the turn-off losses [3], [4]. Further details on the enhanced planar cell can be found in [5].

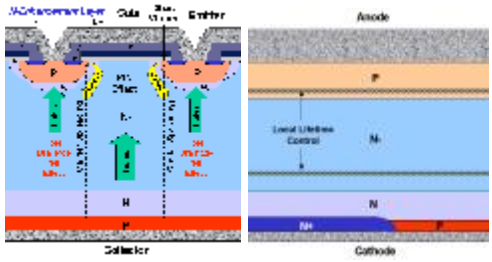

Figure 1: Cross-sections of the Enhanced-Planar (EP) IGBT (left) and Field Charge Extraction (FCE) diode (right).

The FCE-diode consists of a continuous, highly doped P+ emitter on the anode side and the FCE-structure at the cathode side. The emitter efficiency of the anode as well as the excess carrier concentration at the cathode-side of the N-base were adjusted

by local lifetime killing using a double He++ irradiation. The FCE-structure on the cathode side consists of an SPT-buffer and a combination of P+ and N+ contact areas on the semiconductor surface. The P+ and N+ areas are electrically connected (shorted) to each other by the cathode metallization. Electrically, the N+ areas thereby function as the cathode emitter of the PiN diode, whereas the P+ areas act as the emitter of a PNP bipolar transistor. The built in bipolar transistor is mainly active in the end of the reverse recovery phase, supplying an additional hole-current, which prevents a snap-off in this critical stage. The FCE-cathode further enables the diode to reach stable SSCM and in this way increases the recovery ruggedness.

B. Electrical Results under Nominal Conditions

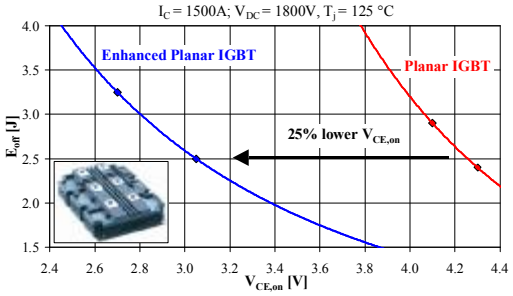

Figure 2: IGBT trade-off curve comparing the standard with the enhanced planar IGBT. The insert shows the tested module type, which contains 24 parallel IGBTs and 12 anti-parallel diodes

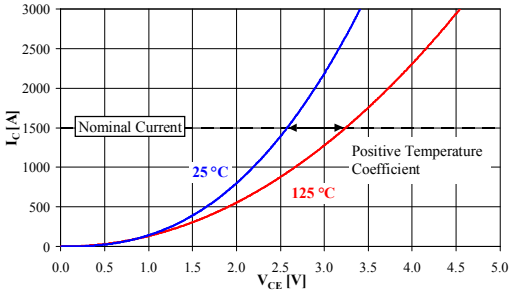

Figure 3: EP-IGBT on-state characteristics.

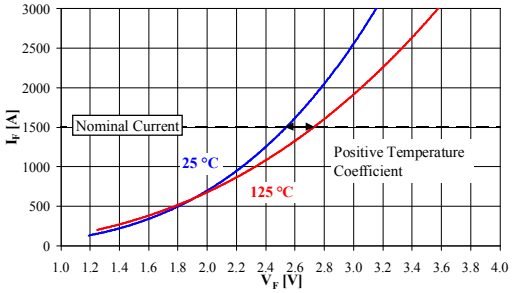

Figure 4: FCE-diode on-state characteristics.

In fig. 2, a comparison between the technology curve of the new EP-IGBT module and a standard IGBT module can be seen. The on-state characteristics for the IGBT and FCE-diode are shown in figure 3 and 4 respectively. At the rated current of 1500A, the EP-IGBT has a benchmark on-state voltage drop of 3.05V at 125 °C, while the diode exhibits a V_F of 2.80V at the same temperature. Both devices show a strong positive temperature coefficient already well below the rated current, which is essential to ensure a good current sharing in such heavy paralleling conditions.

In figure 5 and 6 the turn-on and turn-off waveforms under nominal conditions can be seen. Both the IGBT and the diode exhibit soft and controllable switching performance as well as short current tails, which are reflected in low module switching losses.

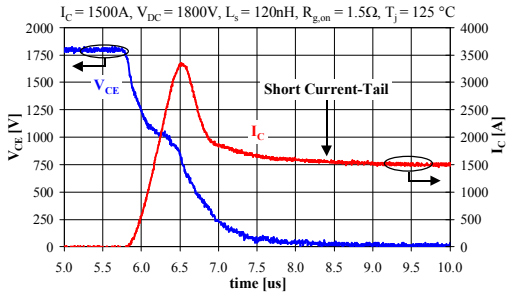

Figure 5: EP-IGBT turn-on under nominal conditions.

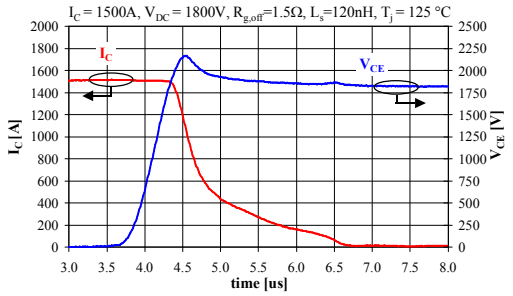

Figure 6: EP-IGBT turn-off under nominal conditions.

C. Ruggedness and Softness when operated under Extreme Conditions

One of the main objectives of this work was to fabricate a module where both the IGBT and the diode exhibit a built-in over-voltage clamping capability (SSCM). To demonstrate this capability, a series of RBSOA tests under extreme conditions (high DC-link voltage and stray-inductance) for both the IGBT and the diode were carried out. As can be seen in figure 7 and 8, both devices show very high dynamic avalanche robustness as well as the desired SSCM capability. This demonstrates that a chip-inherent over-voltage protection can be realized for both the IGBT and the diode even under heavy paralleling as in the measured high-current module. The diode results clearly show that a stable SSCM can be achieved by an additional injection of holes, which prevent a field distortion and associated negative differential resistance in the transition from dynamic avalanche to SSCM.

As a next step, diode softness measurements under worst-case conditions were carried out. In fig. 9, a softness comparison between an FCE- and a standard module measured at T_j=125 °C can be seen. The FCE-module clearly shows a softer, more damped and less oscillatory behavior as compared to the standard one. When the same test was repeated at T_j=25 °C, the standard diode failed due to an over-voltage peak

caused by its snappy recovery, whereas the FCE-diode managed to recover safely showing similar soft behavior as at 125 °C.

Finally, the high short-circuit capability of the new module was demonstrated at 125 °C against a DC-link voltage of 2500V as shown in figure 10.

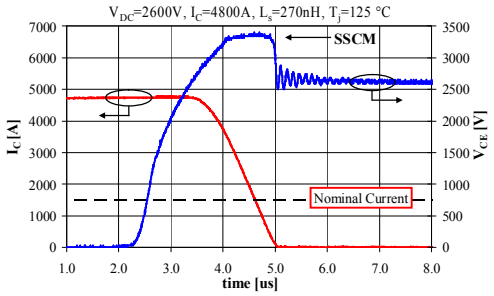

Figure 7: EP-IGBT SSCM (Switching-Self-Clamping-Mode).

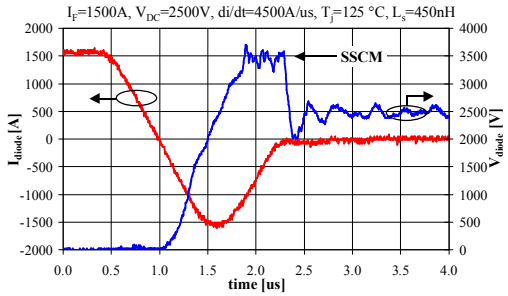

Figure 8: FCE-diode SSCM.

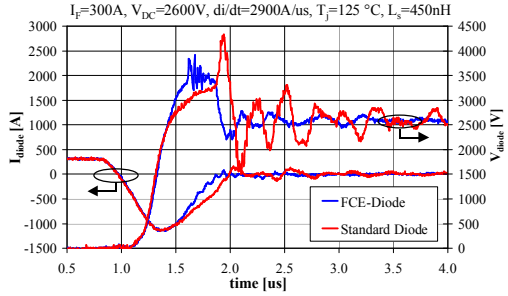

Figure 9: Diode softness test at T_j=125° C. Comparison between a module with standard diodes and a module containing FCE-diodes.

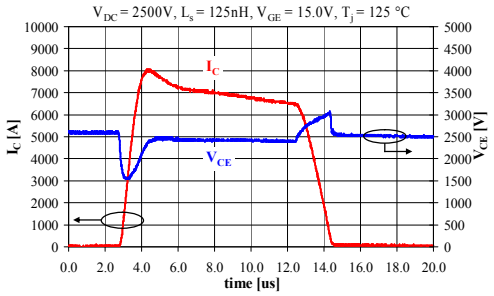

Figure 10: EP-IGBT short-circuit test at 125 °C.

Temperature Induced Current Mismatch in 3300V Modules during dynamic avalanche and SSCM

The extreme ruggedness of the 3300V/1200A SPT-IGBT modules with SSCM capability has enabled us for the first time to study the effect of externally induced temperature variations on the current mismatch between parallel IGBT modules tested under extreme RBSOA conditions.

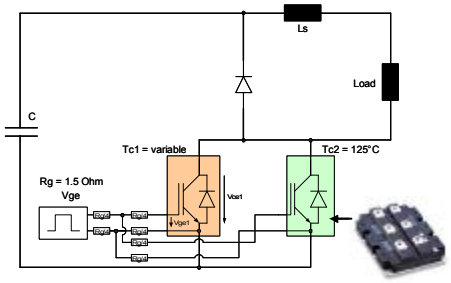

Figure 11: Measurement set-up for turn-off of parallel-connected IGBT modules, where the modules are at different temperatures. Each of the schematic switches corresponds to a full 3300V/1200A module.

By forcing large temperature variations between the two parallel modules, the current redistributions were magnified, and therefore, can be better analyzed for exploring the limits of device operation under such extreme conditions. This work was especially focused on current mismatch effects and redistribution mechanisms during dynamic avalanche and Switching-Self-Clamping-Mode (SSCM). The measurements were done using the test set-up shown in figure 11. By maintaining one module at a fixed temperature of 125 °C, and varying the second module temperature between 25 °C and 125 °C, a full set of turn-off results were obtained for the current sharing mechanisms. The two modules were capable of turning-off 6000A at a DC-link voltage of 2600V, in spite of a forced temperature difference of up to 100 °C. Figures 12 and 13 show RBSOA turn-off waveforms for two cases, where the variable-temperature module was tested at 105 °C and 25 °C, respectively. As expected, the waveforms show a clear trend in increased current mismatch with increasing temperature difference between the modules.

We will now shortly analyze the waveforms in fig. 13. The temperature mismatch was in this case 100 °C, showing a number of distinct phases with substantial current redistributions between the two modules. The current mismatch during the switching transient will depend on the following temperature dependent parameters: MOS-channel injection (threshold voltage and transconductance), excess carrier concentration in the N-base (lifetime, mobility and anode emitter efficiency) and avalanche generation (critical electric field). Prior to the switching transient (at t<0µs), the cooler module carries a significantly higher current due to the positive temperature coefficient of the IGBT chips. In order to explain the current redistribution mechanism during the switching transients, the following observations are important: Firstly, during conduction, the hot IGBT has a higher plasma concentration in the N-base than the cold one in spite of its lower current density. This can be explained by the lower mobility, the higher lifetime and the

higher anode emitter efficiency of the hot IGBT. Secondly, as derived in [7], the initial voltage rise dV_{CE}/dt will depend on the cathode current density J_C and the initially stored carrier plasma concentration. For a given plasma concentration, dV_{CE}/dt will increase with increasing J_C. On the other hand, for a given J_C, dV_{CE}/dt will decrease with increasing plasma concentration in the N-base. In parallel operating IGBTs, V_{CE} has to be the same across both devices and therefore, the current will always redistribute into the *slowest* IGBT (the one, which has the lowest dV_{CE}/dt when switched alone).

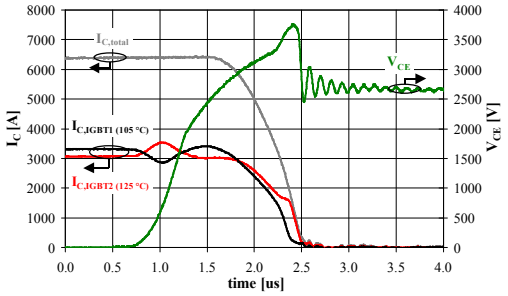

Figure 12: Turn-off of parallel-connected modules with a temperature difference of 25 °C. There is moderate current redistribution.

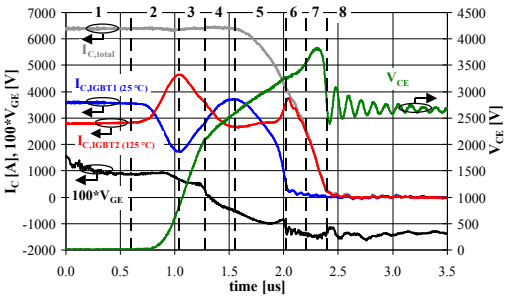

Figure 13: Turn-off of parallel-connected modules with a large temperature difference of 100 °C. A large current redistribution was observed.

In stage 1, the gate-drive begins to discharge the IGBT gate and V_{GE} starts dropping. However, both IGBTs are still in the active (on-state) region. During stage 2, the gate voltage drops further and the MOS-channel of both IGBTs enters the saturation region and V_{CE} starts rising. In this stage, the stored charge in the IGBT will determine the further course of the switching transient. Coming into stage 2, the hot IGBT has both a higher plasma concentration and a lower current density, which means that it is the slower one in terms of dV_{CE}/dt. As discussed above, the current therefore has to commutate from the cold to the hot module. At the beginning of stage 3, V_{GE} drops below the threshold voltage of the cold IGBT. In this stage, dV_{CE}/dt is still determined by the hot module, which is limited by the higher stored plasma concentration. The channel injection in the cold IGBT comes to an end, and as a consequence, dynamic avalanche sets in. This slows the cold IGBT down and as a result, the current starts again to redistribute from the hot to the cold module. At this point, the voltage waveform presents no evidence that the cold module is in dynamic avalanche because the total voltage rise is still determined by the hot module. In stage 4, the hot module also enters into dynamic avalanche. Avalanche generation will, however, be higher in the cold IGBT due to the temperature dependence of the critical electrical field. The high avalanche generation will therefore slow down the cold IGBT, which will once more force the current to redistribute from the hot to the cold module. Up till the end of stage 4, the total current in the two modules remains at 6000A. During stage 5, the total current starts dropping. Due to the fact that the cold IGBT originally had a lower stored plasma concentration than the hot one, the electric field has in this stage penetrated deeper into the N-base and consumed most of the stored charge. Therefore the current in the cold module starts dropping and reaches zero in the beginning of stage 6. All the current now flows in the hot module, which still has a significant stored charge, whereas the cold module has reached its static off-state. In stage 7, the hot module will also run out of charge. Throughout this stage, there is still a substantial energy stored in the stray inductance, which does not allow the current to drop to zero. Instead, the hot module enters into SSCM and dissipates this stored energy. Finally, in stage 8 the current in the hot module has reached zero and the turn-off transient is completed.

Conclusion

We demonstrated that future high power IGBT modules will be capable of providing electrical performance not matched to date in terms of low losses, soft turn-off characteristics, square RBSOA, and full over-current and over-voltage self-protection mechanisms under fault conditions. Results were presented from prototype modules incorporating heavily paralleled 3300V chips employing the next generation *Enhanced-Planar IGBT* technology and the *Field Charge Extraction* diode concept. The two technologies will provide the module with outstanding characteristics, therefore promising higher levels of performance in tomorrow's applications. In addition, results from measurements where two 3300V IGBT modules were tested in parallel under extreme RBSOA conditions with a forced temperature mismatch of up to 100 °C were presented. The modules showed excellent ruggedness and capability of withstanding both dynamic avalanche and SSCM in spite of the temperature induced current mismatch and associated redistribution mechanisms.

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