A New Generation of Asymmetric and Reverse Conducting GTOs and their Snubber Diodes

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Abstract

Transparent Emitter Technology combined with the buffer layer structure allows gate turn-off thyristor (GTO) designs with 50 % lower dynamic losses. Gate drive requirements are considerably reduced and the thinner silicon material used allows monolithic integration of the free-wheel diode with good dynamic performance. Diode lifetime profiling is used in a new generation of snubber diodes for rugged and soft recovery under Undeland/Marquardt or McMurray snubber conditions.
Technical breakthroughs are discussed which enabled the transparent buffered anode to be realised and device characteristics are described.

1. Introduction

Buffer layer structures to increase the blocking voltages of power devices have been known for a long time. The benefit of such $n^+pn^-np^+$ or n^+pinp^+ devices is that the field is stopped in the n layer. This means that the electric field in the n-base can now have a trapezoidal instead of a triangular form. The thickness of the wafers can be drastically reduced. Hence on-state losses and dynamic losses are reduced. However, the incorporation of a buffer layer in a GTO presented difficulties in the past. The major problem was that the buffer layer increases the efficiency of anode shorts during turn-on. The reason is that the buffer layer with its high conductivity is placed between anode and n-base. Thus the electrons flowing through the n-base are collected in the buffer layer and flow laterally along the anode junction through the shorts. The voltage drop in the buffer is lower than in a comparable structure without buffer layer. Thus the amount of anode shorts has to be reduced to ensure good turn-on properties. However, this degrades *turn-off* and it is much more difficult to find a compromise between turn-on and turn-off properties for anode-shorted buffer-layer GTOs. To overcome this difficulty ABB Semiconductors applied the concept of a buffer layer in combination with a thin homogeneous low-efficiency anode emitter [1] (Figure 1). The design of this transparent emitter is such that electrons have a high probability of crossing the emitter without the injection of holes. Thus, there is no need to incorporate anode shorts in order to decrease turn-off losses. The advantage of this approach is a combination of low turn-off losses and low gate-trigger currents. During *turn-on*, the anode current at which hole injection starts is not defined by a lateral voltage drop as it is for an anode shorted GTO. During *turn-off*, the electrons are not confined in the n-base and the tail phase is very short.
The Transparent Emitter GTO has been used successfully in combination with hard drive for some time [2]. This means under typical turn-off conditions di_{GQ}/dt is around 3500 A/µs and turn-off gain is of the order of unity. Today Transparent Emitter GTO wafers in low-inductance housings for hard drive applications are commercialised as Gate Commutated Thyristors or “GCTs”. A GCT together with an appropriate gate driver is commercialised as the Integrated Gate Commutated Thyristor or IGCT. However, the concept of the Transparent Emitter GTO can also be used to fabricate robust GTOs for standard applications with *conventional* gate units. Under such gate conditions during turn-off, di_{GQ}/dt is 30 to 100 A/µs and turn-off gain of the order of 4-5. The aim of this paper is to present a family of new 4.5 kV and 6.0 kV buffer-layer GTOs for such purposes. The GTOs are encapsulated in standard industry housings and are fitted with conventional gate leads.

2. Design

2.1 Blocking Voltage.

The first design parameter is the blocking voltage V_{DM} of the device. The blocking voltage of a buffer layer GTO is given by the avalanche breakdown of the main blocking junction alone. This is in contrast to classical GTOs where punch-through can limit the maximum blocking voltage as well. To reduce device thickness, the resistivity of the base material should be as high as possible, leading to an almost rectangular field distribution in the device.

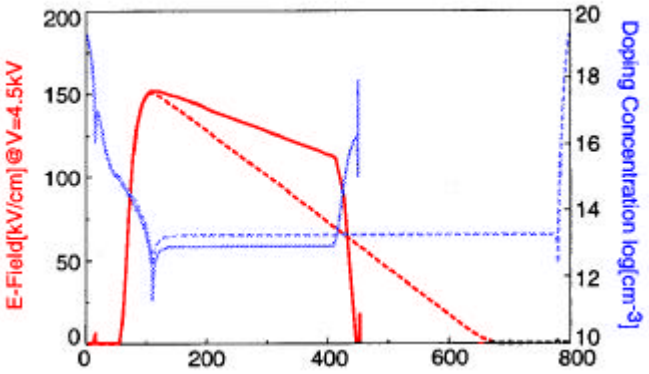


Figure 1: Comparison of doping profiles (grey) and electric field (black) of a non punch-through (- -) and a buffer layer GTO (—). The electric field is calculated at a blocking voltage of 4.5 kV. It can be seen that the thickness of the wafer can be reduced by roughly a factor of two.

After discovering that for increased dc link voltages a major part of failures was induced by cosmic radiation, a second design criterion for high voltage semiconductors had to be taken into account. This design criterion ensures that the probability of a failure caused by cosmic radiation is below a certain limit. A modern GTO is designed to have less than 100 FIT at the specified dc link voltage due to cosmic ray induced failures. 1 FIT corresponds to one failure in $1*10^9$ hours. Again, a high resistivity of the n-base is favourable as is shown in Figure 2. There the calculated FIT rate for a given thickness of the n-base is given as a function of n-base resistivity.

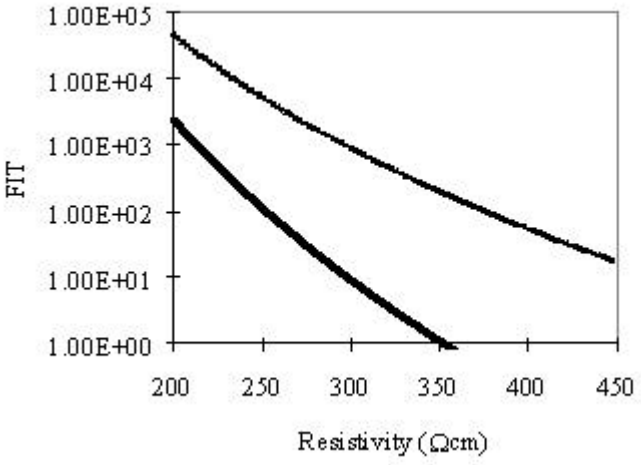


Figure 2: Calculated failures in time due to cosmic radiation at sea level for a buffer layer GTO with an n-base thickness of 400 µm [3]. The calculation assumes dc link voltages of 2.2 kV (—) and 2.8 kV(- -) respectively. The silicon area is 60 cm^2.

Both design criteria depend on the electric field. The maximum blocking voltage is a function of the peak electric field at the blocking junction and the junction termination. The field dependence of the cosmic ray induced failures is much more complicated. A model for this failure mode is given in [3], which allows a prediction of the FIT-rate as a function

of the electric field distribution. It turns out that the design criterion to achieve less than 100 FIT due to cosmic ray induced failures is very restrictive. Thus ABB buffer-layer GTOs are capable of blocking considerably more than the specified maximum blocking voltage.

2.2 Design of RC-GTOs

In the past, in contrast to diodes, most GTOs had no buffer layer structure. This means that GTO wafers were much thicker than diodes. Because the thickness of an RC-GTO was given by the thicker wafer, the design of the diode was far from optimal. Hence, the benefits expected from the integration of both devices on the same wafer were off-set by the high losses of the diode. The success of transparent emitter technology allows integration of a freewheeling diode with acceptable losses and a GTO on the same wafer, because the resulting diode design is close to that of an optimised discrete diode.
A second problem with first generation RC-GTOs was that both GTO and diode share a common main blocking junction. If no special measures are taken, gate current can flow through the common p-base into the anode of the diode. This is a short circuit for the gate current because the anode of the diode and the cathode of the GTO are at the same potential. In the past, two approaches have been proposed to introduce a separation between the p-bases of the GTO and the diode. Firstly a groove can be etched into the p-base. Secondly the p-base can be separated by a small n-conducting region (Figure 3).
One disadvantage of the resistive separation region is that the negative gate current I_{GRM} is increased compared to that of a standard asymmetric GTO. This increases the requirements on the gate-unit during GTO blocking. To obtain an acceptably low value of I_{GRM} the resistance of the separation should be as high as possible. However, this requires a broad separation region reducing the area available for the active parts of the device [4]. The main advantage of the second method is that the current flowing between gate and anode of the diode has no resistive part. Hence I_{GRM} is low, comparable to that of a conventional asymmetric GTO. In addition the area consumed by the npn separation structure is very small, resulting in an optimised use of the wafer area.

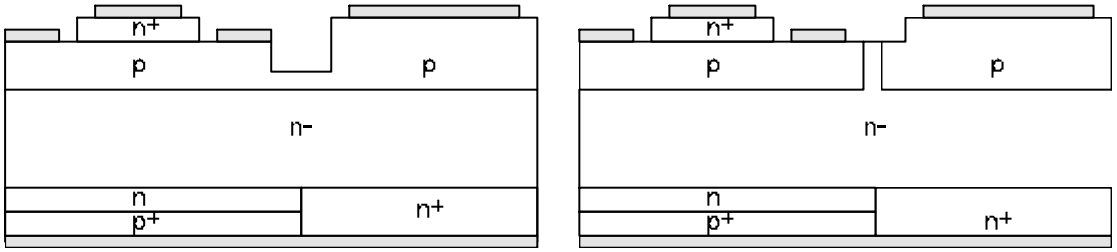


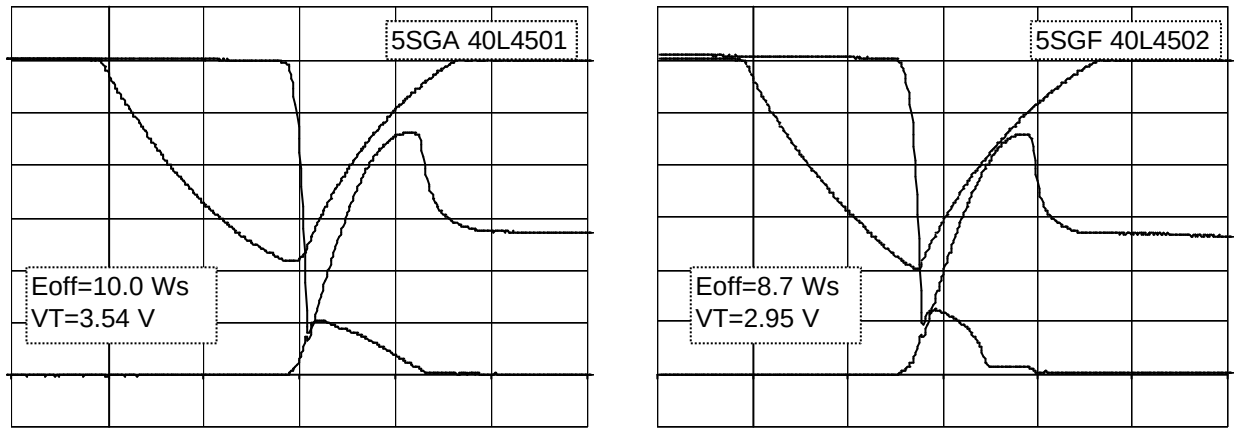
Figure 3: Comparison of resistive separation with pnp separation of a GTO and integrated freewheeling diode. The advantages of the pnp separation are very low gate leakage currents, I_{GRM}, and high blocking stability.

3. Buffer-Layer GTOs for Diverse Requirements

When the development of buffer layer GTOs started, the device was considered as ideal for hard gate drive. In contrast to classical drive, under hard-drive conditions the cathode stops injecting electrons before an electric field starts to be built up over the main blocking junction. Hence under these conditions, turn-off is homogeneous and the generated heat is distributed uniformly over the device. Indeed a device designed for 100 FIT due to cosmic ray induced failures is capable of turning off a very high current density under hard drive gate turn-off, despite its very low thickness.
Under classical drive conditions, the buffer layer GTO optimised for hard drive has reduced turn-off capabilities compared with a conventional GTO of the same diameter. Such devices can, however, be used for applications where extremely low losses are required and demands on turn-off capability are lower (type 5SGT 30J4502). The dependence of the turn-off capability on device thickness has been known for anode shorted GTOs for a long time. Hence, to increase the turn-off robustness of a buffer layer its thickness has to be increased as well. An increase of device thickness results, of course in higher on-state and switching losses.

3.1. New 4.5 kV Buffer-Layer GTOs for High Frequency Application and Retro-fitting of Former GTOs

New low-loss high-frequency GTOs from ABB Semiconductors are based on the Transparent Emitter Technology. A wafer with a diameter of 85 mm is encapsulated in a 108 mm industry standard housing (type 5SGF 30J4502) and a wafer with a diameter of 91 mm in a 120 mm industry standard housing (type 5SGF 40L4502). Both are designed to switch 3 kA with 3 µF snubber capacitance. The exceptionally low dynamic and static losses of these devices enable them to retrofit former 3 kA GTOs of the same voltage class. To ensure compatibility with existing applications and gate units a small number of anode shorts was introduced [5]. This increases the gate trigger current to a level comparable to former anode shorted non punch-through devices. Anode shorted devices are labelled as F-types to distinguish them from the non shorted T-types. In Figure 4, waveforms of a conventional non punch-through GTO (type 5SGA 40L4501) and a buffer layer GTO (type 5SGF 40L4502) are compared. The main differences for the application are the reduced storage times and losses as well as the waveforms of the tail currents. These new F-types are thus "backward compatible" with earlier generations of GTOs and are intended for new designs and retrofitting former devices.
The difference in the tail-current waveform can be explained as follows. In a conventional GTO the electrical field never reaches the anode. The tail current, resulting from the removal of charge carriers from the n-base, drops slowly to zero. At the end of the tail phase, it drops to a lower value as a consequence of the decrease of the voltage after V_{DM}. In the buffer-layer GTO, the tail current can be divided into two parts. In the first part, the current is comparable to that of a conventional GTO. In this part, the electric field has not yet reached the buffer layer. Then, before V_{DM} is reached, the electrical field „punches" to the buffer layer. Now all the excess charge in the n-base has been removed and the current drops to a low value. In the second part of the tail phase, the current is almost constant. The origin of this current is the removal of excess charge confined between n-base and anode emitter in the buffer layer.



I_T: 500 A/div; I_G: 200 A/div; V_D: 1000 V/div; Time: 10 µs/div.

Figure 4: Comparison of turn-off waveforms of conventional non punch-through GTO (type 5SGA 40L4501, left) and buffer layer GTO (type 5SGF 40L4502, right). A 3000 A current is switched off with Cs = 3 µF, Ls = 250 nH, di_{GQ}/dt = 40 A/µs at 125 °C. The on-state of the buffer-layer GTO at 3000 A and 125 °C and the switching losses are lower compared to the non-punch-through device. The main differences in behaviour are the reduced storage times and the form of the tail current.

3.1.1 Comparison between Ratings of Buffer-Layer and Conventional GTOs

The potential of the new buffer-layer devices for retrofitting former devices is illustrated by a comparison of ABB 3 kA GTOs in 108 mm wide industry-standard press-pack housing in Table 1. It can be seen that although the 5SGF 30J4502 is designed for 2800 V DC link voltage, the losses are lower than the ones of a former device designed for 2200 V DC link.

Type	$V_{DC\ link}$ (V)	VT (V) 3000 A, 125 °C	Eoff (Ws) 3000 A, 125 °C , Cs=6µF
5SGA 30J4505	2200	3.5	10
5SGA 30J4502	2800	4.0	12
5SGF 30J4502	2800	3.9	8

Table 1. Comparison of data-sheet values of 3 kA 4.5 kV GTOs. The new buffer layer GTO combines the high dc-link voltage of the 5SGA 30J4502 and the low static and dynamic losses of the 5SGA 30J4502.

3.1.2 Frequency Testing

In the frequency test, GTOs are stressed under application-like conditions, as would be found in a locomotive or in an industrial drive. In contrast to parameter testing, where devices are exposed to single shots for measuring turn-on and turn-off parameters, the frequency test, as its name implies, repetitively switches DUTs on and off at the rated current, with a switching frequency of 150 to 300 Hz, depending on the type of GTO and its specific load profile.
Frequency testing is a very powerful tool for assessing the ruggedness of GTO thyristors. ABB Semiconductors uses test equipment designed to stress GTOs under very hard turn-on as well as turn-off conditions.

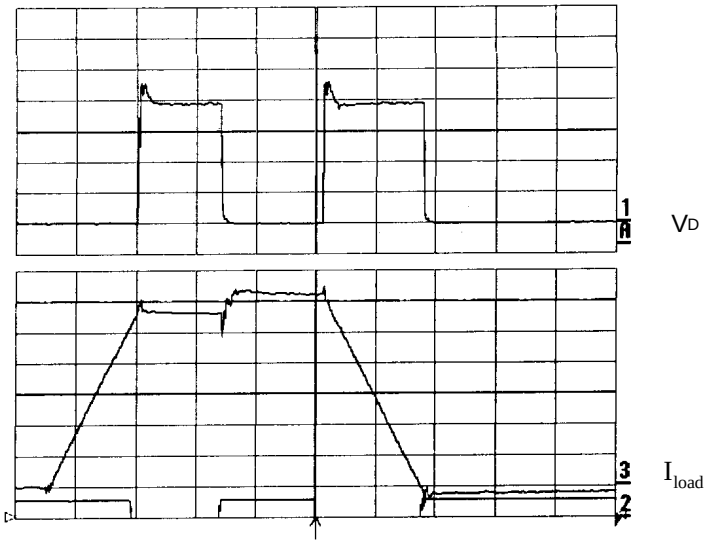


Figure 5: Current and voltage waveforms of a buffer layer GTO (ABB type 5SGF 30J4502) during frequency testing. In the upper part the voltage of the DUT is shown. In the lower part the current in the load is shown. (t: 200µs/div, I: 500A/div, U: 1kV/div)

3.2. Reverse Conducting GTOs

A reverse conducting GTO has been developed based on the technology of the “backward compatible” F-type GTOs and the new separation region concept described in Section 2.2. The wafer has a 91 mm diameter and is encapsulated in a 120 mm housing. As with the F-type GTOs, the reverse conducting GTO has a turn-off capability of 3 kA with a 3 µF snubber capacitance. Because of the smaller GTO area, the reverse-conducting GTO has a slightly higher on-state than the F-type device.
To demonstrate the performance of the new separation region, the reverse characteristic of the gate-cathode junction at 25 °C is given in Figure 6. As described in Section 2.2, there is no resistive contribution from the separation region. The leakage current is small below the avalanche breakdown of the gate cathode junction of about 22 V.

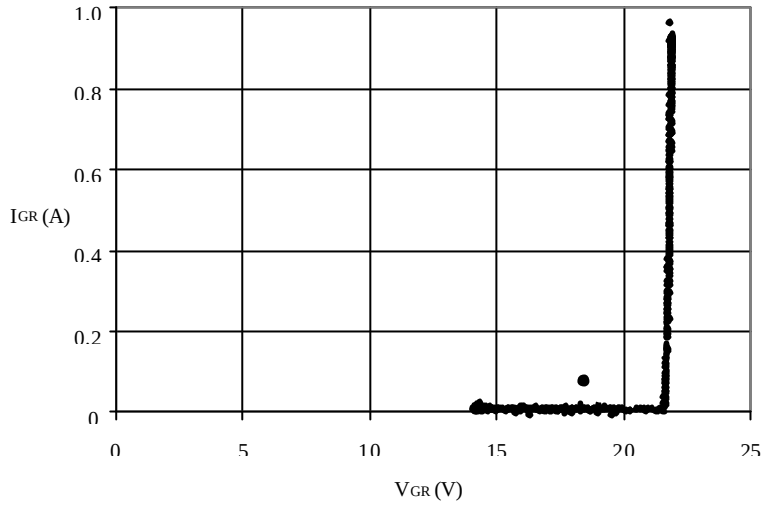


Figure 6: Reverse gate characteristic of RC-GTO

3.3. GTOs for Higher Voltage Classes

The buffer-layer design enables the fabrication of GTOs with higher voltage rating. Of special interest are devices for dc-link voltages around 3.8 - 4.0 kV. Therefore the new 6 kV devices are designed for less than 100 FIT due to cosmic radiation at a dc-link voltage of 4 kV. Because compatibility with former devices is less important in this voltage class, new high-voltage GTOs have *no* anode shorts and are labelled as *T-types* to distinguish them from elements suitable for retrofit applications. In Figure 7, the turn-off waveforms of an 85 mm wafer (type 5SGT 30J6004) are given.

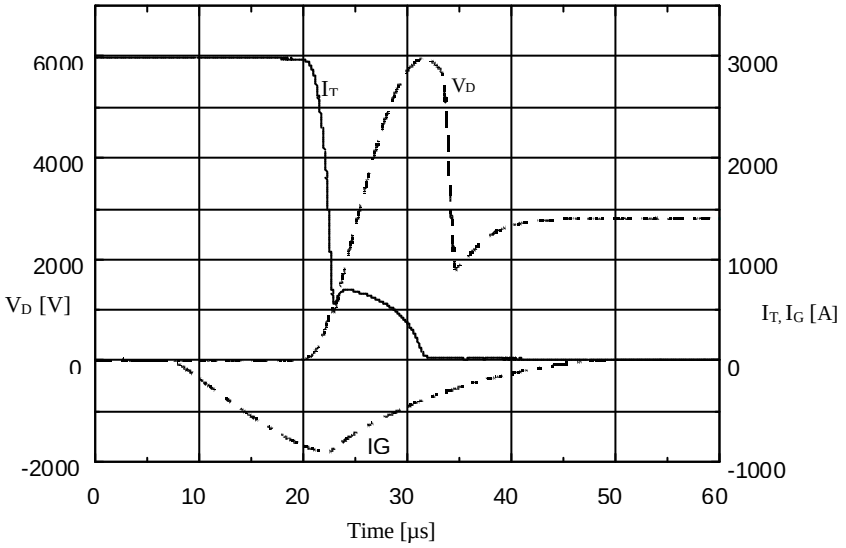


Figure 7: Turn-off waveforms of a 6 kV buffer layer GTO. The on-state of this device is 3.25 V at 3 kA and 110 °C. The turn-off conditions are Cs = 2.66 µF, Ls ≈ 250 nH di_g/dt = 70 A/µs, T = 110 °C.

4. Snubber Diodes

In all GTO or IGCT applications, high performance diodes are a must. As the performance of the active switches improves, pressure increases for corresponding advances in diode behaviour.

4.1 Commutation Behaviour of Diodes

The diodes specified for fast switching GTO, GCT or IGBT applications must feature not only low static and dynamic losses, but must also demonstrate exemplary recovery behaviour. In most applications, the critical need to minimise stray inductance between switch and associated snubberless diode encourages super-fast diode commutation. Such commutation places a premium on low reverse peak current I_{rr}, and "soft recovery" performance. In order to achieve "soft recovery", it is necessary that, at the instant of maximum reapplied voltage, sufficient carriers remain available to support the required "tail current".
To obtain a low reverse recovery peak, the flooded pn junction must be rapidly depleted.
Among various possible methods to achieve these aims, ABB Semiconductors favours local lifetime control in order to ensure the best trade-off between on-state and dynamic losses, while maintaining ideal recovery behaviour under all conditions of operation.

4.2 Diode Design and Technology

Blocking voltage and DC withstand capability as described in Section 2.1 for GTOs have to be taken into account for diodes too. Carrier lifetime is usually adjusted in order to optimise the trade off of static and dynamic losses. The charge carriers in a diode, unlike those in GTOs, are extracted through the anode and cathode immediately after the voltage is reversed. As a consequence, in a device with uniform axial lifetime distribution (i.e. electron irradiated), a space charge region is formed not only across the pn-junction, but also across the n+/n-junction. This results in a virtual reduction of the usable base region (Figure 8) and consequent snap-off of the reverse current at the moment when the two space-charge regions meet at voltages lower than the static punch through voltage. Due to the lower recombination rate and consequently greater diffusion of holes into the base region of the device with profiled lifetime, the slope of the electric field is steeper as compared to the device with uniform lifetime.

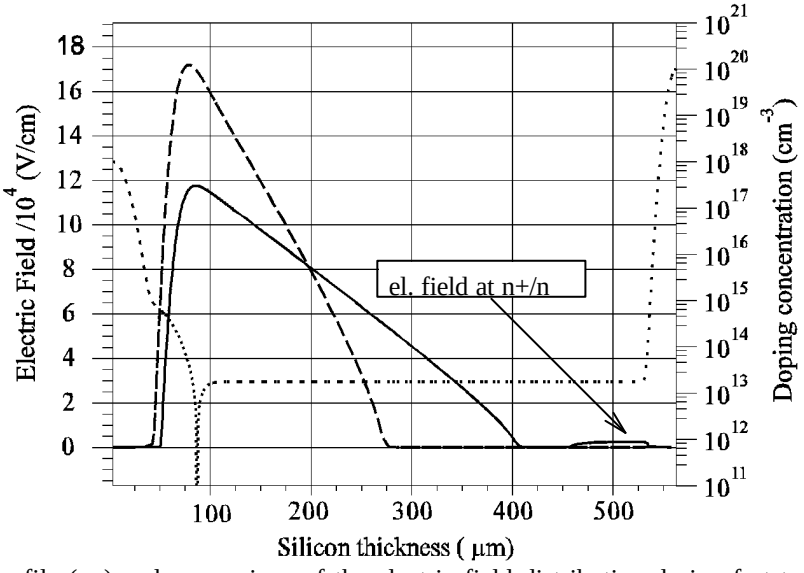


Figure 8: Doping profile (---) and comparison of the electric field distribution during fast turn off in devices with electron irradiation (——) and proton irradiation (———). Voltage is the same in both cases.
hole distribution of an electron (– –) and a proton (——) irradiated device.

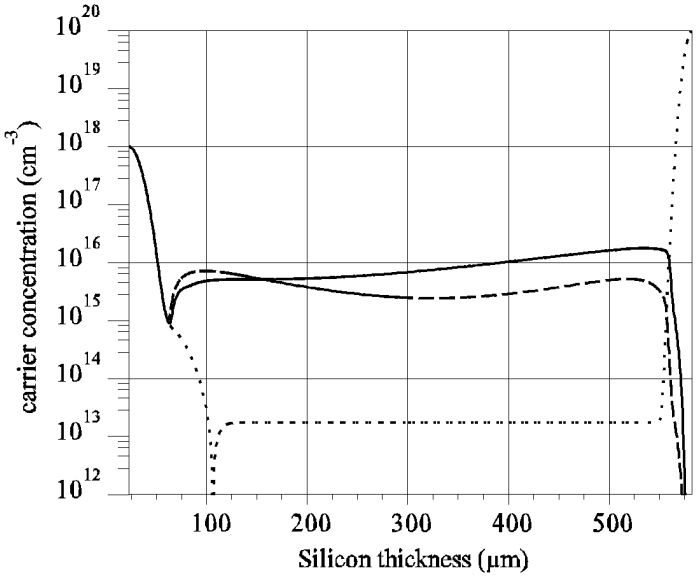


Figure 9: Doping concentration (- -) and comparison of hole distribution of an electron (– –) and a proton (——) irradiated device.

This in turn also delays the "punch through" of the space charge region towards the cathode stopping layer and therefore supports "soft recovery" even up to voltages beyond static punch through voltage.
Formation of the n+/n-space charge region can be widely suppressed and an advantageous dynamic electric field distribution can be obtained by the appropriate tailoring of the carrier distribution during on state.
Consequently, snap-off does not occur before the depletion region punches against the n+ stopping layer. Figure 9 illustrates the hole distribution in the device after the application of reverse voltage, before the reverse current peak is reached.
While the trade-off of static and dynamic losses alone can easily be adjusted by homogeneous lifetime profiling, as produced by electron irradiation, more versatile tools, such as controlled heavy metal diffusion or light ion irradiation, are required to shape the reverse recovery waveforms to the requirements of the particular application.

4.3 Electrical Behaviour of Proton Irradiated Diodes

A test circuit to evaluate the behaviour of snubber diodes under worst case conditions is given in Figure 10. Figure 11 compares the turn-off waveforms of a snubber diode with homogeneous lifetime (that is, a distribution of recombination centres as determined by electron irradiation) with those of a proton and electron irradiated device (5SDF 03D4501).

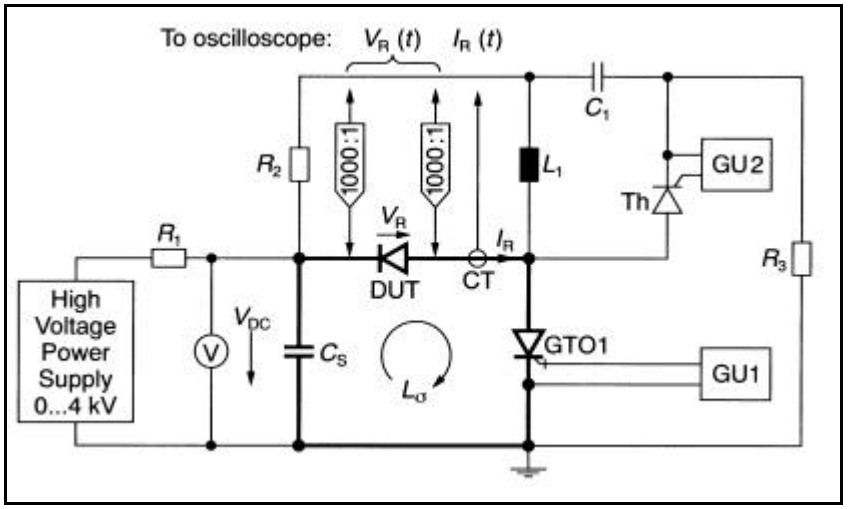


Figure 10: Test circuit to evaluate the behaviour of snubber diodes under worst case conditions
The commutation loop is drawn in **bold**
DUT: Diode under test (clamped in a heated press)
GTO_1: Fast-switching GTO whose turn-on characteristic mainly determines the turn-off-stress in the DUT
C_S: Snubber capacitor, initially charged to V_{DC}
L_σ: Stray loop inductance (≈ 200 nH)
R_2, L_1, C_1, Th and R_3 generate the forward current (10-150 A) in the DUT before GTO_1 is fired.

The forward current density through the device is about 13 amps/cm^2, the di/dt at zero crossing is approximately 500 amps/µs and exceeds 1000 amps/µs before the reverse current peak is reached. No DUT-snubber is applied.
The electron irradiated diode shows severe "snap off", at a source voltage of 3.2 kV, whereas the 5SDF 03D4501 exhibits “good-natured“ (soft) behaviour, even at 3.5 kV. Also, I_{rr} of the proton-irradiated diode is lower by about 30%. Silicon material and diffusion profiles are the same for both devices.

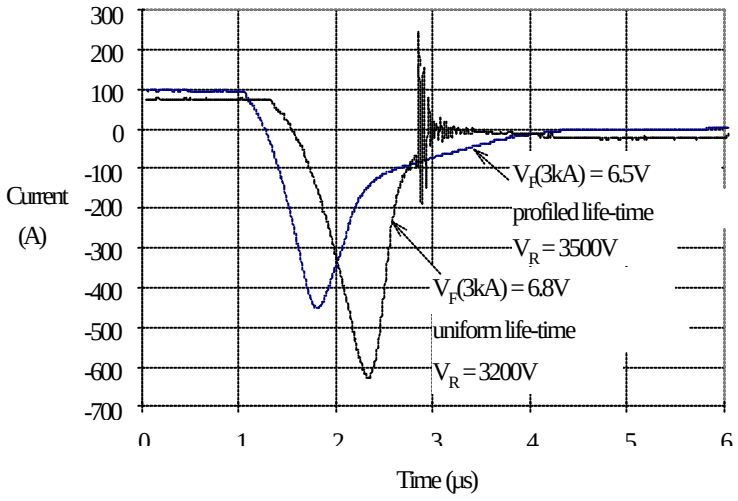


Figure 11: Comparison of different lifetime technologies in 4.5 kV snubber diodes. Note the different source voltages.

Figure 12 illustrates current and voltage waveforms of the same 5SDF 03D4501 as above, turned off from an extremely low forward current density of about 1A/cm^2, where snap-off is even more likely to occur. Even under these conditions, the device performs very well.

Table 2 is a comparison of the major characteristics of this product, with those of a gold-doped and an electron irradiated diode. It shows, unequivocally, that a lower dynamic forward voltage (V_{fr}) and lower leakage current are the additional benefits of ion irradiation.

Lifetime Technology	Blocking		Turn-off @ di/dt = 100 A/us, V_{dc} = 1000 V, I_F = 1000 A			Turn-on @ 1000 A/us	
	V_F @ 3000A, 125°C	leakage current @ 4.5 kV, 125 °C	I_{rr}	Q_{rr}	s-factor	V_{fr} @ 25°C	V_{fr} @ 125°C
gold	6.5 V	24 mA	185 A	615 mC	1.2	90 V	145 V
electrons	6.8 V	6 mA	235 A	585 mC	0.7	55 V	120 V
protons	6.5 V	11 mA	175 A	620 mC	1.4	52 V	115 V

Table 2: Comparison of snubber diodes with different lifetime technologies.

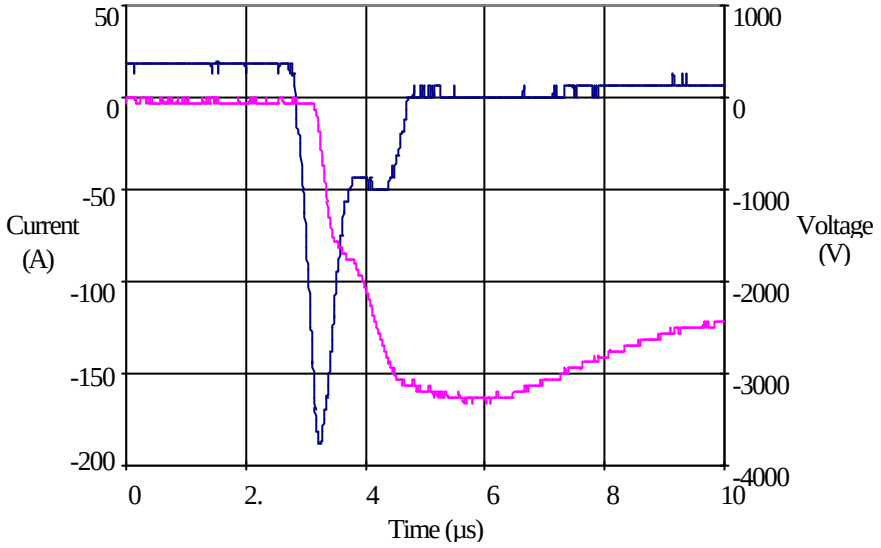


Figure 12: 5SDF 03D4501in Undeland/Marquardt circuit, I_F = 10 A, V_{dc} = 3500 V, T = 110 °C

5. Conclusion

The concept of a buffer layer GTO with transparent emitter is not only applicable to GTO wafers designed for application with hard gate-drive (GCTs), but also for applications using conventional gate drivers. Losses can be drastically reduced compared to former non-punch-through devices. This enables the development of GTOs with high dc-link withstand capabilities combined with low losses. These new devices are appropriate to retrofitting former high dc-link and low dc-link GTOs with just one device. The new buffer-layer technology enables the integration of a freewheeling diode onto the GTO wafer. New lifetime profiling techniques allow the development of rugged diodes with controlled recovery for snubberless forced commutation at high values of di_r/dt.

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