AboCom System, Inc.

Product Specification

GS1KMEPA
(Green Product)

High power WiFi module

Producing Place: Factory: No.77, Yu-Yih Rd., Chu-Nan, Miao-Lih County 35059, TW R.O.C.

Made in Taiwan

Table of Contents

1. Revision History

Date	Release	Author	Description
2012/07/27	0.1	Paula	First version release

2. Related Documents

Date	Author	Document

3. Introduction

The GS1KMEPA based modules provide cost effective, high power, and flexible platform to add Wi-Fi® connectivity for embedded devices for a variety of applications, such as wireless sensors and thermostats. It combines ARM7-based processors with an RF transceiver, 802.11 MAC, security, & PHY functions, FLASH and SRAM, onboard and off module certified antenna options, and various RF front end options for end customer range needs in order to provide a WiFi and regulatory certified IEEE 802.11 radio with concurrent application processing services for variety of applications, while leverage existing 802.11 [1] wireless

network infrastructures.

4. Main Features

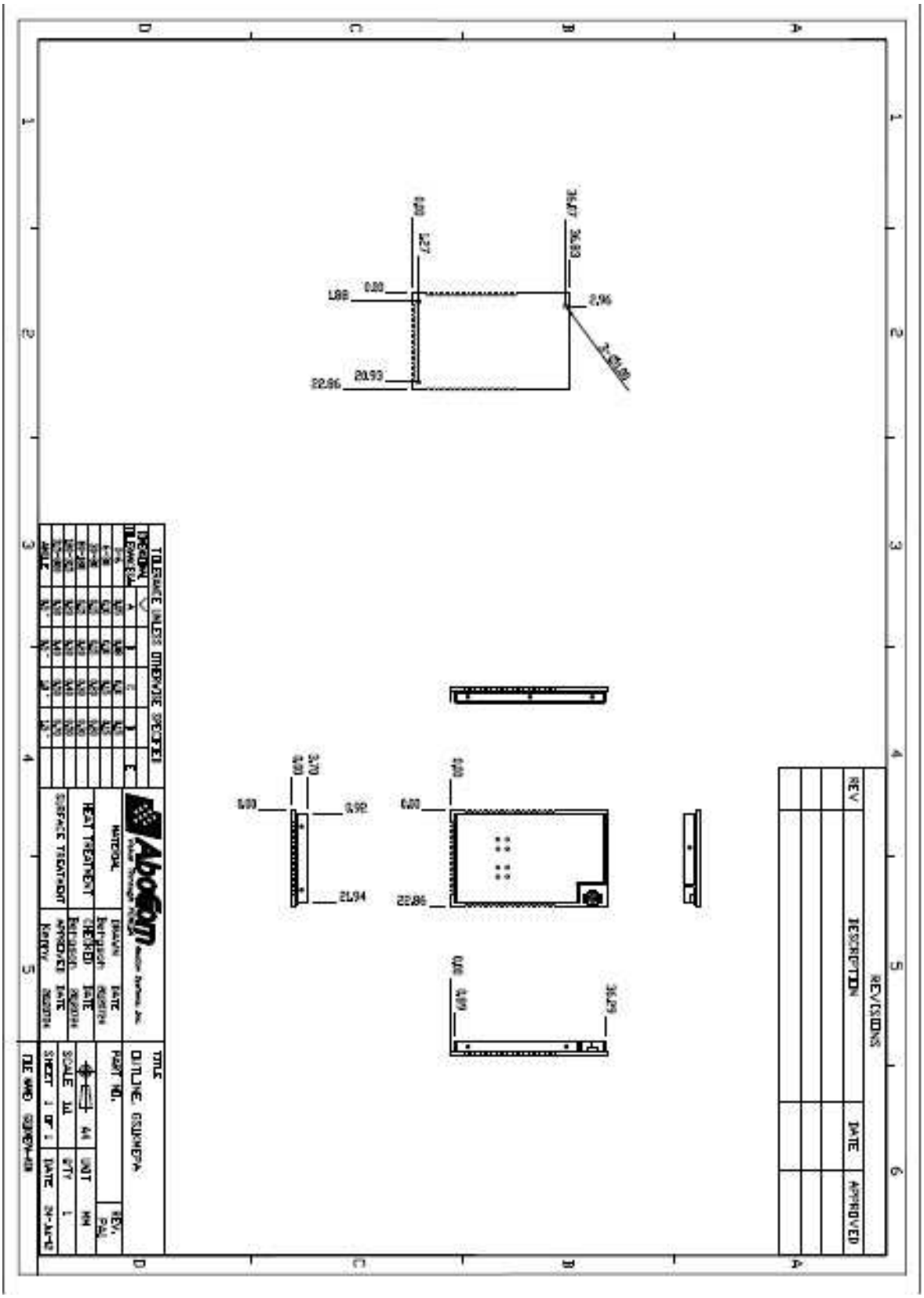
- GS1KMEPA 1.450 inches by 0.900 inches by 0.143 inches (Length * Width * Height) 48-pin Dual Flat pack PCB Surface Mount Package.
- Compliant with IEEE 802.11and regulatory domains
- Dual ARM7 Processor Platform
- Interfaces is external antenna
- Embedded RTC (Real Time Clock) can run directly from battery.
- Power supply monitoring capability.
- Low-power mode operations (Sleep, Deep Sleep, and Standby)

5. Specification

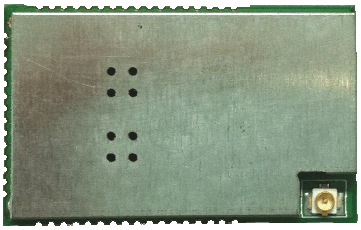
5.1. Physical Specifications

Standard	IEEE 802.11 b standards
Chipset / Mac/BB/RF Processor	GainSpan GS1011
Wireless LAN	1T1R mode
RF Connector	U.FL connectors
Antenna Designs	SMA antenna
Frequency Range	2.412 ~ 2.4835GHz (subject to local regulations)
Number of Selectable Channels	USA,Canada(FCC):11 channels (2.412GHz~2.462GHz) Europe (CE): 13 channels (2.412GHz~2.472GHz) Japan (TELEC): 13 channels (2.412GHz~2.475GHz)
Data Rate	802.11b: 1, 2, 5.5, 11Mbps 802.11g: None 802.11n: None
Output Power	11b: 23dBm(default) +/- 1dBm 11g: None 11n: None
Receiver Sensitivity	11b: 11Mbps 8% PER ~ -85dBm(default) 11g: None 11n: None
Power Consumption	Idle : 40 mA Continue TX : 750mA/3.3V Continue RX : 160mA/3.3V
Environmental Requirement	**Operating** Temperature :-40 ℃ ~85 ℃ Humidity : 10% to 90% (Non-Condensing) **Storage** Temperature : -55 ℃ ~125 ℃ Humidity : 10% to 95% (Non-Condensing)
Physical Specifications	Weight : 4 g Dimension : L:37mm X W:23mm X H: 4mm

5.2. Dimension :



5.3. Mechanical Designs



5.4. Pin define:

Pins	Name	Voltage Domain	Internal Bias after hardware reset	Signal State	Description
1	GND	0V	Not Applicable	Analog port	Ground
2	JTAG_TCK	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Clock
3	JTAG_TDO	VDDIO	Not Applicable	Digital Output	Joint Test Action Group Test Data Out
4	JTAG_TDI	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Data In
5	JTAG_TMS	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Mode Select
6	JTAG_nTRST	VDDIO	Pull-up (See Note 1)	Digital Input	Joint Test Action Group Test Mode Reset Active Low
7	ALARM1	VBAT	Pull-down (See Note 1)	RTC Input	Embedded Real Time Clock Wake Up Input 1
8	RTC_OUT1	VBAT	Not Applicable	RTC Output	Embedded Real Time Clock Wake Up Output 1
9	VBAT	VBAT	Not Applicable	Analog port	Embedded Real Time Clock Power Supply
10	DC_DC_CNTL	VBAT	Not Applicable	Digital Output	VIN_3V3 Regulator Control Output
11	ADC1	VDD18 (internal)	Not Applicable	Analog Output	General Analog to Digital Converter 1
12	ADC2	VDD18 (internal)	Not Applicable	Analog Output	General Analog to Digital Converter 2
13	ALARM2	VBAT	Pull-down (See Note 1)	RTC Input	Embedded Real Time Clock Wake Up Input 2
14	MSPI_DIN / GPIO6	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Data Input / General Purpose Input Output
15	MSPI_DOUT / GPIO7	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Data Output / General Purpose Input Output

16	VOUT_1V8	VIN_3V3 (internally regulated)	Not Applicable	Analog port	Internal 1.8V Vout
17	GND	0V	Not Applicable	Analog port	Ground
18	MSPI_CLK / GPIO5	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Clock / Gen-eral Purpose Input Output
19	MSPI_CS0 / GPIO4	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Chip Select 0 / General Purpose Input Output
20	MSPI_CS1 / GPIO13	VDDIO	Pull-down	Digital Input / Output	Master Serial Peripheral Interface Bus Chip Select 1 / General Purpose Input Output
21	GPO21_11MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output
22	GPO20_22MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output
23	GPO19_44MHZ	VDDIO	Pull-down	Digital Input / Output	Internal Clock Circuitry Test Point / General Purpose Input Output
24	PWM0 / GPIO10	VDDIO	Pull-down	Digital Input / Output	Pulse Width Modulator / General Purpose Input Output
25	I2C_CLK/GPIO9	VDDIO	Pull-down (NOTE 4)	Digital Input / Output	Inter-Integrated Circuit Clock / General Purpose Input Output
26	I2C_DATA/ GPIO8	VDDIO	Pull-down (NOTE 4)	Digital Input / Output	Inter-Integrated Circuit Data / General Purpose Input Output
27	SSPI_DOUT	VDDIO	Pull-up (See Note 1)	Digital Output	SPI Slave Transmit Data Output to the HOST
28	SSPI_CLK	VDDIO	Pull-up (See Note 1)	Digital Input	SPI Slave Clock Input from the HOST
29	SSPI_CS	VDDIO	Pull-up (See Note 1)	Digital Input	SPI Slave Chip Select Input from the HOST
30	SSPI_DIN	VDDIO	Pull-down (See Note 1)	Digital Input	SPI Slave Receive Data Input from the HOST
31	VIN_3V3	VIN_3V3	Not Applicable	Analog port	Single Supply Port
32	GND	0V	Not Applicable	Analog port	Ground
33	EN_1V8	VDDIO	Need to be driven HIGH or LOW externally	Digital Input	Internal 1.8V regulator enable port-Active High
34	VDDIO	VDDIO	Not Applicable	Analog port	All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply)

35	UART1_CTS / GPIO26	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Request to Send Output (See Note 6) / General Purpose Input Output
36	UART1_RTS / GPIO27	VDDIO	Pull-down (See Note 2)	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Request to Send Output (See Note 6) / General Purpose Input Output
37	UART1_RX / GPIO3	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Receive Input / General Purpose Input Output
38	UART1_TX/GPIO2	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 1 Transmitter Output / General Purpose Input Output
39	UART0_TX /PIO1	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Transmitter Output / General Purpose Input Output
40	UART0_RTS / GPIO25	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Request to Send Output (See Note 6) / General Purpose Input Output
41	UART0_RX / GPIO0	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Receive Input / General Purpose Input Output
42	UART0_CTS / GPIO24	VDDIO	Pull-down	Digital Input / Output	Universal Asynchronous Receiver Transmitter 0 Clear to Send Input (See Note 6) / General Purpose Input Output
43	GPO31_LED2	VDDIO	Pull-down	Digital Input / Output	Light Emitting Diode Driver / General Purpose Input Output
44	GPIO30_LED1	VDDIO	Pull-down	Digital Input / Output	Light Emitting Diode Driver / General Purpose Input Output
45	GPIO29	VDDIO	Pull-down (See Note 3)	Digital Input / Output	General Purpose Input Output
46	GPIO28	VDDIO	Pull-down (See Note 3)	Digital Input / Output	General Purpose Input Output
47	EXT_RESETn (See Note 5)	VDDIO	Pull-up	Digital Open Drain Input / Output	Module Hardware Reset Input and Power Supply Reset Monitor Indictor Active Low
48	GND	0V	Not Applicable	Analog port	Ground

Notes:

1. These pins have onboard hardware configured pull-ups/downs and cannot be changed by software.

2. If UART1_RTS is high during boot, then the WLAN will wait for Flash download via UART0. Route this pin on the base board so it can be pulled up to VDDIO for programming the module.

3. GPIO 28 and 29 are sampled at reset to establish JTAG configuration for debugging. These signals should not be driven from an external device. If using JTAG, configure these pins as outputs.

4. If I2C interface is used, provide 2K Ohm pull-ups, to VDDIO, for pins 25 and 26 (I2C_CLK and I2C_DATA)

5. EXT_RESETn is a active low signal. It is an output during power up, indicating to the system when GS1011 device is out of power-on-reset. After power-on-reset, this pin is an input. It is not necessary to assert reset to the GS1011M after power on, since the GS1011 has a built-in power on reset. Also, the EXT_RESETn signal does not clear the RTC RAM or the SRAM.

6. CTS and RTS signals indicate it is clear to send or ready to send when they are LOW. If signals are high, indicates device is not ready.

5.5. Block Diagram :