TDC-GP2 to TDC-GP21 Migration and Compatibility Guideline

This paper is an add-on to the TDC-GP21 datasheet. It describes the functional and configuration differences between TDC-GP2 and TDC-GP21.

Hardware and Software Compatibility

The TDC-GP21 offers an extended architecture that, within some very small restrictions, is fully compatible to existing TDC- GP2 designs. According to its new features the GP21 configuration register architecture is extended compared to TDC-GP2. However, the device supports 100% downwards compatibility so there is no need for any hardware and software adaption when switching your design from GP2 to GP21.

- **I/O supply voltage**
  The GP21 I/O supply voltage (Vio) is limited to max. 3.6 V, compared 5.5 V with TDC-GP2.
- **Chip marking**
  Basically, the GP21 chip marking is identical except for one difference. Compared to TDC-GP2 the acam label on GP21 package might be rotated in some device charges. According to that we strongly recommend to check the position of the orientation indicator (and not the acam label) to ensure a correct PCB assembly of the device.
- **Fire out configuration**
  GP2 configurations where Fire1 and Fire2 are switched in parallel are not supported by the GP21. This leads to a misbehaving of your system as the GP21 fire pulse generator will not generate any output signals. In this case a small software modification is necessary that changes the settings of CONF_FIRE parameter in configuration register 5.

To get access to the device's extended functionality some hardware- and software modifications are necessary.

32 kHz Oscillator

Basically, the TDC-GP21 offers full clock signal compatibility to TDC-GP2. With GP21 the internal 32 kHz clock driver has an additional low power option. This reduces current consumption of the 32 kHz quartz to typ. 1 µA (compared to typ. 4.5 µA in GP2)

Table 1: Current consumption of 32 kHz clock source in GP2 /GP21

		TDC-GP2				TDC-GP21			
Symbol	Description	Min.	Typ.	Max.		Min.	Typ.	Max.	Unit
I32	Current 32 kHz		4.5				1.0		µA

Also the TDC-GP2 1 offers enhanced clock options for clock distribution via FIRE_IN pin. They are available via register 1 configuration. The following table provides the details:

Table 2: Parameters for enhanced clock options of TDC-GP21

Parameter	Terminal	Description	Value
SEL_TSTO2	Reg1[11:13]	Additional functionality of Fire_In pin for clock signal output	7 = 4 kHz out (32 kHz / 8)
SEL_TSTO1	Reg1[10:8]		7 = 32 kHz out
Curr32	Reg1[15]	Low power option for 32 kHz clock	1 = enabled (recommended) 0 = disabled

Time measurement unit

The base resolution of the GP21 is typ. 90 ps. In measure mode 2 it can be improved by setting Double resolution (typ. 45 ps) and Quad resolution (typ. 22 ps) mode. For GP2 compatibility the GP21 by default operates in standard mode (GP2 mode, 90 ps resolution). Configuring higher resolution requires write access to configuration register 6. This register is part of the extended register architecture of the TDC-GP21. Setting bit 12 or 13 activates double or quad resolution mode

Table 3: GP21 Double and Quad resolution mode

Parameter	Terminal	Description	Value
QUAD_RES	Reg6[13]	Improves resolution from 90 ps to 22 ps in measure mode 2	0 = off (GP2 compatibility) 1 = 0n
DOUBLE_RES	Reg6[12]	Improves resolution from 90 ps to 45 ps in measure mode 2	0 = off (GP2 compatibility) 1 = 0n

All details about the TDC-GP21 register architecture are available in chapter 3 of the datasheet.

Fire Pulse generator

With GP21 the maximum number of send pulses has been increased to 127. A detailed description of the fire pulse generator is available in TDC-GP21 datasheet section 5.2.1. Information about the correct configuration is described in section 5.2.2.

Table 4: New parameters for GP21 fire pulse generator

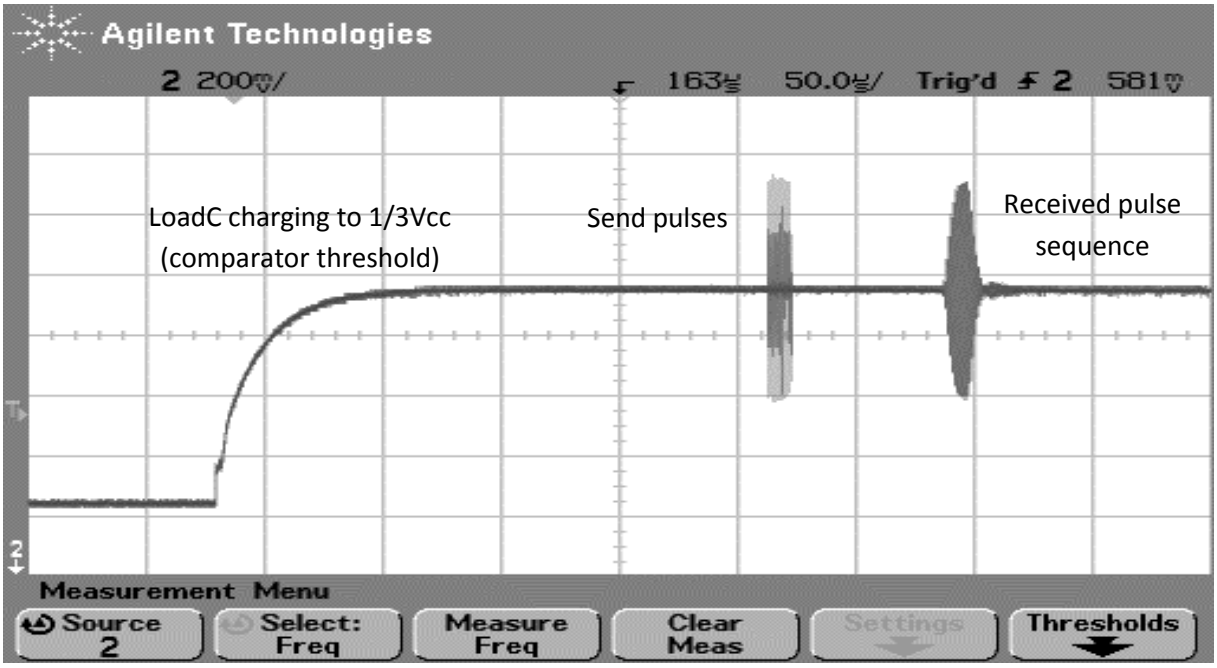
Parameter	Terminal	Description	Value
ANZ_FIRE	Reg0[31:28] Reg6[10:8]	Sets number of pulses	0 = off 127 = 127 pules
CONF_FIRE	Reg5[31:29]	Output configuration for pulse generator	Bit 23 = 1: Fire both Bit 22 = 1: disable Fire_Up Bit 21 = 1: disable Fire_Down
SEL_START_FIRE	Reg1[14]	Uses fire pulse signal as start	0 = GP2 behaviour 1 = use Fire as TDC start
FIRE_DEFAULT	Reg6[14]	Specifies default level of inactive fire buffer	0 = High-Z (GP2-Mode) 1 = Low (mandatory to use analog input section)

Analog input section

The TDC-GP21 integrates a complete analog section. It can be used alternatively to the pure digital input. This significantly simplifies the design of ultrasonic flow and heat meters, which is one of the main application areas of the TDC-GP21.

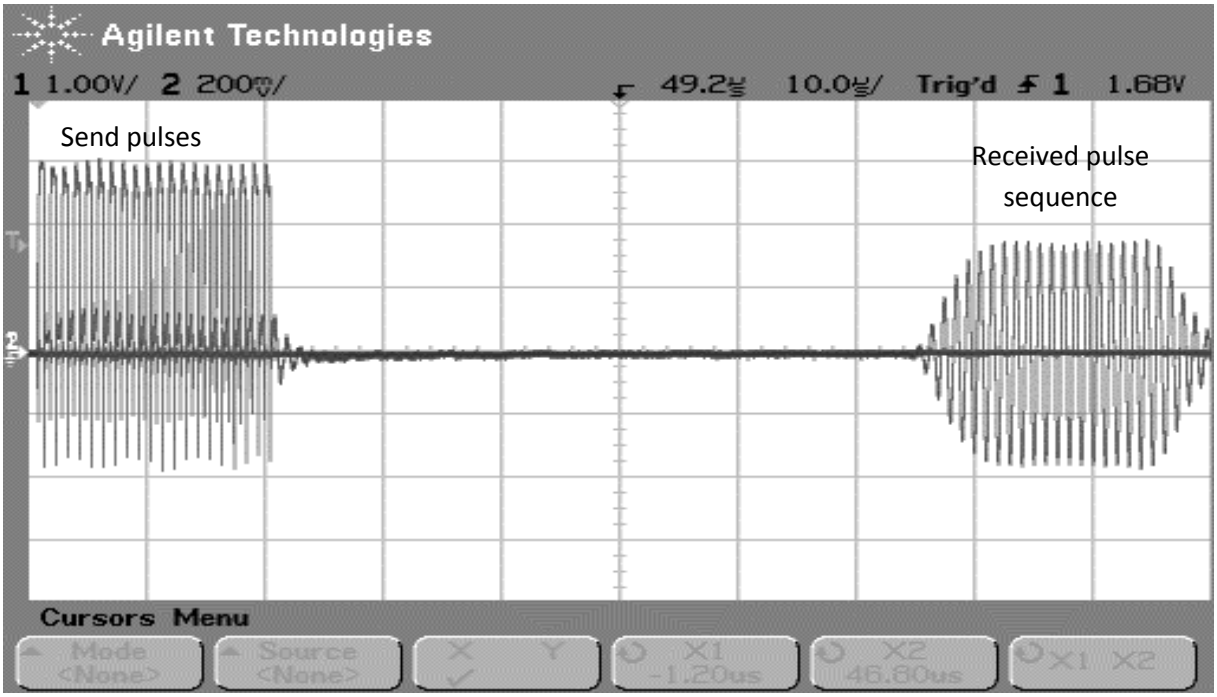
The signals are coupled to the TDC-GP2 analog inputs by means of a high pass filter. This is necessary as the comparator cannot handle GND as threshold. Thus, the input signal level of the non-inverted comparator input is switched to 1/3 Vcc. According to that the comparators threshold is also 1/3 Vcc. Figure 1 shows the corresponding oscilloscope trace.

Figure 1: Signal curve on non-inverted comparator input. (measured at TP1)



The GP21 integrates complete control for a measurement cycle. Figure 2 shows an oscilloscope trace of a measurement cycle with a 1 Mhz signal burst (20 pulses).

Figure 2: Oscillogram of a complete measurement cycle (measured at TP2 and TP3)



According to the received pulse sequence the integrated comparator generates a digital output signal that is internally feed into stop1 input. With SEL_TST1 = 6 (configuration register 6) the comparator output signal is available on FIRE_IN pin,(e. g. for hardware diagnosis) as shown below.

Figure 3: Received pulse sequence and corresponding comparator output signal

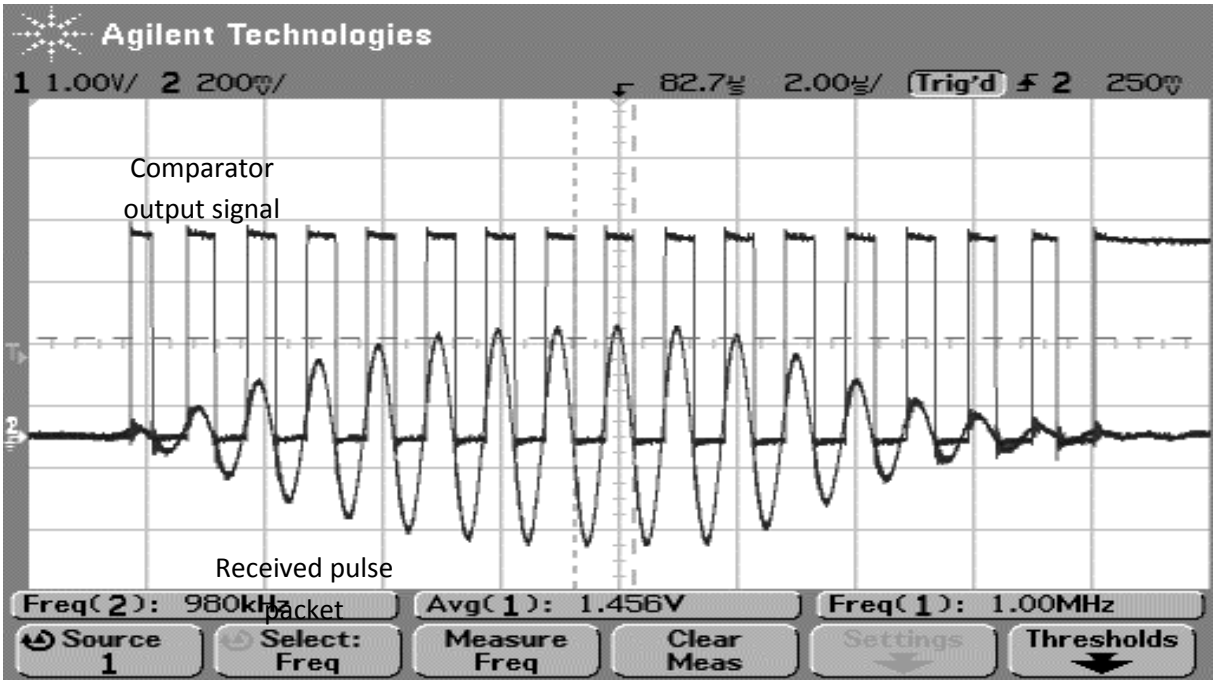


Table 6: Configuration parameters that are relevant for the GP21 analog section

Parameter	Terminal	Description	Value
EN_Analog	Reg6[31]	Activates analog part for ultrasonic flow measurements	0 = Stop1 and Stop2 are digital inputs (GP2 compatibility) 1 = activates analog section
TW2	Reg6[23:22]	Sets charge time of capacitor LoadC when the integrated analog section is used	0 = 90 µs 1 = 120 µs 2 = 150 µs 3 = 300 µs
CYCLE_TOF	Reg6[17:16]	Selects timer for triggering the second Time-of-Flight measuterment in multiples 56/69 Hz	0 = 1 1 = 1.5 2 = 2 3 = 2.5
HZ60	Reg6[15]	Forces GP21 to execute a complete up and down flow measurement cycle and two temperature measurement in series. The time interval between two measurements is based on 50 / 60 Hz	0 = 50 Hz base (20 ms) 1 = 60 Hz base (16.67 ms)

A detailed description of the analog section is available in section 4.3 of the TDC-GP21 datasheet.

Temperature measuring unit

The GP21 temperature measurement unit has the comparator already integrated. Due to GP2 compatibility it also works with an external Schmitt Trigger. Here we recommend the 74AHC14 to get

best results. The functional details are described in section 4.4 of the datasheet. The following table provides an overview of the relevant configuration parameters.

Table 8: Additional configuration Parameters for GP21 temperature measurement unit

Parameter	Terminal	Description	Value
NEG_STOP_TEMP	Reg6[30]	Inverts the SenseT input signal. Has to be set when internal Schmitt-trigger is uses trigger	0 = external Schmitt Trigger (GP2 compatibility) 1 = internal Schmitt-trigger
Cycle_TEMP	Reg6[19:18]	Selects timer for triggering the second temperature measurement in multiples of 50/60 Hz	0 = 1 1 = 1.5 2 = 2 3 = 2.5
TEMP_PORT_DIR	Reg6[11]	Option for measuring the temperature ports in the opposite order	0 = PT1>PT2>PT3>PT4 1 = PT4>PT3>PT2>PT1
HZ60	Reg6[15]	Sets base frequency for delay between up and down measurement	0 = 50 Hz base 1 = 60 Hz base

Configuration Register Architecture

The GP21 includes 7 configuration registers, each with 32-bit width (compared to 6 x 24 bit in GP2). The register organization is fully downwards compatible to GP2. To get access to the extended configuration space in order to use the enhanced GP2 functionality, the SPI communication has to be expanded by one additional byte of configuration data.

TDC-GP2: Opcode + Address + 3 Bytes configuration data

TDC-GP21: Opcode + Address + 4 Bytes configuration data

The complete register set is described in section 3 of the datasheet. Details about the SPI communication can be found in section 3.4.

Internal EEPROM

The TDC-GP21 integrates a 7x32 bit EEPROM, that can be used to store the configuration data together with a system ID or version number. For details please refer to section 3.3 of the datasheet.

Interrupt sources

The GP21 interrupt behavior is expanded by an additional interrupt source, that especially refers to EEPROM access. It has to be enabled by activating bit 21 in configuration registers 6. Then the end of an EEPROM action is indicated by an Interrupt.

Table 9: EEPRPOM action as interrupt source

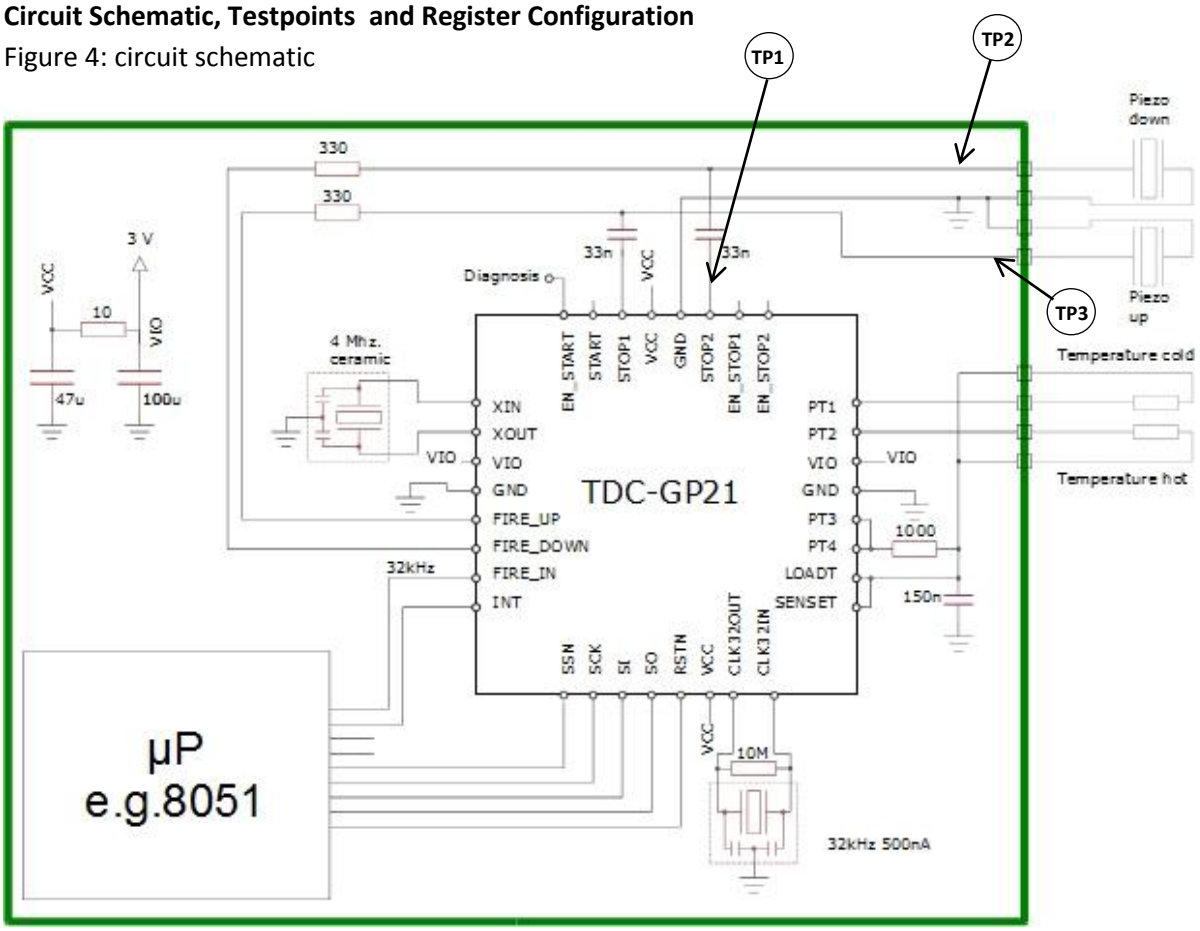
Parameter	Terminal	Description	Value
EN_INT[3]	Reg6[21]	Highest bit to enable additional EEPROM action as additional interrupt source. See also register 2 for lower 3 bits (GP2 compatible interrupt sources)	0 = disable EEPROM action as interrupt (GP2 compatibility) 1 = end of EEPROM action is indicates by an interrupt

Basic Reference Design

Test measurements were made with a GP21 hardware connected to a Weihai Ploumeter spoolspiece with 1 MHz transducers. TP1 to TP3 indicate the test points where the oscilloscope has been connected.

Circuit Schematic, Testpoints and Register Configuration

Figure 4: circuit schematic



The following register configuration has been used for the test measurement.

Table 10: Content of TDC-GP21 configuration registers

Configuration Register	Address	Register Content
Register 0	0	0xA30B6800
Register 1	1	0x21044000
Register 2	2	0x2024B800
Register 3	3	0x102A3000
Register 4	4	0x202AF855
Register 5	5	0x40000000
Register 6	6	0cC0006000

Related Documentation

acam-messelectronic gmbh -, “TDC-GP21 datasheet”