

## Customer Notification

November 2015

Our PICOPROG device is used as a general interface between PC and all our evaluation kits.

From today on PICOPROG V2.0 will be replaced by PICOPROG V3.0. The reason is that we want to support the UART capability of our new TDC-GP30 device.

V3.0 is fully downwards compatible to V2.0. In use there is no difference.

Following comparison points out the hardware differences between PICOPROG V2.0 and PICOPROG V3.0.

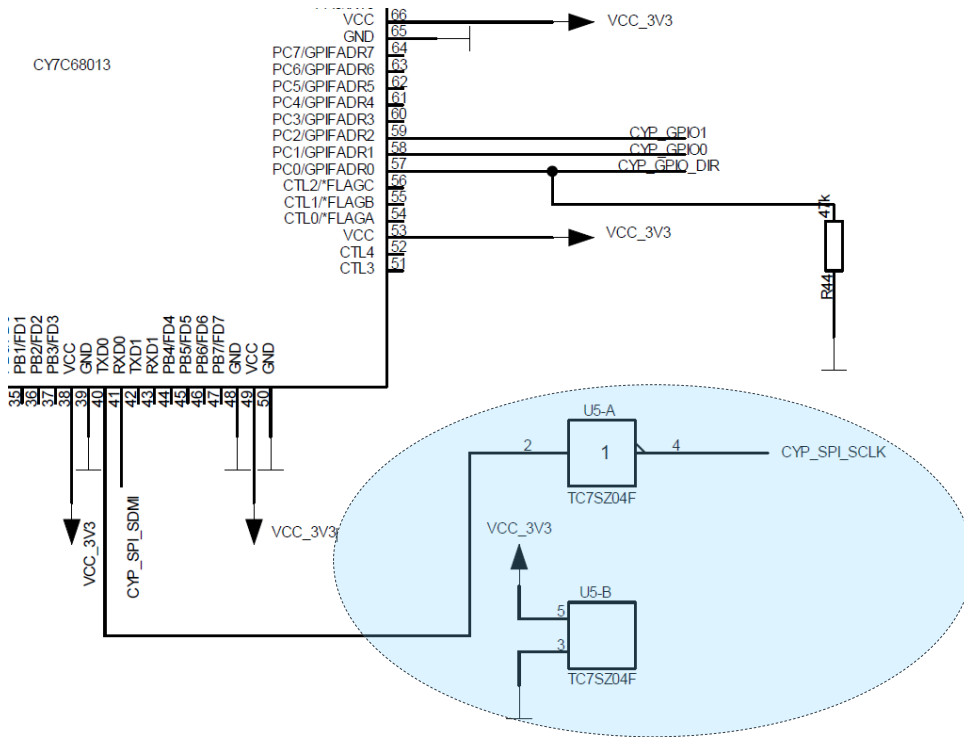
PICOPROG V2.0		PICOPROG V3.0	
Supported Communication Interface:		Supported Communication Interface:	
<ul style="list-style-type: none"> <li>- SPI</li> <li>- I2C</li> </ul>		<ul style="list-style-type: none"> <li>- SPI</li> <li>- I2C</li> <li>- <b>UART (additional for TDC-GP30)</b></li> </ul>	
Pin Description:	Pin Description:	Pin Description:	Used ports GP30-DEV-KIT
1 – IIC_SDA	1 – IIC_SDA	1 – IIC_SDA	
2 – SPI_ENABLE	2 – SPI_ENABLE	2 – SPI_ENABLE	
3 – GND	3 – GND	3 – GND	3 – GND
4 – PP_GPIO0	4 – PP_GPIO0	4 – PP_GPIO0	
5 – VCC_OTP	5 – VCC_OTP	5 – VCC_OTP	
6 – SPI_CSN	6 – SPI_CSN	6 – SPI_CSN	6 – SSN
7 – IIC_SCL	7 – IIC_SCL	7 – IIC_SCL	
8 – SPI_MISO	8 – SPI_MISO	8 – SPI_MISO	8 – MISO / <b>TXD</b>
9 – VCC_3V3	9 – VCC_3V3	9 – VCC_3V3	
10 – PP_GPIO1	10 – PP_GPIO1	10 – PP_GPIO1	
11 – SPI_MOSI	11 – SPI_MOSI	11 – SPI_MOSI	11 – MOSI
12 – SPI_SCLK	12 – SPI_SCLK	12 – SPI_SCLK	12 – SCK / <b>RXD</b>
13 – INT_GPIO_C1	13 – INT_GPIO_C1	13 – INT_GPIO_C1	13 – INTN
14 – VCC_LEVEL	14 – VCC_LEVEL	14 – VCC_LEVEL	14 – VCC_LEVEL
15 – VCC_5V	15 – VCC_5V	15 – VCC_5V	15 – VCC
Schematic Difference:		Schematic Difference:	
U13 – CY7C68013 / Pin 61 – unused		U13 – CY7C68013 / Pin 61 – UART	
U5 – TC7SZ04F (CMOS-Inverter)		U5 – SN74LVC1G86 (Exclusive-OR Gate)	
		R61 – 100k (additional PULL-UP resistor)	
By default CYPRESS µC applies HIGH at TXD0 (U13 – Pin 40). Therefore an inverter is used for the SPI clock to provide a LOW by default.		Now, an XOR gate provides either SPI clock or UART – RXD which is controlled by additional GPIO (U13 – Pin 61).	

**Schematics, differences only**

PICOPROG V2.0:

U5 – TC7SZ04F (CMOS-Inverter)

U13 – CY7C68013 / Pin 61 – unused



PICOPROG V3.0:

U5 – SN74LVC1G86 (Single 2-Input Exclusive-OR Gate)

U13 – CY7C68013 / Pin 61 – UART

