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PICOSTRAIN

Application Note

EMI Countermeasures for a Digital Load Cell

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1 Introduction

In May 2010 acam performed EMI[1] tests with Digital Load Cell (DLC) prototypes. The goal of the investigations were to prove immunity towards electromagnetical interference ("EMI immunity") for the DLC prototypes towards the OIML[2] specification. Thereby several EMI countermeasures were tried out to see which of them work best.

The results of these investigations are presented in this paper, including the recommendations of how to protect the circuit against EM interference.

Summed up in a single sentence it can be said that with relatively simple measures a good EMI behavior can be achieved, good enough to meet the requirements of legal specifications like OIML.

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[1] EMI = Electromagnetic Influence, Electromagnetic Interference

[2] OIML = Organisation Internationale de Métrologie Légale is an international organization which gives rules and guidelines for legal metrology. Please see www.oiml.org for more information.

[3] EMC = Electromagnetic Compatibility

[4] OIML R 76-1, Metrological and technical requirements of non-automatic weighing instruments, Edition 2006, downloadable at <http://www.oiml.org/publications/>, viewed on 17-June-2010.

2 Test Condition

The ability to resist against electromagnetic influences is an important point in building electronic units like the DLC nowadays. EMC[3] investigations are part of the certification process when it comes to legal for trade scales. For example, the OIML specification R76[4] states, that the fluctuations caused by EMI shall not exceed 1e. In other words, a 3000 divisions scale according to OIML must not show a variation of more than 1 division.

Please note:

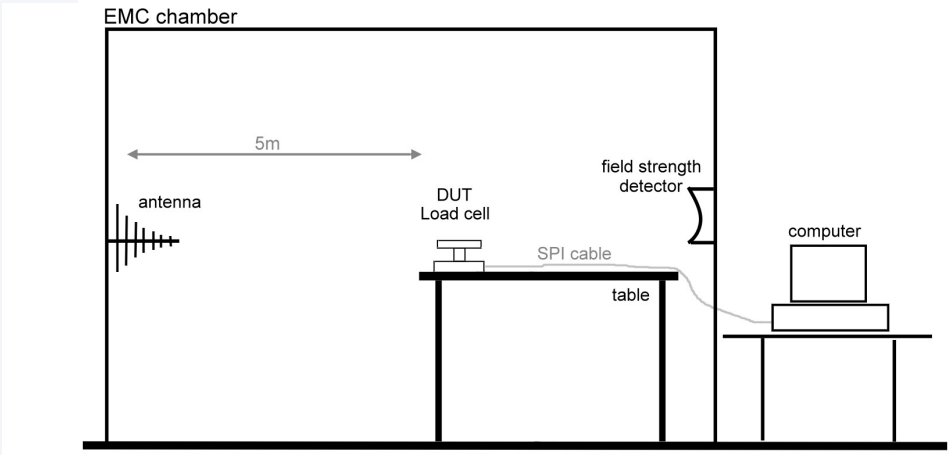
Unlike ESD tests, EMC investigations can only be applied to an electronic unit, not only to the chip itself. Therefore, the results gained from these investigations are only indicative and need to be investigated with the electronic unit in question individually.

The investigations were performed in a dedicated EMC test lab and according to EMC test specification and regulation and under supervision of an EMC expert. The Device under Test (DUT) was the Digital Load Cell prototype – a load cell mounted on a wooden carrier with the electronics embedded in the load cell. In that sense, the electronic board (PCB) was encapsulated in the body of the load cell. The connection to the 'outside world' consisted of a shielded SPI cable which transmits the data from the load cell to the computer outside of the chamber.

Edge conditions of the set-up:

- Electromagnetic radiation in the range from 80MHz to 2 GHz
- Applied field strength was 10V/m
- Horizontal and vertical polarisation of the radiation were tested
- EMI countermeasures taken as explained in the following

Figure: 1 Set-up in the EMC chamber



3 Countermeasures

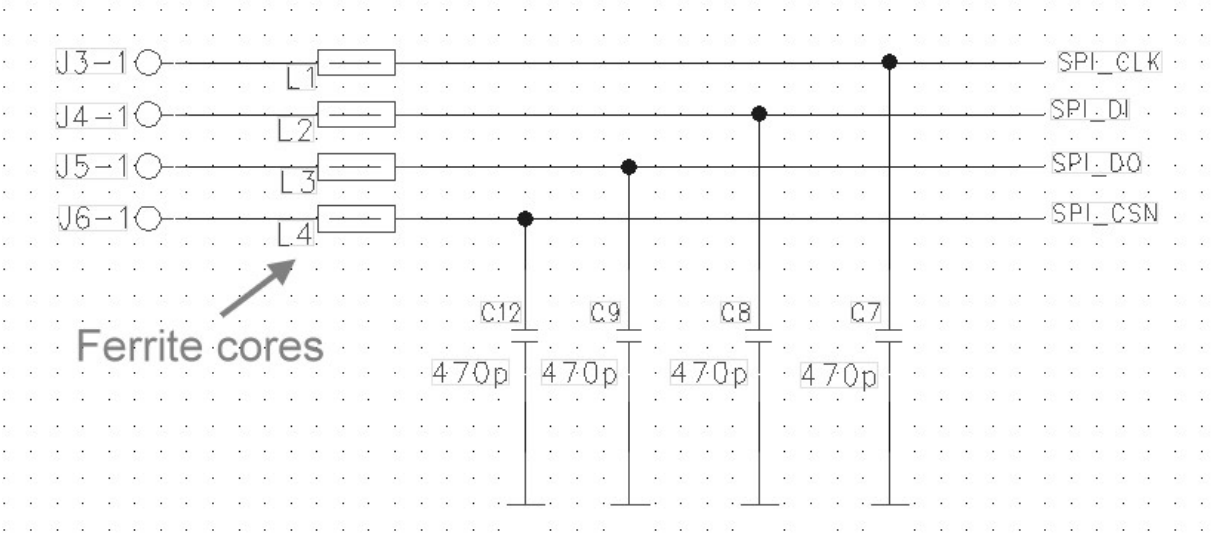
If an electronic unit is exposed to radiation, interference can occur due to electromagnetical effects, e.g. coupled-in into wires or the routes on a PCB. Typical countermeasures against these effects are to use ferrite cores or beads, blocking capacitors or ordinary resistors.

The protection of the PICOSTRAIN circuit is not an exception and can be protected the same way. As the measurement port lines and the interface lines are the “weak points” of the DUT and the countermeasures should be applied here. In the following we will demonstrate how the lines in consideration can be protected.

Protection of the SPI interface lines:

The easier of the two parts is the protection of the SPI interface lines. The lines SPI_DO, SPI_DI, SPI_CLK and SPI_CSN need to be protected by high impedance ferrites, such as 2.5kΩ @100MHz.

Fig. 2: Protection of SPI-interface lines



As shown in the picture, there is a ferrite core L1 to L4 directly in series with each of the SPI interface lines. Important here is to have a high resistance of the ferrite cores, e.g. 2.5kΩ (see appendix for sources). The second measure to protect the SPI-lines are capacitors towards ground, like indicated in the picture by C7, C8, C9 and C12. They should be in the range around 470pF and can be of X7R or COG/NPO material.

The protection of the SPI-interface lines in general is quite important as the tests showed major disturbances coming from the interface lines if unprotected.

3 Countermeasures

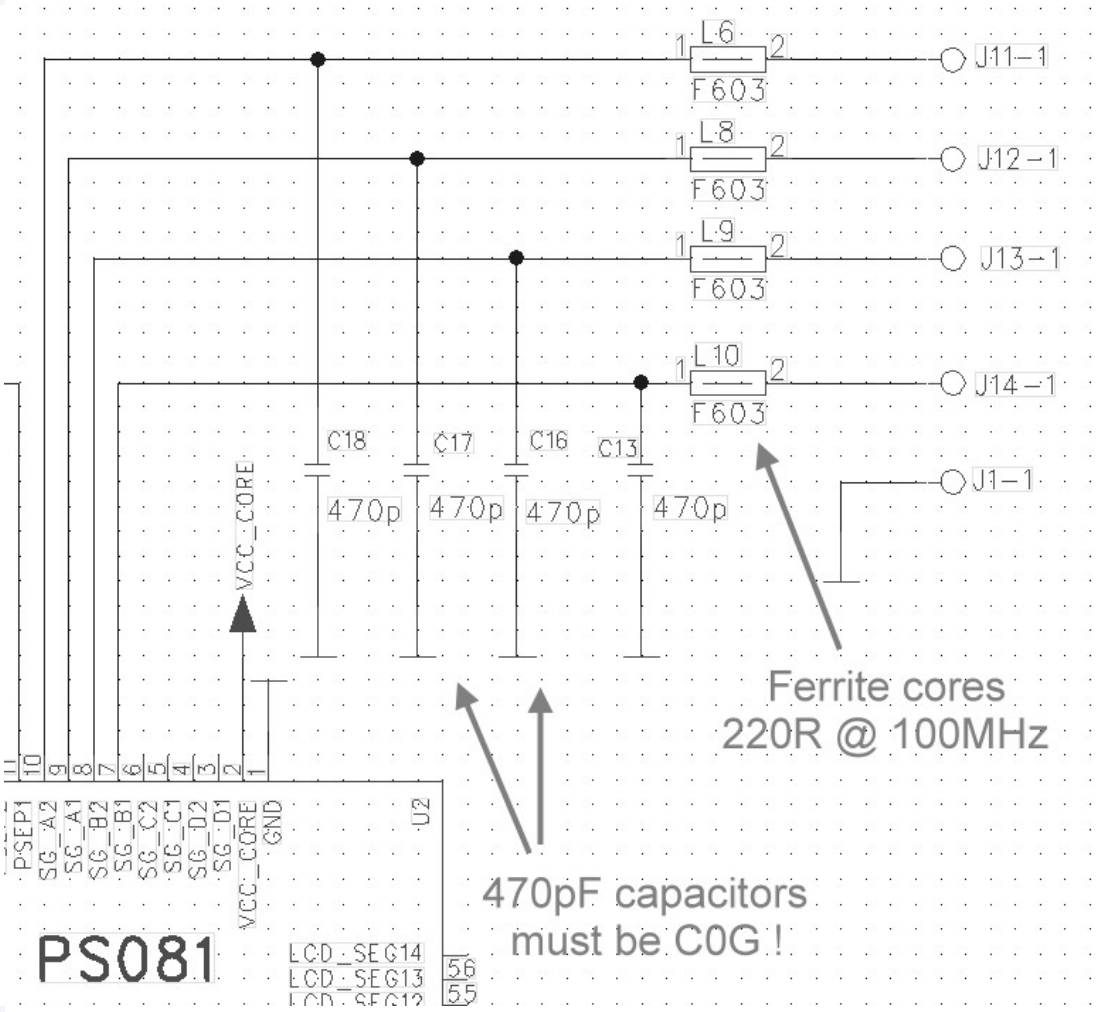
Protection of the measurement port lines:

To protect the measurement port lines, the countermeasures taken are almost the same as in the SPI-interface lines protection. However, here attention has to be paid to some more details. Depending on the level of EMI immunity that needs to be achieved there are two basic ways to protect the port lines:

- the optimal version achieves the best results but requires more components
- the minimal version allows for saving on some components but the level of EMI suppression is not quite as high.

The following pages will explain the two methods in detail.

Fig. 3: Protection of measurement port lines



3 Countermeasures

Optimal protection of the measurement port lines:

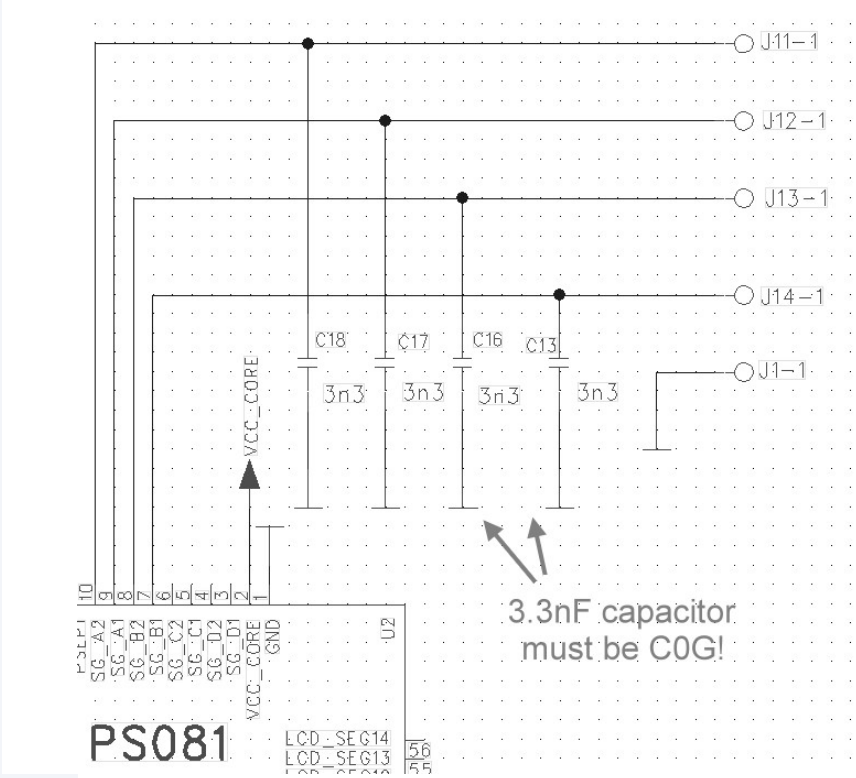
In this version the protection for the measurement port lines consists of ferrite cores and capacitors towards ground as well. But the ferrite cores need to have a lower resistance value, e.g. 220Ω @ 100MHz and most importantly their DC-resistance has to be as low as possible, preferably <=50mΩ. The value of to the capacitors remains the same with approximately 470pF, but in this case it is crucial that they are of C0G / NP0 material, e.g. Murata GRM1885C1H471JA01D or Kemet C0603C471J5GAC.

The version in figure 3 of the protection circuit shows best behavior as we will see in the diagrams later. However, there is a 'minimal version' which also showed good behavior – with this configuration the ferrite cores are left out and the protection consists only of the capacitors.

Minimal protection of the measurement port lines:

In this version of the protection circuit no ferrite cores are used. Instead the value of the capacitors is increased to 3.3nF, again C0G-types. The protection circuit looks like the following:

Fig. 4: Minimal protection of measurement port lines



As we will see later on in the recorded diagrams the minimal protection is not as good as the optimal one, but still shows good behavior and is sufficient for reaching an EMI immunity which is good for scales with 3000 divisions according to OIML specification.

4 Results

In the following we will present the results of the EMC tests – on the basis of the previously shown protection possibilities. During all tests the SPI interface lines were always protected by the same circuit and the results shown were achieved with the two different versions for the port lines, the optimal and minimal approach.

Each measurement is shown in two ways:

- with the relation to 1e out of 3000 divisions
- with the relation to the voltage of 3.3V and nominally 2mV/V, shown in µV/e

Optimal version:

Fig. 5: Optimal protection circuit, 80MHz to 2GHz, related to 1e out of 3000

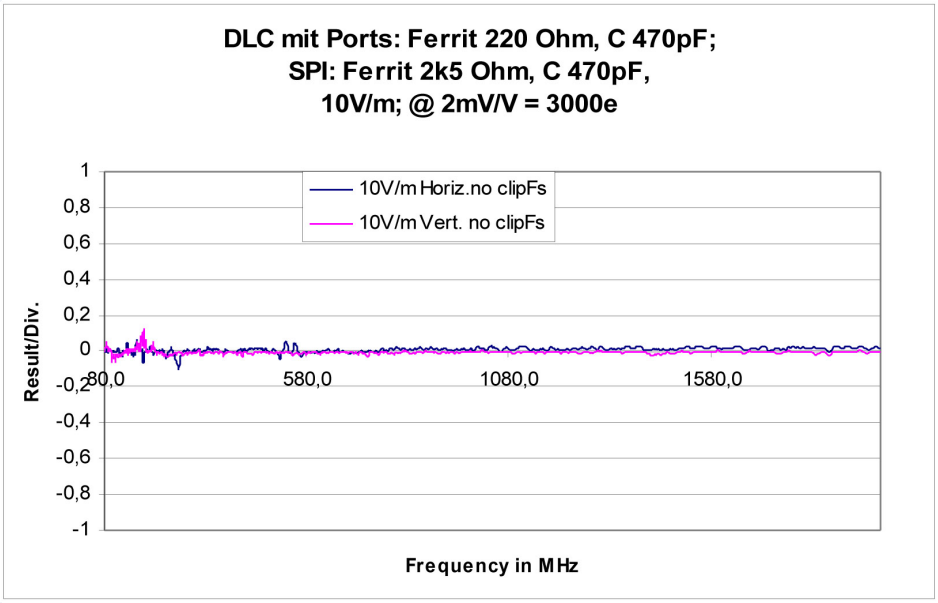
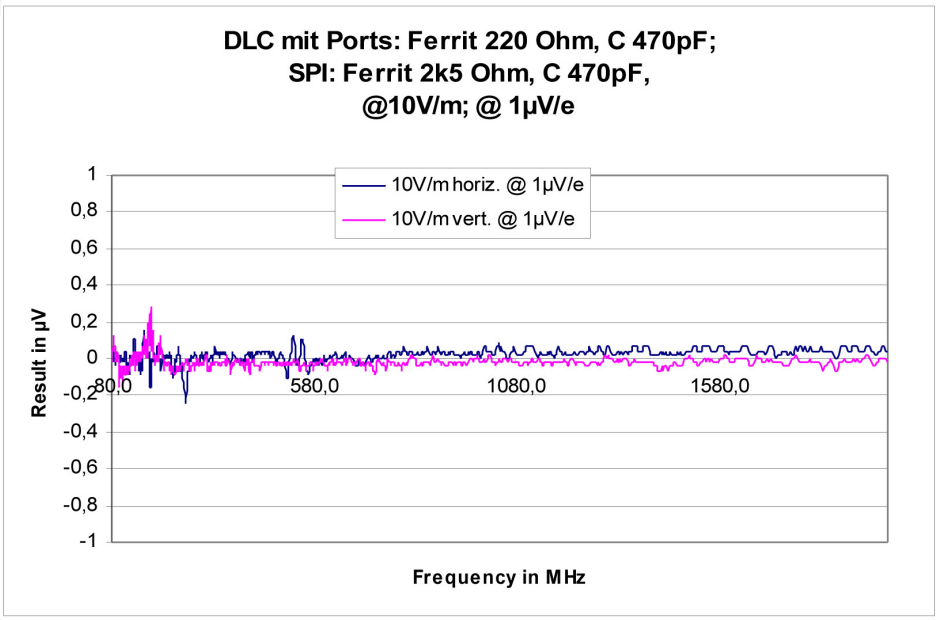


Fig. 6: Optimal protection circuit, 80MHz to 2GHz, shown in µV/e (@3.3V)



4 Results

Minimal version:

Fig. 7: Minimal protection circuit, 80MHz to 2GHz, related to 1e out of 3000

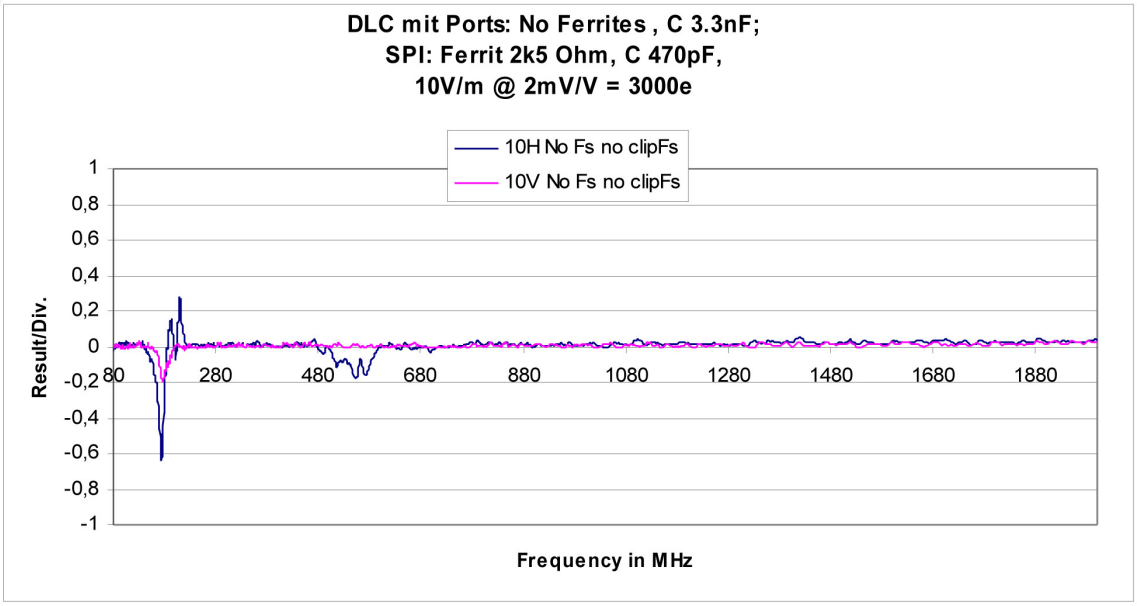
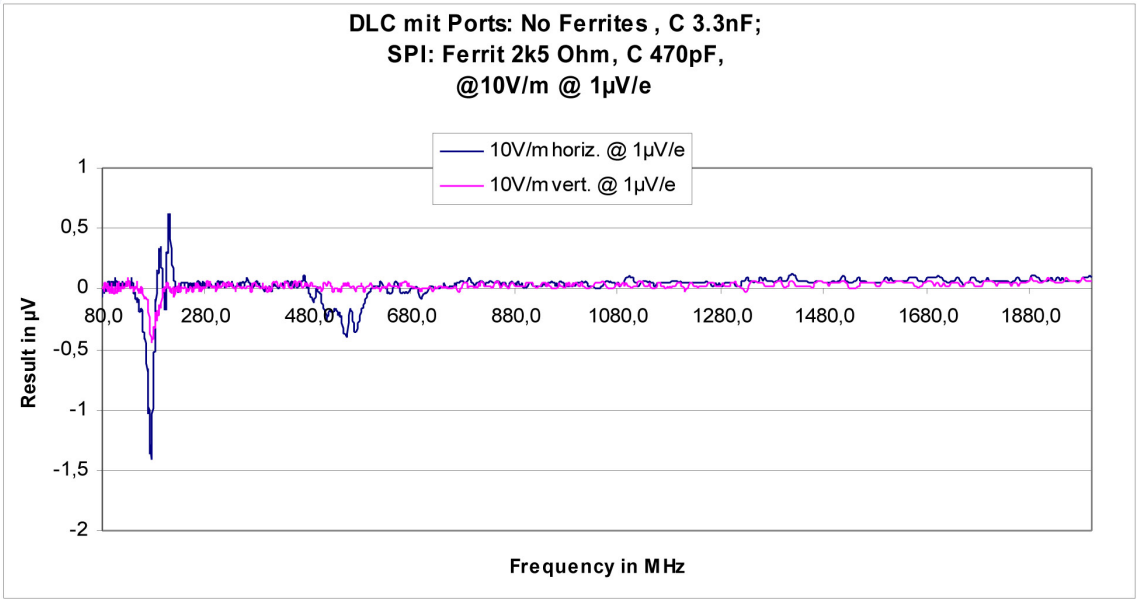


Fig. 8: Minimal protection circuit, 80MHz to 2GHz, shown in µV/e (@3.3V)

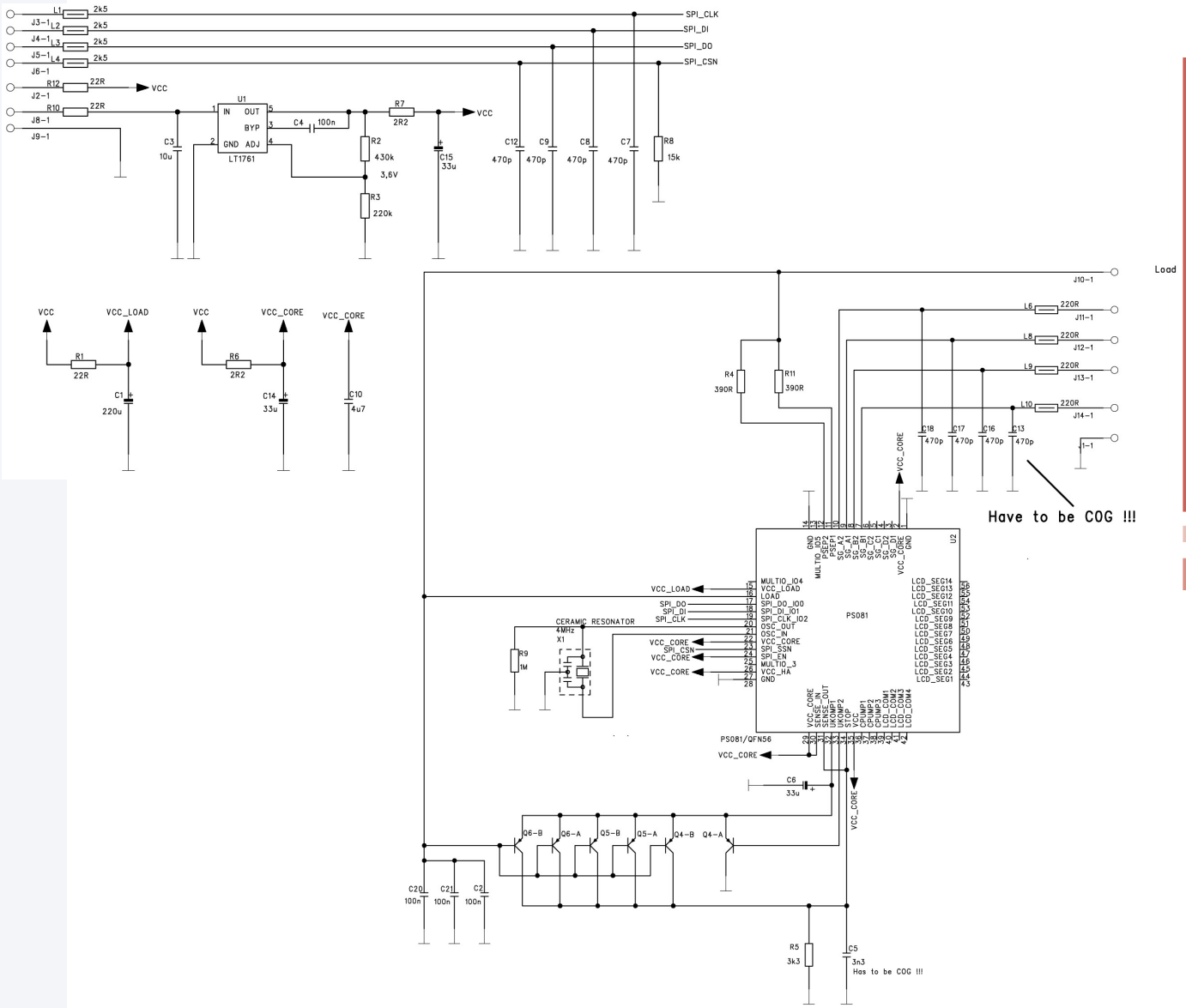


5 Conclusion

With relatively simple standard methods of protection a good EMI immunity can be achieved. When using the optimal protection circuit the EM influence is very low and deeply within 1e out of 3000, indeed the values are good enough to match (theoretically) the OIML specification of a 13200e (!) scale. Even with the minimal protection circuit the results are good enough to match the OIML specification of a 3000e scale.

6 Appendix

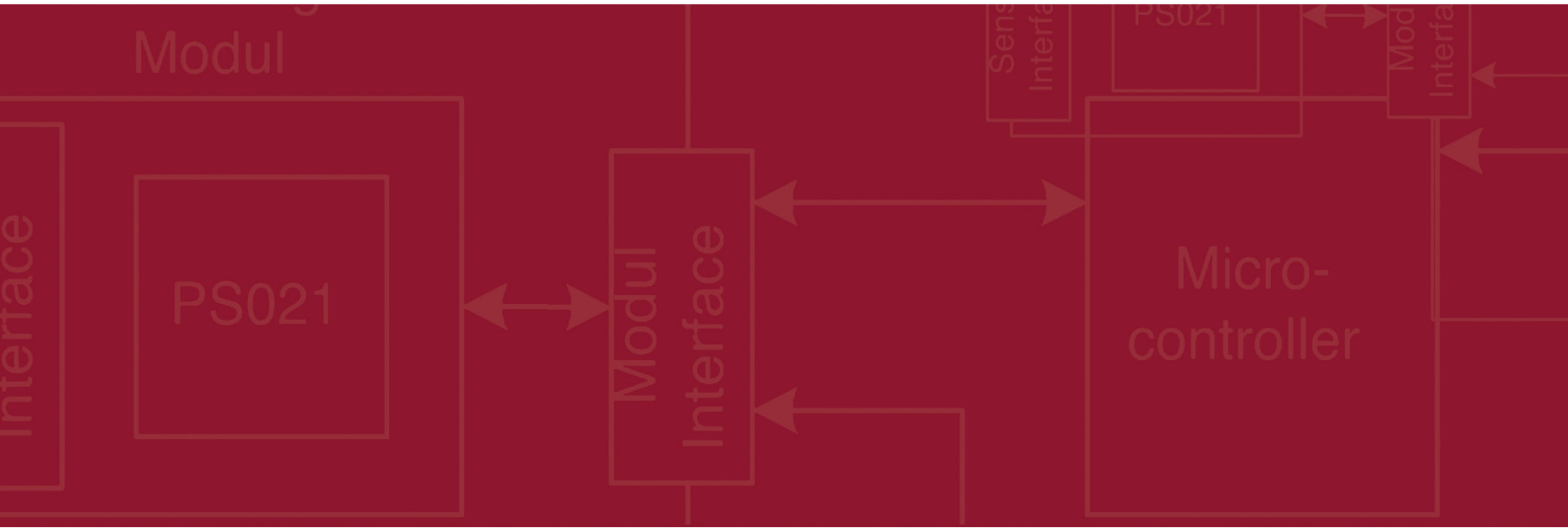
Fig. 9: Schematics of Digital Load Cell PCB with EMI protection circuit



Sources for Ferrite cores and COG/NPO capacitors:

Part:	Value:	Supplier / Part-No:	Distributor:	Part-No:
Capacitor	470pF	Murata GRM1885C1H471JA01D Kemet C0603C471J5GAC	e.g. Farnell	1118169
Ferrite core	220Ω @ 100MHz 0.04Ω DC res.	Murata BLM18SG221TN1	e.g. Farnell	1414640
Ferrite core	2.5kΩ @ 80MHz	Wuerth elektronik 742792695	e.g. Wu-erth	1515753

Note: The parts given in the table are only indicative. Most parts are available from a number of suppliers which are not all listed here.



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