

## MELPe

Mixed-Excitation Linear Predictive enhanced

### PRODUCT DESCRIPTION

Adaptive Digital's **enhanced-MELP (MELPe)** is a low bit rate vocoder supporting 2400, 1200 and 600 bps. It can operate at half the rate of the MELP standard.

**Enhancements include:** Improved encoding/decoding, transcoding between 2400, 1200 and 600 bps bit streams, and noise preprocessing for removing background noise.

MELPe provides better quality than all older military standards, especially in noisy environments such as battlefield, vehicles and aircraft. MELPe is suitable for use by OEM customers for VoIP, telecom, military; secure voice & radio, and other low bit-rate compressed speech applications.

### FEATURES

- Functions are C-callable.
- Multi-channel capable
- Optional noise preprocessing
- Transcodes between rates

### AVAILABILITY

ADT MELPe is available on the following Platforms: [Other configurations are available upon request.](#)

Platform
TI TMS320C674x
TI TMS320C64x, C64x+, C66x   TI TMS320C6416x
TI TMS320C55x
ARM Cortex A8 / A9 / A15
ARM Cortex-M4 / M7
ARM9e / ARM11
Win32 static lib
Linux i686

\* These Melpe libraries are available in 3 different Build configurations:

- Rate2400/Rate1200/Rate600 (all three) With Noise Pre-Processing (NPP)
- Rate2400/Rate1200 with NPP
- Rate2400 (only) with NPP

Endian, byte order: "Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

### Acronyms

Mm – Memory Model: Memory Model is specific to Texas Instruments processors.

N/A – Not Applicable

N/R – Not Recorded

## SPECIFICATIONS

Coding Rate: 600 bps, 1200 bps and 2400 bps

Sampling Rate: 8 kHz

**MELPe Frame Size**

The Melpe coder frame size is dependent on the Encode/Decode rate

Rate	Frame Size (Samples)	Frame Size (msec.)
600 bps	720	90 .0
1200 bps	540	67.5
2400 bps	180	22.5

**TI TMS320C6000****MELPe C64x+****MEMORY REQUIREMENTS**

Memory is given in units of bytes

C64x+ / C66x	Program	Channel	Scratch	Tables	Data
Encoder	191k	6560	6984	163k	70k
Decoder		1376			
NPP		11968			

**MELPe C64x****MEMORY REQUIREMENTS**

Memory is given in units of bytes

C64x	Program	Channel	Scratch	Tables	Data
Encoder	188.4k	6560	5672	148k	63k
Decoder		1376			
NPP		11968			

**MELPe C64x+ / C66x / C674 OMAP (Cache Enabled)****CPU UTILIZATION**

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS (C674 OMAP) Cache Enabled and C64x+	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	11.4	11.5	13.7
Encoder	23.4	23.5	24.8
Decoder	15.1	15.1	17.4
Total	49.9	50.1	55.9

**MELPe C6416****CPU UTILIZATION**

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS (C6416)	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	12.2	12.2	13.3
Encoder	23.7	27.5	23.4
Decoder	15.7	22.5	17.9
51.6	42.6	62.2	54.6

## TI TMS320C5000

### MELPe C55x

#### MEMORY REQUIREMENTS

Memory is given in units of bytes

C55x	Program	Channel	Scratch	Tables	Data
Encoder	78.3k	6560	6984	162k	5k
Decoder		1600			
NPP		11968			

### MELPe C55x

#### CPU UTILIZATION

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS (C55x)	MIPS (600bps)		MIPS (1200 bps)		MIPS (2400 bps)	
	Max	Avg	Max	Avg	Max	Avg
Nonlinear Preprocessor (NPP)	19.6	18.7	20.0	19.0	21.8	20.5
Encoder	34.2	32.5	46.5	41.3	29.7	26.6
Decoder	12.7	10.7	14.4	11.2	14.8	13.3
Total	66.5	61.9	80.9	71.5	66.3	60.4

## ARM® DEVICES

### MELPe ARM Cortex-A8 / A9 / A15

#### CPU UTILIZATION

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS Cortex-A8/A9/A15	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	14	14	14
Encoder	46	44	27
Decoder	17	17	17
Total			

### MELPe ARM Cortex-M4 / M7

#### CPU UTILIZATION

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS ARM9e	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	< 30	< 30	< 30
Encoder	< 60	< 50	< 50
Decoder	< 30	< 30	< 25
Total	< 120	< 110	< 105

**MELPe ARM Cortex-M4 / M7****Memory Requirements**

All Memory usage is given in units of byte.

Cortex-M4	Program	Channel	Scratch	Table	Data
Encoder	100 K	6560	6984	148 K	63 K
Decoder		1376			
NPP		11968			

**MELPe ARM9e****CPU UTILIZATION**

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS ARM9e	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	35	35	35
Encoder	493	489	81
Decoder	27	27	27
Total			

**Linux****MELPe i686****CPU UTILIZATION**

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	78	78	78
Encoder	214	238	207
Decoder	71	71	71
Total			

**Windows****MELPe Win32****CPU UTILIZATION**

All CPU usage given in MIPS (also known as MCPS or MHz)

MIPS	MIPS (600bps)	MIPS (1200 bps)	MIPS (2400 bps)
Nonlinear Preprocessor (NPP)	84	83	85
Encoder	250	279	237
Decoder	70	68	72
Total			

**FUNCTIONS**

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*API function call summary*

MELP_ADT_initEnc	Initializes an Encode Channel
MELP_ADT_initDec	Initializes an Decode Channel
MELP_ADT_encode	Encodes a frame of data
MELP_ADT_decode	Decodes a frame of data

### *Deliverables*

The deliverable items are platform dependent. In general, there is one library. (Sometimes multiple variants of the library are included in the deliverables.) There are also header files, some of which are specific to the product and others are common across many of Adaptive Digital's products. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes and a data sheet. Sample/test code may be included as well.

*Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.*

### CONTACT INFORMATION

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