Software Echo Canceller Integration – Handling Bulk Delay

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Issue 1

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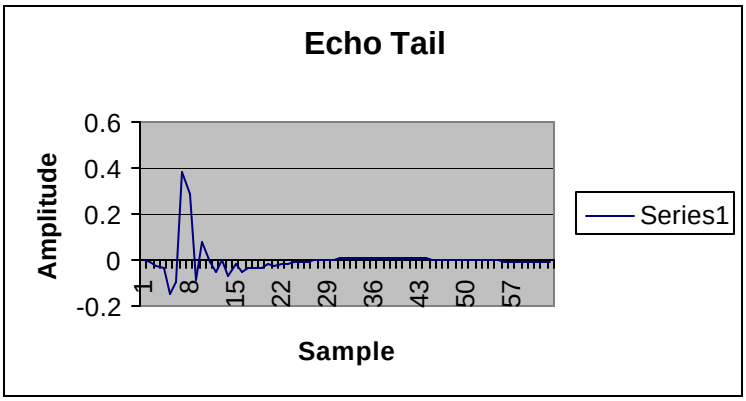
Revision History

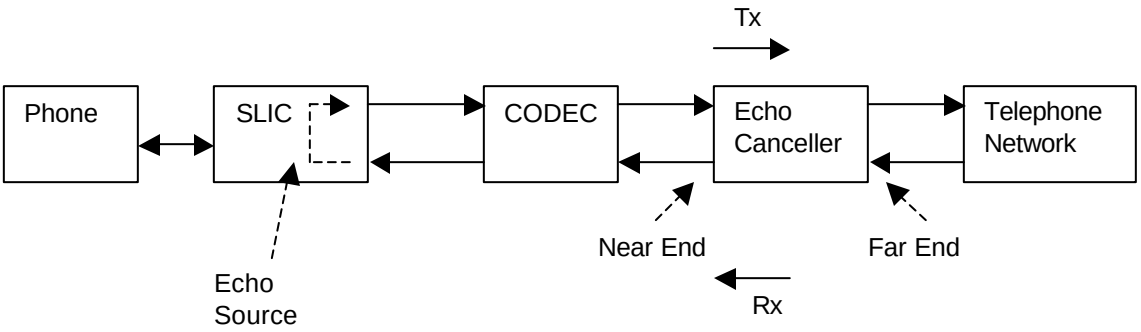
Issue	Revision History	Date	Initials
1	Creation	10/27/2000	SDK

Integrating an echo canceller into a packet based or frame based system requires special timing considerations. A realistic source of electrical echo in a telephone system exhibits diffusion. By this I mean that the impulse response of the echo source (the echo tail) is not an impulse. The amplitude of the echo tail is non-zero for a period of time known as the tail length. This is shown in the following graph.

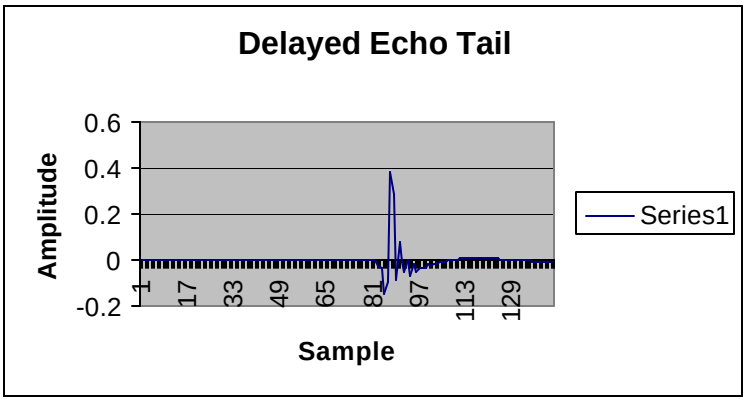


In this example, the tail length is approximately 60 samples in duration. This corresponds to approximately 8 milliseconds at a sampling rate of 8000 samples per second.

The following block diagram shows the use of an echo canceller in a typical system.



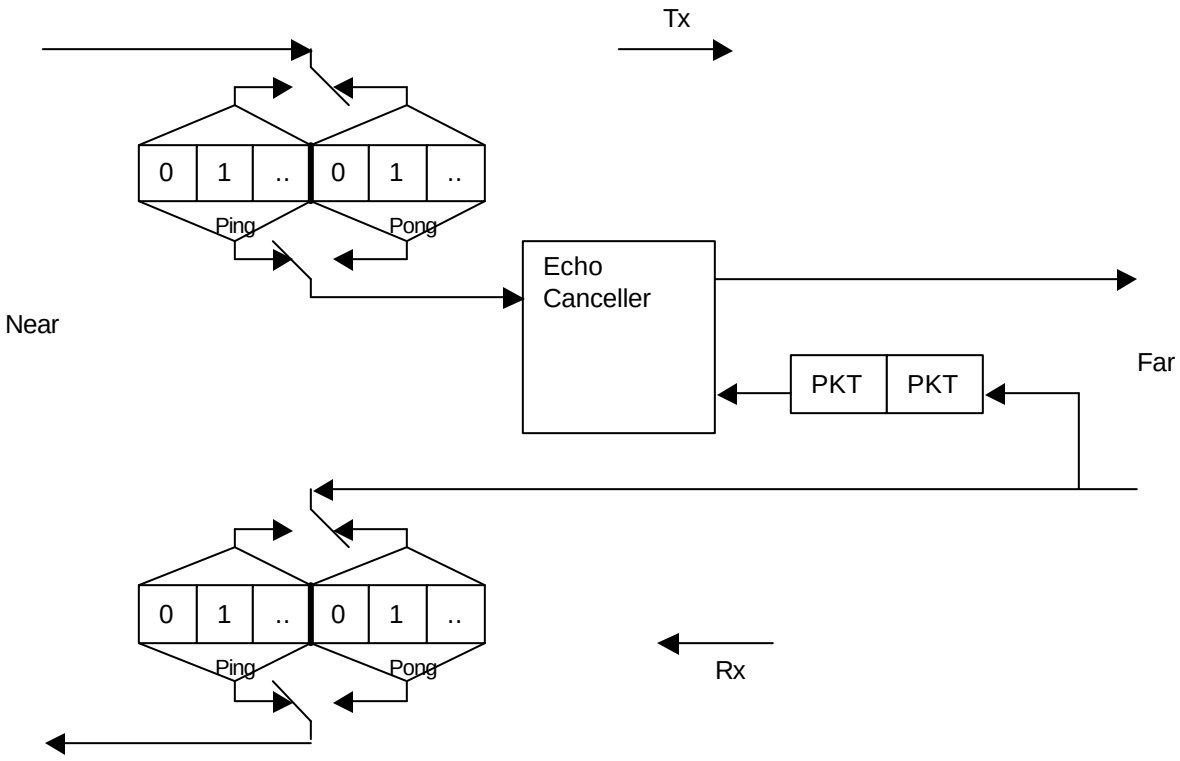
In a packet or frame based system, there is a buffering delay inserted between the echo canceller and the echo source. This buffering delay is usually approximately twice the packet size in duration. The cause of this buffering delay will be discussed later. From the point of view of the echo canceller, this buffering delay causes the echo tail to be shifted as shown in the graph below. In this example, the buffering delay is approximately 90 samples in duration.



If the echo canceller were not somehow compensated for the fixed (bulk) delay, the echo canceller would be required to attempt to cancel the additional 90 samples even though no echo component can be present.

The compensation is rather simple. Each time the echo canceller is called, it is presented with a frame (packet) of near end and far end samples. To compensate for the bulk delay, the far end input is delayed by the bulk delay duration before being fed into the echo canceller. This effectively removes the bulk delay from the point of view of the echo canceller.

The diagram below shows how the data flows through the system. The diagram shows both the cause of the bulk delay and the compensation technique.



A ping-pong buffering scheme is used between the echo canceller and the near end. The ping-pong buffering scheme is a software mechanism that allows the DSP input / output device (the serial port) to read/write from/to ping buffer while the echo canceller is writing/reading to/from the pong buffer. When a frame is complete, the serial port and echo canceller swap usage of the ping and pong buffers. This ensures that there is no contention between buffers and therefore no corruption of data.

The ping-pong buffering results in an additional delay equal to the size of the ping or pong buffer. These buffers are each the size of a packet or frame. The ping-pong buffering therefore results in two additional frames of bulk delay. One frame in the receive direction and one frame in the transmit direction.

The compensation for this delay is shown between the far end and the echo canceller. There are two packet buffers in a delay-line fashion. This results in a two frame delay of the inbound far end signal into the echo canceller.