VoIP Aggregator – C6472

VoLTE Aggregator

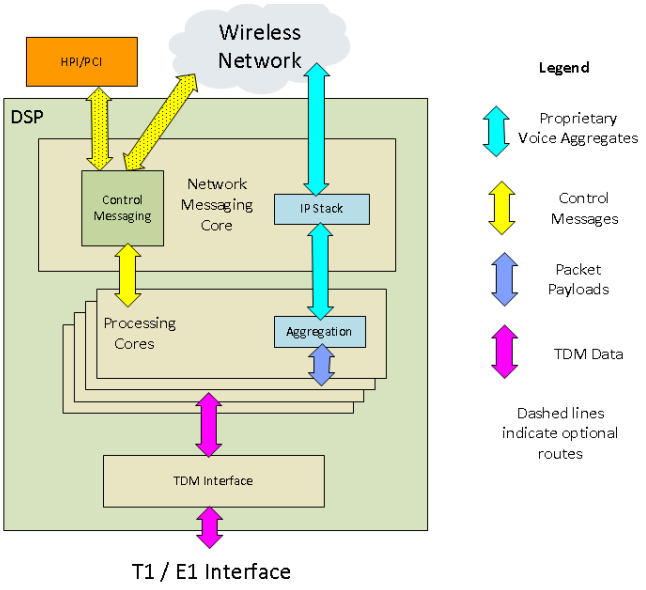
TARGET APPLICATIONS

LTE Wireless Networks

VoIP Transcoding

OVERVIEW

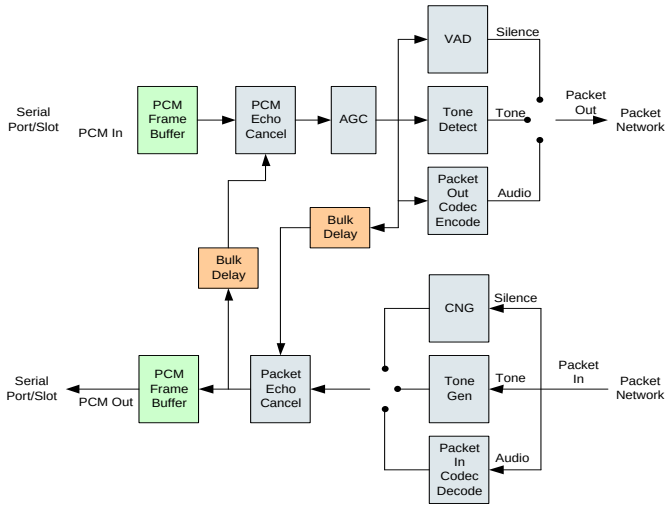
Adaptive Digital's High Density Gateway product combines Adaptive Digital's G.PAK DSP software plus host APIs along with Texas Instruments' C6472 DSP for use in wireless VoIP LTE network equipment. This product provides the functionality necessary to bridge traditional analog telephone lines and digital trunks to a digital Voice over IP Network.



Chip Block diagram

SOFTWARE FEATURES

- Voice Transcoding
- AGC
- DTMF
- Tone generation
- VAD
- Network Stack
- T.38 Fax Relay
- Codecs
  - G.711
  - G.722.1
  - G.723.1
  - G.726
  - G.729AB



Software Block diagram

Optional Software Features

- Echo cancellation

HARDWARE FEATURES

- 6 On-Chip DSP Cores @ 500/625/700 MHz
- 32 KB L1 Program Cache
- 32 KB L1 Data Cache
- 608 KB L2 Memory
- MII, RMII, GMII and RGMII EMAC
- 16-Bit HPI (Host Port Interface)
- 3 TSIP TDM Buses
- Up to 256 MB External Memory

ADDITIONAL HARDWARE FEATURES

- EDMA Controller
- 2 Serial Rapid IO Links
- I^2C Bus
- 16 GPIO Pins

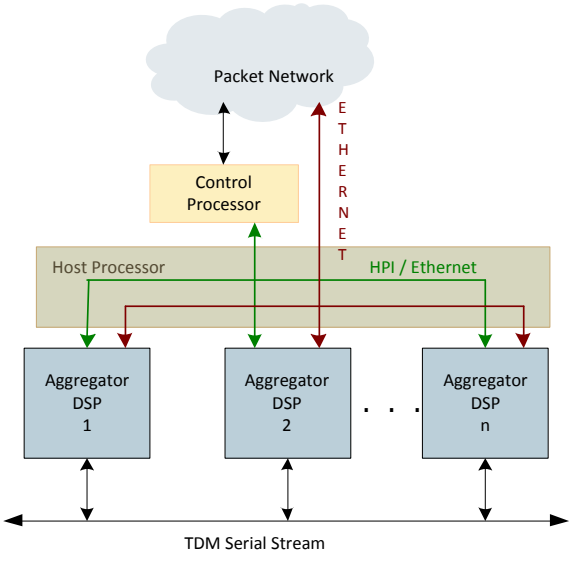
SPECIFICATIONS

Product Number/Silicon	Channel Count	Description
TMS320C6472 / 700 MHz with 128 MB DDR2 @ 533 MHz	128 G.711	G.711 with VAD, T.38 and DTMF detection.
	128 G.722.1	G.722.1 with VAD, T.38, and DTMF detection.
	128 G.723.1	G.723 with VAD, T.38, and DTMF detection.
	128 G.726	G.726 with VAD, T.38, and DTMF detection.
	128 G.729 AB	G.729 A/B with T.38 and DTMF detection.

DETAILED DESCRIPTION

A VoIP aggregator provides performance increases in wireless LTE VoIP networks. The VoIP aggregator reduces packet overhead by multiplexing voice packets from parallel VoIP connections into a single packet for transmission. By performing functions such as voice and fax compression, decompression, and packetization. A VoIP aggregator enables the data infrastructure to significantly reduce the bandwidth required for voice and fax over wireless applications.

Figure (2) shows a block diagram for a typical VoIP aggregator. A VoIP aggregator usually consists of a host control processor connected to one or more VA-LTE C6472 chips. The host processor typically controls the VA-LTE C6472 via either the host port interface or via Ethernet. The voice packets can be routed between the network and the VA-LTE



C6472 chip via the control processor. Alternatively, the IP aggregator chip can be connected directly to the network via the Ethernet interface. The VA-LTE C6472 chip connects to the TDM interface via the chip's TDM serial port.

The major components in a VoIP aggregator chip include vocoders, voice quality enhancement algorithms, and telephony algorithms. The VoIP aggregator chip supports TDM to Packet and Packet to Packet channel types. Channel setup (identification of input and output ports, vocoders, and voice algorithms), conference setup, and teardown operations are controlled by the host processor using a set of VoIP aggregator API functions

Channel Types

The VoIP aggregator C6472 provides only the TDM to Packet and Packet to Packet channels as standard. TDM to TDM channel types are available as an option.

A TDM channel is typically associated with one of the following types of telephone interfaces:

- FXO
- FXS
- T1/E1 time slot (DS0)

Each channel in a DSP is dynamically setup as any type. Frame sizes, vocoder types, and tone detection types are selected when a channel is setup.

All are designed to operate as full duplex channels. A full duplex channel may be configured to operate as a half duplex by setting the end points of one-half of the full duplex channel to NULL end-points.

HOST API

The VA-LTE C6472 APIs are the interface between a user's application program and [IPG-C6472] DSP cores. The APIs execute in a host control processor connected to the DSP via either Ethernet or the DSP's Host Port Interface (HPI). The APIs support multiple DSP cores/chips and use a DSP Identifier to select a particular core. The association between a DSP Identifier and a particular DSP core/chip is made by the user modified [IPG-C6472] driver support functions.

The APIs are provided as ANSI "C" source code. The APIs will work with any host application regardless of the operating system being used.

REFERENCES

1. Adaptive Digital Technologies VA-LTE C6424 Users Guide
2. Texas Instruments TMS320C647 Fixed-Point Digital Signal Processor (literature number SPRS612G.)

Deliverables

The deliverable items are platform dependent. In general, there is a single DSP-downloadable binary image along with host API software in C source code format. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes. Sample/test code may be included as well.

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

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