Acoustic Echo Canceller G2

Narrowband

PRODUCT DESCRIPTION

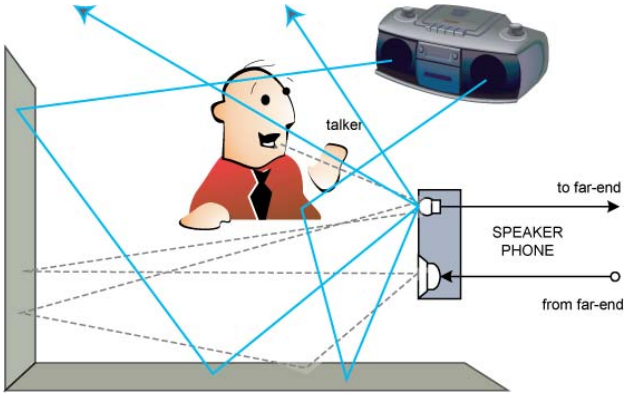
Acoustic Echo is caused by direct and indirect feedback from speaker to microphone.

The Adaptive Digital Technologies patented acoustic echo canceller, electronically removes both direct coupling and reflected echo, enabling true full-duplex hands-free telephony for both mobile phones and desktop speakerphones.

Adaptive Digital's fielded, second generation AEC handles undesirable acoustic echo in both iPhone and Android based Mobile Digital Devices/Handsets.

FEATURES

- Available on Texas Instruments 'C6000, 'C5000, ARM, and x86 platforms
- Cancels acoustic echo caused by speaker to microphone feedback
- Designed for both traditional speakerphones and mobile handsets.
- Prevents howling
- Adapts quickly to changing echo characteristics
- Nonlinear processor
- Comfort Noise Generation
- Noise Suppression
- 8 kHz sampling rate
- Can achieve greater than 35 dB of echo return loss enhancement (ERLE) without Nonlinear Processor
- Supports echo tail length up to 128 msec



AVAILABILITY

ADT AEC G2 is available on the following Platforms: Other configurations are available upon request.

Product	Platform	Memory Model	Endian	Code Gen Tool Version
ADT_aec_c64x	TI TMS320C64x	L3	Little	6.1.15
ADT_aec_arm11	ARM11	N/A	Little	N/R
ADT_aec_arm9	ARM9	N/A	Little	N/R
ADT_aec_armM3	ARM Cortex-M3	N/A	Little	GCC v 4.6.1
ADT_aec_armM4	ARM Cortex-M4	N/A	Little	GCC v 4.6.1
ADT_aec_armA8	ARM Cortex-A8	N/A	Little	GCC v 4.6.1
ADT_aec_armA9	ARM Cortex-A9	N/A	Little	GCC v 4.6.1
ADT_aec_armA15	ARM Cortex-A15	N/A	Little	GCC v 4.6.1

Endian, byte order: "Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.
Acronyms

Mm – Memory Model: Memory Model is specific to Texas Instruments processors.

SPECIFICATIONS

TI TMS320

C64X

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Tail Length	MIPS(Peak)	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
18 msec	65.2	51808	4783	4485	1221

ARM® DEVICES

ARM-9 / ARM-11

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Tail Length	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
18 msec	58.9	59276	4238	4485	1221

Cortex-A8/A9/A15

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Tail Length	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
18 msec	62.4	58240	4238	4485	1221

Cortex-M3/M4

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Tail Length	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
6 msec	39.9	42676	4238	3873	837

FUNCTIONS

AEC_ADT_aecInit(…)	Initializes echo canceller channel
AEC_ADT_aecCancel(…)	Executes cancellation function

Deliverables

The deliverable items are platform dependent. In general, there is one library. (Sometimes multiple variants of the library are included in the deliverables.) There are also header files, some of which are specific to the product and others are common across many of Adaptive Digital's products. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes and a data sheet. Sample/test code may be included as well.

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

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