

VoIP TRANSCODING CHIP

Transcoding is the direct digital-to-digital conversion of one encoding to another.

1 HARDWARE FEATURES

- High-Performance
 - 400-/500-/600-/700-MHz, C64x+™Clock Rate
 - Eight 32-Bit C64x+[™] Instructions/Cycle
 - 2.5-, 2-, 1.67-, 1.43-ns Instruction Cycle Time
 - 3200, 4000, 4800, 5600 MIPS
- 16-Bit Host-Port Interface (HPI)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- C64x+ L1/L2 Memory Architecture

2 SOFTWARE FEATURES

- Voice transcoding (packet to packet)
- Field proven algorithms: G.729 AB, G.723.1, G.711 A1A2, G.726, G.728, GSM AMR, MELP G.722, G.722.1, G.722.2

- Two Multichannel Buffered Serial Ports
- 10/100 Mb/s Ethernet MAC (EMAC)
- Multichannel Audio Serial Port (McASP0)
- IEEE-1149.1 (JTAG[™]) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
 Up to 111 General-Purpose I/O (GPIO) Pins
- Port count: 64
- 3.3-V and 1.8-V I/O, 1.2-V Internal
 3.3-V and 1.8-V I/O, 1.05-V Internal
- Supports Tone Relay
- Scalable
- The encoders and decoders meet all ITU/ETSI compliance and interoperability requirements

3 DEVICE OVERVIEW

Supporting multiple codecs is one of the most challenging aspects effecting VoIP services across telephone, cable, cellular, Wi-Fi, and Internet networks. As VoIP networks, usage, and applications expand, the need to translate traffic from one codec type to another becomes more and more important to ensure global connectivity.

Codec transcoding provides a means to convert traffic so that two VoIP networks using different codecs can exchange traffic without making codec format changes on their individual network devices. Transcoding efficiently and effectively interconnects traffic thereby allowing each provider's network to use its codec of choice.



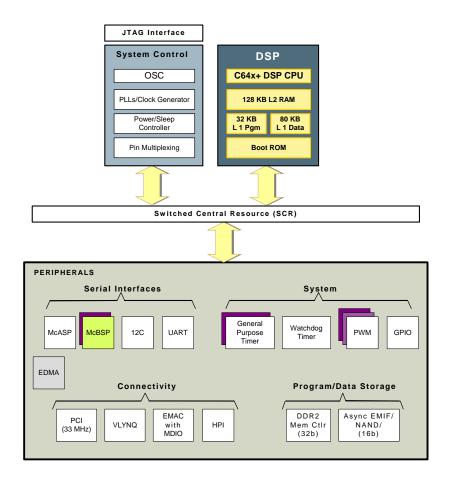


Figure 1: TMS320C6424 Functional Block Diagram

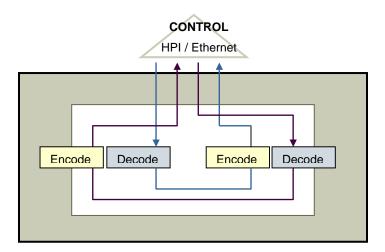


Figure 2: Transcoding chip Block Diagram

4.1 Channel Type

Packet to Packet Channel Type

The Packet to packet channel type provides a linkage between packet channels. Packet to packet channels are typically used in gateway applications to perform frame size conversions, codec type conversions (transcoding), and/or echo cancellation of packet data. This type of channel can also be used to convert silence and tone packets to audio packets or to convert audio packets to silence and tone packets. Channels of this type have two threads of processing as shown in figure 3. Each VIP-P packet to packet channel is half duplex; however, these channels are always allocated in pairs (channels A and B) to allow full duplex operation.

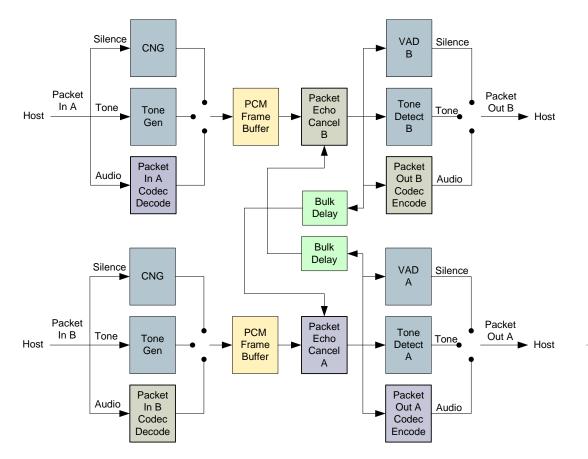


Figure 3- Packet to Packet Channel

Packet decode processing. The packet decoding thread reads a channel 's packet from the host control processor and generates and buffers 8 KHz samples according to the received packet type. If a silence packet is received, comfort noise is generated. If a tone packet is received, the specified tone is generated. If an audio packet is received, it is decoded according to the input packet codec type. The generated PCM samples are buffered for encoding by the paired channel.

Packet encode processing. When enough of the paired channel's PCM samples are buffered to build an output frame, this PCM data is optionally passed through the packet echo canceller, the tone detector (TD) and the voice activity detector (VAD).

Tone detection is optionally performed on the PCM data after the G.168 echo cancellation ¹ but prior to the non-linear post-processing of the echo canceller. XCD notifies the host at the start and end of each tone. If tone relay is enabled, tone packets are generated for each frame until the tone ends; an end of tone packet is generated when the tone stops.

Voice activity detection is optionally performed when no tone is detected. A silence packet is generated when VAD does not detect voice activity,

Voice encoding is performed whenever tone or silence packets are NOT generated. The channel's encoder type identifies which vocoder will be used. The vocoder output is formatted and packed into the vocoder's packet payload and sent to the host for transmission to the paired device.

Echo cancellation. Channel A's echo canceller cancels the echo contained in channel B's input from channel A's output. Similarly, channel B's echo canceller cancels the echo contained in channel A's input from channel B's output.

Each of the voice enhancement algorithms: packet echo canceller, VAD, and tone detection and tone relay; are independent options selectable at channel setup.

¹ Although not shown in the diagram, tone detection is performed using an echo canceller intermediate signal to improve the reliability of the tone detection.

5 XCD APIs

The **XCD** APIs are the interface between a user's application program and **XCD** DSP cores. The APIs execute in a host control processor connected to the DSP via the DSP's Host Port Interface (HPI). The APIs support multiple DSP cores and use a DSP Identifier to select a particular core. The association between a DSP Identifier and a particular DSP core is made by the user modified **XCD** support functions.

The APIs are provided as ANSI "C" source code.

6 **REFERENCES**

1. Adaptive Digital Technologies G.PAK Users Guide

2. Texas Instruments TMS320C6424 Fixed-Point Digital Signal Processor (literature number SPRS347C)

Adaptive Digital is a strategic member of the Texas Instruments Developer Network.

CONTACT INFORMATION

www.adaptivedigital.com
information@adaptivedigital.com
610.825.0182
1.800.340.2066
610.825.7616
525 Plymouth Road, Suite 316, Plymouth Woods
Plymouth Meeting, PA 19462



IMPORTANT NOTICE: Data subject to change, for the most up to date information visit our website. Customers are advised to obtain the most current and complete information about Adaptive Digital products and services before placing orders.

All trademarks are property of their respective owners.

