HDGW – C6472

High Density Gateway

TARGET APPLICATIONS

High Density Gateways

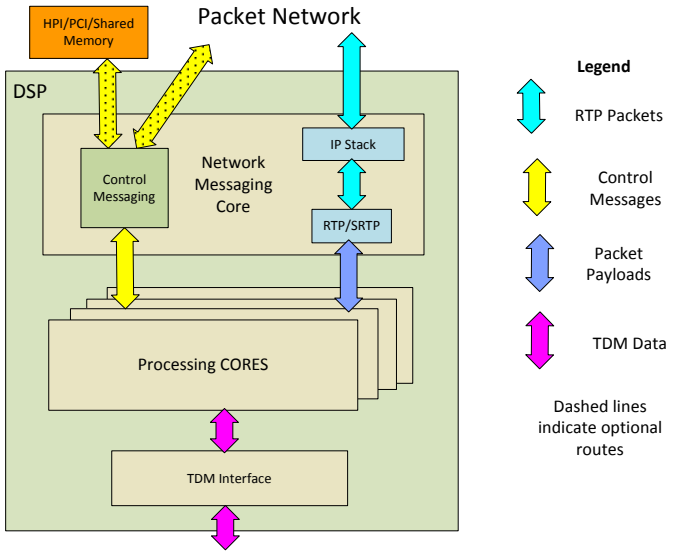
IP PBX/Gateway

VoIP Transcoding

OVERVIEW

Adaptive Digital's High Density Gateway product combines Adaptive Digital's G.PAK DSP software plus host APIs along with Texas Instruments' C6472 DSP to form a turnkey soft-chip for use in VoIP gateway equipment.

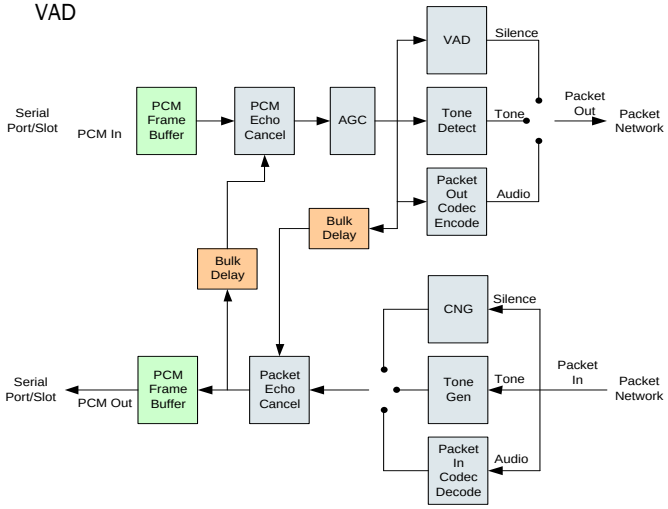
This product provides the functionality necessary to bridge traditional analog telephone lines and digital trunks to a digital Voice over IP Network.



Chip Block diagram

SOFTWARE FEATURES

- Voice Transcoding
- AGC
- DTMF
- Caller ID (Types ! and II)
- RTP
- SRTP
- Tone generation
- VAD
- Network Stack
- Codecs
  - G.711
  - G.722
  - G.723.1
  - G.726
  - G.729



Software Block diagram

Optional Software Features

- T.38 FAX Relay
- RFC 4733 Tone Relay
- Echo cancellation
- Conferencing

HARDWARE FEATURES

- 6 On-Chip DSP Cores @ 500/625/700 MHz
- 32 KB L1 Program Cache
- 32 KB L1 Data Cache
- 608 KB L2 Memory
- MII, RMII, GMII and RGMII EMAC
- 16-Bit HPI (Host Port Interface)
- 3 TSIP TDM Buses
- Up to 256 MB External Memory

ADDITIONAL HARDWARE FEATURES

- EDMA Controller
- 2 Serial Rapid IO Links
- I^2C Bus
- 16 GPIO Pins

SPECIFICATIONS

Product Number/Silicon	Channel Count	Description
TMS320C6472 / 700 MHz with 128 MB DDR2 @ 533 MHz	128 G.711	G.711 with DTMF detection.
	128 G.722	G.722 with DTMF detection.
	128 G.723	G.723 with DTMF detection.
	128 G.726	G.726 with DTMF detection.
	128 G.729 AB	G.729 A/B with DTMF detection.

DETAILED DESCRIPTION

A VoIP gateway acts as a bridge between traditional telephone equipment and VoIP equipment. Traditional telephone interfaces include both analog (FXS and FXO), and digital (PCM, T1/E1 DS0). These interfaces can be found in the PSTN (Public Switched Telephone Network), PBX (Private Branch Exchange) equipment in business offices, and in residential telephone equipment. Gateways enable users of traditional telephone equipment to make use of the benefits of VoIP. Without gateways, it is impossible for VoIP equipment to place calls to users of traditional telephone equipment. Stated differently, without VoIP gateways, traditional telephone equipment and VoIP equipment could not co-exist.

By performing functions such as voice and fax compression, decompression, packetization, call routing and control signaling, a VoIP gateway enables the data infrastructure to handle voice and fax applications.

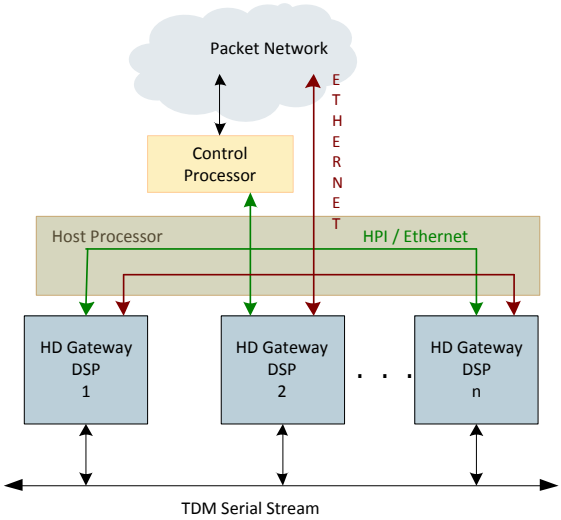


Figure 2: High Density Gateway system block diagram

Figure (2) shows a block diagram for a typical VoIP Gateway. A VoIP Gateway usually consists of a host control processor connected to one or more HDGW chips. The host processor typically controls the HDGW C6472 via either the host port interface or via Ethernet. The voice packets can be routed between the network and the HDGW chip via the control processor. Alternatively, the IP Gateway chip can be connected directly to the network via the Ethernet interface. The HDGW C6472 chip connects to the TDM interface via the chip's TDM serial port.

The major components in an IP Gateway chip include vocoders, echo cancellation, voice quality enhancement algorithms, and telephony algorithms. The HDGW C6472 chip supports the following channel types: TDM to Packet, Packet to Packet, TDM to Conference, Packet to Conference, and Conference Composite. Channel setup (identification of input and output ports, vocoders, and voice algorithms), conference setup, and teardown operations are controlled by the host processor using a set of HDGW C6472 API functions.

Channel Types

The HDGW C6472 provides only the TDM to Packet channel as standard. Channel types of: TDM to TDM, Packet to Packet, TDM to Conference, Packet to Conference, and Conference Composite are available as an option.

A TDM channel is typically associated with one of the following types of telephone interfaces:

- FXO
- FXS
- T1/E1 time slot (DS0)

Each channel in a DSP is dynamically setup as any type. Frame sizes, vocoder types, and tone detection types are selected when a channel is setup.

All channels (except for the conference composite channel type) are designed to operate as full duplex channels. A full duplex channel may be configured to operate as a half duplex by setting the end points of one-half of the full duplex channel to NULL end-points.

HOST API

The HDGW C6472 APIs are the interface between a user's application program and [IPG-C6472] DSP cores. The APIs execute in a host control processor connected to the DSP via either Ethernet or the DSP's Host Port Interface (HPI). The APIs support multiple DSP cores/chips and use a DSP Identifier to select a particular core. The association between a DSP Identifier and a particular DSP core/chip is made by the user modified [IPG-C6472] driver support functions.

The APIs are provided as ANSI "C" source code. The APIs will work with any host application regardless of the operating system being used.

REFERENCES

1. Adaptive Digital Technologies HDGW C6472 Users Guide
2. Texas Instruments TMS320C647 Fixed-Point Digital Signal Processor (literature number SPRS612G.)

Deliverables

The deliverable items are platform dependent. In general, there is a single DSP-downloadable binary image along with host API software in C source code format. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes. Sample/test code may be included as well.

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

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