G.722 Audio Coder

PRODUCT DESCRIPTION

The Adaptive Digital Technologies G.722 Audio Coder is a real-time implementation of the ITU G.722 audio coder. It is used with many applications that require audio frequency bandwidth coding such as video conferencing, multimedia, and speaker/microphone digital telephony. The G.722 audio coder encodes 16 kHz sampled audio signals for transmission over 48, 56, and 64 kbps channels, and provides 7 k Hz of audio bandwidth.

Furthermore, G.722 on TI's C55x™DSP, and ARM devices supports optional feature on the decoder side: Packet Loss Concealment. Adaptive Digital's G.722PLC is a high quality low-complexity proprietary algorithm for packet loss concealment with G.722. We also offer a Packet Loss Concealment algorithm compliant to the G.722 Appendix IV Standard.

Adaptive Digital's implementation of G.722 includes a proprietary VAD/CNG/DTX (Voice Activity Detection, Comfort Noise Generation / Discontinuous Transmission) feature. While many VoIP and wireless codecs include this type of functionality as part of the standard, G.722 does not. Adaptive Digital therefore implemented a proprietary implementation that is voice-quality-optimized for the G.722 codec. Adaptive Digital plans to make this available on other platforms in the near future.

FEATURES

- Functions are C-callable.
- Multi-channel capable
- Can be integrated with echo cancellers, VOX and tone detection/regeneration.
- Can be integrated with G.711/G.728 to provide the audio portion of the H.320 video standard.
- The encoder and decoder meet all ITU G.722 compliance data files.
- C55x and ARM – Optional Packet Loss Concealment (PLC): Proprietary technique developed by Adaptive Digital.
- ARM, Win32, and i686 – Optional PLC compliant to G.722 Appendix IV Standard

AVAILABILITY

ADT G.722 is available on the following Platforms: Other configurations are available upon request.

Product	Platform	Memory Model	Endian	Code Gen Tool Version
adt_g722_armv7a	ARM Cortex-A8/A9/A12/A15/A17	N/A	Little	Android NDK r6b
adt_g722_ armv8a	ARM Cortex- A53/A57	N/A	Little	Android NDK r6b
adt_g722_cortex-m3 / -m4	ARM Cortex-M3/M4	N/A	Little	GCC v 4.5.2*
adt_g722_arm9e /11	ARM9E / 11	N/A	Little	N/R
adt_g722_c64x/_c66xp/_c66x/_c674x	TI TMS320C64x/C64x+/C66x/C674x	Far	N/A	N/R
adt_g722_c55x	TI TMS320C55x	Large	Little	N/R
adt_g722_c54x	TI TMS320C54x	L3	Little	N/R

*GCC v 4.5.2 (Sourcery G++2011.03-41)

ADT G.722 PLC is available on the following Platforms: Other configurations are available upon request.

Product	Platform	Memory Model	Endian	Code Gen Tool Version
adt_g722plc_armv7a	ARM Cortex-A8/A9/A12/A15/A17	N/A	Little	Android NDK r6b
adt_g722plc_ armv8a	ARM Cortex- A53/A57	N/A	Little	Android NDK r6b
adt_g722plc_cortex-m3 / -m4	ARM Cortex-M3/M4	N/A	Little	GCC v 4.5.2*
adt_g722plc_arm9e /11	ARM9E / 11	N/A	Little	N/R
adt_g722plc_dll	Win32 dll	N/A	Little	VS2010
adt_g722plc _lx84	Win32 static lib	N/A	Little	VS2010
adt_g722plc _i686	I686	N/A	Little	gcc

ADT G.722 Annex IV is available on the following Platforms: Other configurations are available upon request.

Product	Platform	Memory Model	Endian	Code Gen Tool Version
adt_g722 annex4_armv7a	ARM Cortex-A8/A9/A12/A15/A17	N/A	Little	Android NDK r6b
adt_g722 annex4_ armv8a	ARM Cortex- A53/A57	N/A	Little	Android NDK r6b
adt_g722 annex4_cortex-m3 / -m4	ARM Cortex-M3/M4	N/A	Little	GCC v 4.5.2*
adt_g722 annex4_arm9e /11	ARM9E / 11	N/A	Little	N/R
adt_g722 annex4_dll	Win32 dll	N/A	Little	VS2010
adt_g722 annex4_lx84	Win32 static lib	N/A	Little	VS2010
adt_g722 annex4 _i686	I686	N/A	Little	gcc

Endian, byte order: “Little Endian” means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

Acronyms

Mm – Memory Model: Memory Model is specific to Texas Instruments processors.

N/A – Not Applicable

N/R – Not Recorded

GCC - GNU Compiler Collection

SPECIFICATIONS

Coding Rate: 48, 56, or 64 kbps

Sampling Rate: 16 kHz

Delay: 125 microseconds

NOTE: We specify MIPS (Millions of Instructions Per Second) as MCPS (Millions of Instruction Cycles Per Second). Unless otherwise specified, peak MIPS are indicated.

TI TMS3200

G.722 C64x/C64x+/C66x/C674x

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G.722 Encode	5.3	4768	1426	192
G.722 Decode	4.8			

G.722 C64x/C64x+ Variant processes 2 channels simultaneously thereby by reducing the per channel MIPS by a factor of 2.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G.722 Encode Variant	2.84	8000	1664	364
G.722 Decode Variant	2.36			

*Note: Above numbers for non-cached. After caching, cycle count will improve.

G.722 C55x

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
Encode	6.0	2717	1212	164
Decode	4.8			164
Decode with PLC* enable	5.5	3811	609	3528

*Note: Proprietary technique developed by Adaptive Digital.

G.722 C54x

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of 16-bit word.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	7.5	1438	654	80
Decode	6.4			80

ARM® DEVICES

G.722 CORTEX-A8/A9/A15 / CORTEX-M3/M4

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs		Program Memory	Data Memory	Per Channel Data Memory
	M3/M4	A8/A9/A15			
G.722 Encode	12.4	5.9	6996	1284	146
G.722 Decode	11.3	5.3			

G.722 with PLC CORTEX-A8/A9/A12/A15/A17

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G722_ADT_encode	13.5	42k	7.6k	288
G722_ADT_decode	7.4			288
G722_ADT_decode_withPLC enable	11.1			4248

G.722 with PLC CORTEX-M3/M4

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G722_ADT_encode	16.1	30k	1.5k	288
G722_ADT_decode	15.2			288
G722_ADT_decode_withPLC enable	22.3			4248

* Adaptive Digital's G.722 ARM-Cortex-A device family version also has optional packet loss concealment (PLC) plus a proprietary VAD/CNG/DTX feature.

G.722 Annex I V CORTEX-A8/A9/A12/A15/A17

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G722_ADT_encode	13.5	43k	7.7k	288
G722_ADT_decode	7.4			288
G722_ADT_decode_withPLC enable	11.1			2020

G.722 Annex I V CORTEX-M3/M4

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPs	Program Memory	Data Memory	Per Channel Data Memory
G722_ADT_encode	16.1	30k	1.7k	288
G722_ADT_decode	15.2			288
G722_ADT_decode_withPLC enable	21.3			2020

G.722 ARM9E/ARM11

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Device	MIPs	Program Memory	Data Memory	Per Channel Data Memory
ARM9E	25.5	5.3k	1.3k	292
ARM11	41.4	5.2k		

G.722 with PLC ARM9E/ARM11

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	11.3	34K	7.6K	288
Decode	11			288
Decode with PLC* enable	16.9			4248

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

G.722 Annex I V - PLC ARM9E/ARM11

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	11.3	58K	7.7K	288
Decode	11			288
Decode Annex IV	16.9			2020

WINDOWS

G.722 with PLC Win DLL

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	14.5	12k	9.3k	288
Decode	12.9			288
Decode with PLC* enable	14.9			4248

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

G.722 with PLC Win Static Library

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	13.9	12k	9.3k	288
Decode	12.9			288
Decode with PLC* enable	14.9			4248

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

G.722 Annex I V Win32 – DLL or Static library

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	13.6	31k	18k	288
Decode	12.9			288
Decode with PLC* enable	13.3			2020

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

LINUX

G.722 with PLC I686

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	11.2	27k	7.6k	288
Decode	11.2			288
Decode with PLC* enable	13.9			4248

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

G.722 Annex I V I686

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	MIPS (Peak)	Program Memory	Data Memory	Per-Channel Data Memory
Encode	10.8	51k	7.7k	288
Decode	10.5			288
Decode with PLC* enable	10.8			2020

*PLCDecode MIPS measurement taken with simulated 2% packet loss.

FUNCTIONS

API function call summary

```
ResetG722 ()            Initializes the G.722 audio coder Channel structures

EncodeG722 ()           Executes the G.722 encoder

DecodeG722  ()          Executes the G.722 decoder
```

Deliverables

The deliverable items are platform dependent. In general, there is one library. (Sometimes multiple variants of the library are included in the deliverables.) There are also header files, some of which are specific to the product and others are common across many of Adaptive Digital's products. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes and a data sheet. Sample/test code may be included as well.

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

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