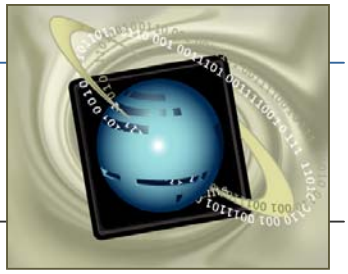


GSM / ITU Wireless Voice

Transcoding Chip Solution

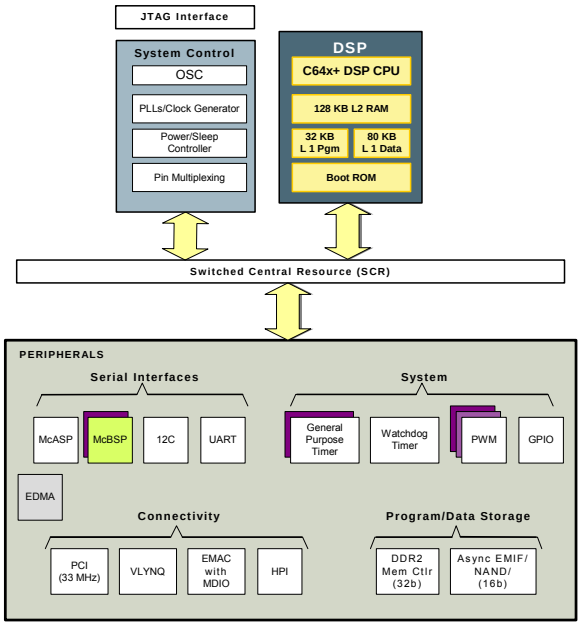
The Adaptive Digital GSM / ITU Wireless Voice Transcoding Chip provide a complete high-density solution for simultaneously converting multiple voice channels between the wireless and fixed line networks. The Transcoder chips combine Adaptive Digital's field-proven DSP software with Texas Instruments Incorporated (TI) high performance fixed-point TMS320C64x+™ DSPs. The chip is a complete solution designed to enable designers to increase the value of their end product thus providing a superior voice experience to the customer.

Supporting multiple codecs is one of the most challenging aspects effecting VoIP services across telephone, cable, cellular, Wi-Fi, and Internet networks. As VoIP networks, usage, and applications expand, the need to translate traffic from one codec type to another becomes more and more important to ensure global connectivity. Transcoding is the ability to adapt digital files so that content can be viewed on different playback devices. Working like an interpreter, a transcoder translates files to a suitable format for the end user.

1 HARDWARE FEATURES - TI TMS320C6424™ DSP

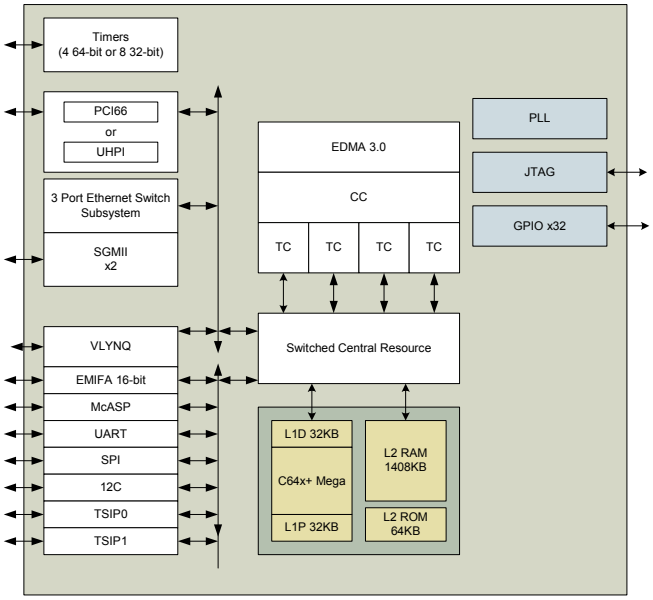
The C6424 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for digital signal processor applications.

- High-Performance
  - 400-/500-/600-/700-MHz, C64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 2.5-, 2-, 1.67-, 1.43-ns Instruction Cycle Time
- 16-Bit Host-Port Interface (HPI)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- C64x+ L1/L2 Memory Architecture
- Two Multichannel Buffered Serial Ports
- 10/100 Mb/s Ethernet MAC (EMAC)
- Multichannel Audio Serial Port (McASP0)
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- Up to 111 General-Purpose I/O (GPIO) Pins
- Port count: 64
- 3.3-V and 1.8-V I/O, 1.2-V Internal
- 3.3-V and 1.8-V I/O, 1.05-V Internal



1.1 HARDWARE FEATURES - TI TMS320C6452™ DSP

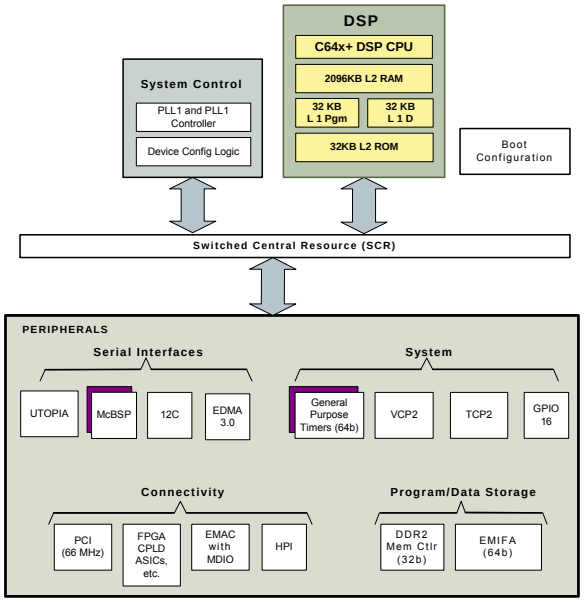
- High-Performance
  - 720, 900--MHz, C64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 1.39, 1.11-ns Instruction Cycle Time
- 1 32/16-Bit Host-Port Interface (HPI)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- C64x+ L1/L2 Memory Architecture
- Two Telecom Serial Interface Ports (TSIP0/1)
- Multichannel Audio Serial Port (McASP0)
- Ten Serializers and SPDIF (DIT) Mode
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- 32 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions) Power
- 3.3-V and 1.8-V I/O, 1.2-V Internal (-720, -900)



The TMS320TCI6452 DSP is a multicore device with large, on-chip shared memory, a DDR interface and Serial RapidIO for inter-DSP communications. Gigabit Ethernet is embedded for native connectivity to IP-based systems. The TCI6486 is ideal for high-density transcoding in mobile video distribution systems.

1.1 HARDWARE FEATURES - TI TMS320C6455™ DSP

- High-Performance
  - 720/850/-MHz, 1/1.2 GHzC64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 1.39-, 1.17, 1-, and 0.83-ns Instruction Cycle Time
- Enhanced Turbo Decoder Coprocessor (TCP2)
- DDR2 Memory Controller
- Enhanced Direct-Memory-Access 3 (EDMA3)
- 64 Independent Channels
- 64-Bit External Memory Interface (EMIFA)
- Two Multichannel Buffered Serial Ports
- 10/100/1000 Mb/s Ethernet MAC (EMAC)
- 32-/16-Bit Host-Port Interface (HPI)
- One Inter-Integrated Circuit (I2C) Bus
- IEEE-1149.1 (JTAG™)
- Boundary-Scan-Compatible



TI TMS320C6455 DSP

This solution is based upon TMS320C6455 DSP. The TMS320C6455 DSP has proven itself in demanding applications, including video and telecom infrastructures. Using 90-nm process technology, the C6455 supports as many as

9,600 MIPS at a 1.2-GHz clock rate. The C6455 also features Serial RapidIO™ for high-speed, low latency interprocessor communications, critical in real-time systems such as video processing equipment.

1.2 HARDWARE FEATURES - TI TMS320TCIC6486™ DSP

- Six On-Chip TMS320C64x+ Megamodules
- Endianess: Little Endian, Big Endian
- High-Performance
  - 500 MHz/625 MHz
  - Eight 32-Bit Instructions/Cycle
- Dedicated SPLOOP Instruction
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- 32-Bit DDR2 Memory Controller
- Two 1x Serial RapidIO® Links
- UTOPIA Level 2 Slave ATM Controller
- L1/L2 Memory Architecture
  - 256K-Bit (32K-Byte) L1P Program
  - 256K-Bit (32K-Byte) L1D RAM/Cache
- Three Telecom Serial Interface Ports (TSIPs)
  - Each TSIP is 8 Links of 8 Mbps per direction
- Two 10/100 Mb/s Ethernet MACs (EMACs)
- 16-Bit Host-Port Interface (HPI)
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- 16 General-Purpose I/O (GPIO) Pins

This solution is based upon TMS320TCI6486 DSPThe TMS320TCI6486 device has six 500-MHz-optimized TMS320C64x+™ megamodules, which combinehigh performance with the lowest power dissipation per port. The C64x+ megamodules are thehighest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C64x+megamodule is based on the third-generation high-performance, advanced

2 SOFTWARE FEATURES - ADAPTIVE DIGITAL

- G.711 with appendices 1(Packet Loss Concealment) and 2 (silence suppression, voice activity detection (VAD), discontinuous transmission (DTX), and comfort noise generation (CNG))
- T-38 Fax Relay
- G.729 AB
- DTMF Detect
- Automatic Gain Control (AGC)
- G.168 EC Certified by AT&T Voice Quality Lab
- Tone Generate
- Tone Relay
- Supports TDM to Packet Channel
- RTP payload formatting
- Transcoding

OPTIONAL FEATURES

- G.723.1A
- G.726
- G.728
- Conferencing
- GSM AMR
- MELP
- Channel types: TDM to TDM, Packet to Packet, TDM Conference, Packet Conference, Conference Composite

3 CHANNEL DENSITY

Application	Solution	Product Number/Silicon	Channel Count	Description
GSM / ITU Wireless Voice Transcoder	XCODE	XCD TMS320C6424V	16	C64x+ core 400-, 500-, 600-MHz C64x+™ Clock Rate 1, 16-Bit Host-Port Interface (HPI) 10/100 Mb/s EMAC2 McBSPs
	XCODE	XCD TMS320C6452V	32	C64x+ core 720, 900-MHz C64x+™ Clock Rate 32-/16-Bit Host-Port Interface 64 32-bit General-Purpose Registers Five Configurable Video Ports
	XCODE	XCD TMS320C6455V	32	C64x+ core 720-MHz, 850-MHz, 1-GHz, & 1.2-GHz Clock Rate 32-/16-Bit Host-Port Interface (HPI) 10/100/1000 Mb/s EMACs2 McBSPs
	XCODE	XCD TMS320C6472	72, 96	6 C64X+ Megamodules (cores) @ 500 MHz ea. 608 KB L2 RAM3 TSIP (Telecom Serial Ports) 10/100/1000 Mb/s EMAC

Codec transcoding provides a means to convert traffic so that two VoIP networks using different codecs can exchange traffic without making codec format changes on their individual network devices. Transcoding efficiently and effectively interconnects traffic thereby allowing each provider's network to use its codec of choice.

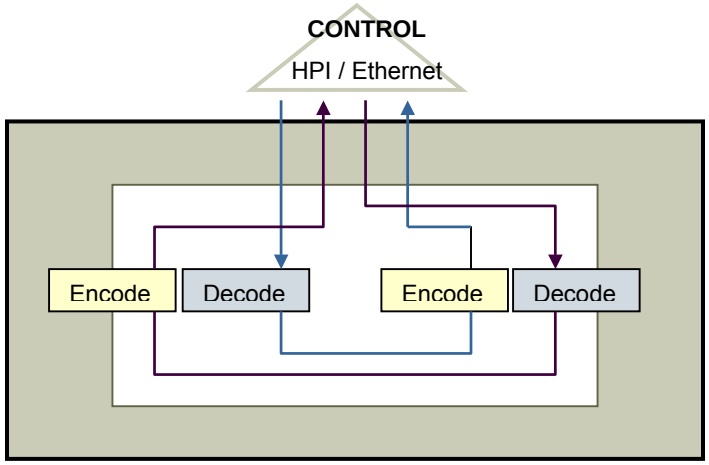


Figure 2: Transcoding chip Block Diagram

4.1 Channel Type

Packet to Packet Channel Type

The Packet to packet channel type provides a linkage between packet channels. Packet to packet channels are typically used in gateway applications to perform frame size conversions, codec type conversions (transcoding), and/or echo cancellation of packet data. This type of channel can also be used to convert silence and tone packets to audio packets or to convert audio packets to silence and tone packets. Channels of this type have two threads of processing as shown in figure 3. Each VIP-P packet to packet channel is half duplex; however, these channels are always allocated in pairs (channels A and B) to allow full duplex operation.

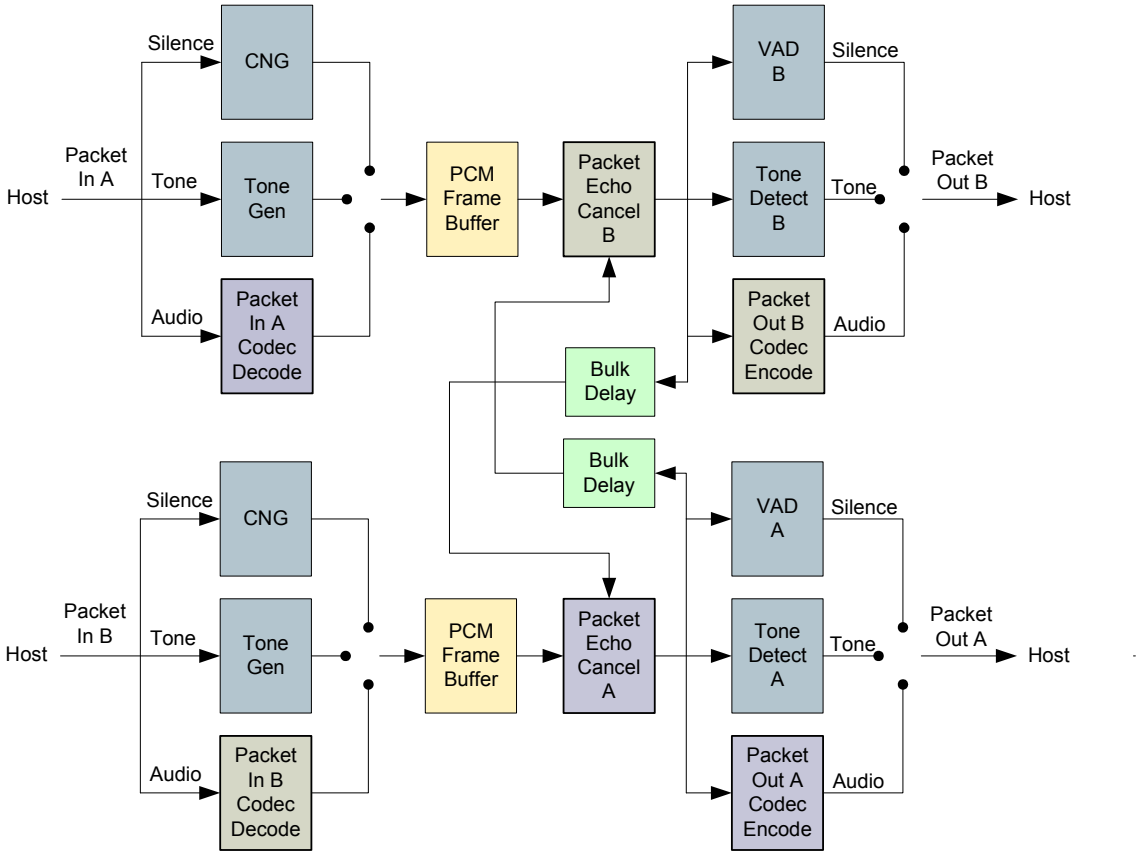


Figure 3– Packet to Packet Channel

Packet decode processing. The packet decoding thread reads a channel ‘s packet from the host control processor and generates and buffers 8 KHz samples according to the received packet type. If a silence packet is received, comfort noise is generated. If a tone packet is received, the specified tone is generated. If an audio packet is received, it is decoded according to the input packet codec type. The generated PCM samples are buffered for encoding by the paired channel.

Packet encode processing. When enough of the paired channel's PCM samples are buffered to build an output frame, this PCM data is optionally passed through the packet echo canceller, the tone detector (TD) and the voice activity detector (VAD).

Tone detection is optionally performed on the PCM data after the G.168 echo cancellation [1] but prior to the non-linear post-processing of the echo canceller. XCD notifies the host at the start and end of each tone. If tone relay is enabled, tone packets are generated for each frame until the tone ends; an end of tone packet is generated when the tone stops.

Voice activity detection is optionally performed when no tone is detected. A silence packet is generated when VAD does not detect voice activity,

Voice encoding is performed whenever tone or silence packets are NOT generated. The channel's encoder type identifies which vocoder will be used. The vocoder output is formatted and packed into the vocoder's packet payload and sent to the host for transmission to the paired device.

Echo cancellation. Channel A's echo canceller cancels the echo contained in channel B's input from channel A's output. Similarly, channel B's echo canceller cancels the echo contained in channel A's input from channel B's output.

Each of the voice enhancement algorithms: packet echo canceller, VAD, and tone detection and tone relay; are independent options selectable at channel setup.

[1] Although not shown in the diagram, tone detection is performed using an echo canceller intermediate signal to improve the reliability of the tone detection.

5 XCD APIs

The **XCD** APIs are the interface between a user's application program and **XCD** DSP cores. The APIs execute in a host control processor connected to the DSP via the DSP's Host Port Interface (HPI). The APIs support multiple DSP cores and use a DSP Identifier to select a particular core. The association between a DSP Identifier and a particular DSP core is made by the user modified **XCD** support functions.
The APIs are provided as ANSI "C" source code.

6 REFERENCES

1. Adaptive Digital Technologies G.PAK Users Guide
2. Texas Instruments TMS320C6424 Fixed-Point Digital Signal Processor (literature number SPRS347C)
3. Texas Instruments TMS320C6455 Fixed-Point Digital Signal Processor (literature number SPRS276H)
4. Texas Instruments TMS320C648x Digital Signal Processor (literature number SPRU894D)

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

CONTACT INFORMATION

Web:	www.adaptivedigital.com
Email:	information@adaptivedigital.com
Tel:	610.825.0182
Toll Free:	1.800.340.2066
Fax:	610.825.7616
Address:	525 Plymouth Road, Suite 316, Plymouth Woods Plymouth Meeting, PA 19462