G.723.1 Audio Coder

PRODUCT DESCRIPTION

Dual rate speech coder for multimedia communications transmitting at 5.3 and 6.3 kbit/s.

The Adaptive Digital Technologies' G.723 voice coder is a real-time implementation of the ITU G.723.1 voice coder. It is used with many applications that require high quality, robust speech reproduction. **Due to its low bandwidth requirement, G.723.1 is ideal for VoIP applications.** G.723.1 is specified in numerous Voice-Over-Packet environments such as Voice-Over-IP, and Voice-Over-ATM.

FEATURES

- Fixed bit rate (5.3 kbit/s with 20 byte 30 ms frames, 6.3 kbit/s with 24 byte 30 ms frames)
- Functions are C-callable.
- eXpress DSP Compliant.
- Can be integrated with echo cancellers, VOX and tone detection/regeneration.
- The encoder and decoder meet all ITU G.723.1 compliance data files interoperability requirements.
- C64x xDM Compliant: easy codec implementation and integration for DaVinci™ Technology

AVAILABILITY

ADT G.723.1 is available on the following Platforms: Other configurations are available upon request.

Product	Platform	Memory Model	Endian	Code Gen Tool Version
ADT_g723-1_C64xp	TI TMS320C64x+	MmL3	Little	N/R
ADT_g723-1_C674x	TI TMS320C674x	MmL3	Little	N/R
ADT_g723-1_c64x	TI TMS320C64x	MmL3	Little	N/R
ADT_g723-1_c62x	TI TMS320C62x	MmL3	Little	N/R
ADT_g723-1_c55x	TI TMS320C55x	Large	Little	N/R
ADT_g723-1_c54x	TI TMS320C54x	Far	N/A	N/R
ADT_G723-1_WIN32_LIB	Windows/x86 LIB	N/A	N/A	--
ADT_G723-1_WIN32_DLL	Windows/x86 DLL	N/A	N/A	--
ADT_g723_1_i686	I686	N/A	Little	gcc
ADT_g723_1_cortex-m3	Cortex-M3	N/A	Little	2011_09-69_BareMetal
ADT_g723_1_cortex-a8	Cortex-A8	N/A	Little	2011_09-70_linux
ADT_g723_1_arm9	ARM9e	N/A	Little	2011_09-70_linux

Endian, byte order: "Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

Acronyms

Mm – Memory Model: Memory Model is specific to Texas Instruments processors.

N/A – Not Applicable

N/R – Not Recorded

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SPECIFICATIONS

Coding Rate: 5.3 or 6.3 kbps

Sampling Rate: 8 kHz

Delay: 37.5 microseconds

SPECIFICATIONS CONTINUED

TI TMS320C6000

C64x

MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Function	Program Memory		Data Memory	Per Channel Data Memory	Stack
Encode	Common 10112	40128	23812	1420	444
Decode		8920	21364	400	260

SPECIFICATIONS CONTINUED

C64x+

MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

G.722 C64x Variant processes 2 channels simultaneously thereby by reducing the per-channel MIPS by a factor of 2.

Function	Program Memory		Data Memory	Per Channel Data Memory	Stack
Encode	Common 10208	35232	23880	1420	444
Decode		9152	21432	400	260

C6x Processor Utilization

CPU UTILIZATION

All Memory usage is given in units of byte.

Rate	MIPS		
	C62x	C64x*	C64x+
5.3 Encode	6.1	7.8	7.2
5.3 Decode	0.57	0.7	0.62
6.3 Encode	5.7	7.3	7.0
6.3 Decode	0.57	0.7	0.62

*Note: C64X MIPS is different from C62X MIPS, because C64X has different cache and cross path architecture.

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TI TMS320C5000

C55x - Standard – G.723.1 Annex A*

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Rate	MIPS	Program Memory	Data Memory	Per Channel Data Memory
5.3 Encode	11.2	21502	21716	1480
5.3 Decode	1.3			424
6.3 Encode	11.2	21502	21716	1480
6.3 Decode	1.4			424

C55x - Low Memory – G.723.1 Annex A*

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

Rate	MIPS**	Program Memory	Data Memory	Per Channel Data Memory
5.3 Encode	11.2	21620	20744	1480
5.3 Decode	1.3			424
6.3 Encode	11.2	21620	20744	1480
6.3 Decode	1.4			424

*G.723.1 Annex A, which specifies silence suppression, voice activity detection (VAD), discontinuous transmission (DTX), and comfort noise generation (CNG), is included.

**Note: The MIPS is measured when the program placed internally, and channel and tables are placed in the DARAM. For the low memory version build, the total MIPS usage increases by 0.5 MIPS.

C54x – G.723.1 Annex A*

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of 16-bit word.

Rate	MIPS (Peak)	Program Memory	Data Memory	Table Memory	Per-Channel Data Memory
5.3	22.6	14K	1K	10K	1K
6.3	20.56	14K	1K	10K	1K

*G.723.1 Annex A, which specifies silence suppression, voice activity detection (VAD), discontinuous transmission (DTX), and comfort noise generation (CNG), is included.

ARM® DEVICES

ARM9E / ARM11 | Cortex-M3/M4

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Function	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
Encode	224	193k	18,980	1600	8
Decode	13			504	8

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Arm Cortex-A8 / A9 / A15

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Function	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
Encode	131	166k	18,980	1600	8
Decode	8			504	8

LINUX

i686

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Function	MIPS	Program Memory	Data Memory	Per Channel Data Memory	Scratch Memory
Encode	145	160k	19,176	1600	8
Decode	8			504	8

We specify MIPS (Millions of Instructions Per Second) as MCPS (Millions of Instruction Cycles Per Second). Unless otherwise specified, peak MIPS are indicated.

PC-WINDOWS

PLATFORM PC-WINDOWS

CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

Function	MIPS Average	Program Memory	Data Memory	Scratch	Per Channel Data Memory	Stack	Heap-Persistent	Heap - Scratch
Encode	95	70,000	19,000	16	2100	<20 KB	See Per-channel	See Per-channel
Decode	8							

We specify MIPS (Millions of Instructions Per Second) as MCPS (Millions of Instruction Cycles Per Second). Unless otherwise specified, peak MIPS are indicated.

FUNCTIONS

API function call summary

```
codInitializeG723Channel (. . .)    Initializes the G.723 voice coder software
decInitializeG723Channel(. . .)     Initializes the G.723 voice decoder software
EncodeG723(. . .)                   Executes the G.723 encoder
DecodeG723(. . .)                   Executes the G.723 decoder
```


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Memory Specifications Description

Program Memory – (also known as text, code)

Data Memory – data memory that is common across multiple channels. Tables, .cinit. const, etc.)

Scratch Data – data memory that does not need to be preserved from one algorithm call to the next. Scratch data can be shared with other algorithms or other instances of the same algorithm in a non-preemptive environment.

Per Channel Data – data memory that needs to be preserved from one algorithm call to the next.. Also known as instance data or persistent data.

Stack

Heap - Persistent – dynamically allocated memory that must be maintained from one algorithm call to the next. This would typically be allocated at initialization time. (Rarely used by Adaptive Digital algorithms)

Heap – Scratch – dynamically allocated memory that is allocated on the fly and freed before the return from any algorithm functions. (Rarely used by Adaptive Digital algorithms)

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Deliverables

The deliverable items are platform dependent. In general, there is one library. (Sometimes multiple variants of the library are included in the deliverables.) There are also header files, some of which are specific to the product and others are common across many of Adaptive Digital's products. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes and a data sheet. Sample/test code may be included as well.

Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.

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