High Density PCM / Packet

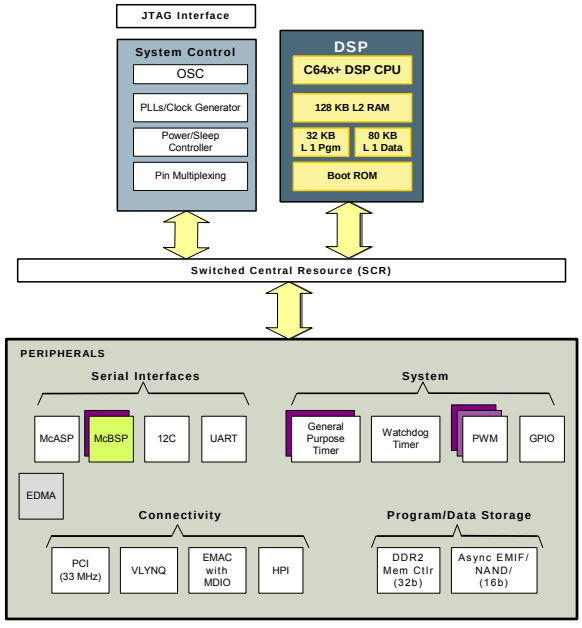
Conferencing Chip Solution

The Adaptive Digital Conferencing Chips offer a complete solution designed to enable designers to increase the value of their end product thus providing a superior voice experience to the customer. Adaptive Digital's Conferencing chip solutions provide all of the essential voice quality features needed to create sophisticated telephony equipment. The PCM Conferencing (CONF-T) and Packet conferencing (CONF-P) chips combine Adaptive Digital's field-proven DSP software with Texas Instruments Incorporated (TI) high performance fixed-point TMS320C64x+™ DSPs.

The Adaptive Digital PCM conference chip (CONF-T-1024/1536) is designed to provide up to 1536 channels of conference call capability to telephone systems. The Packet Conference chip (CONF-P-416/512) provides up to 512channels of conference call capability. The number of conferences and number of members per conference is fully programmable, providing the ultimate flexibility.

1 HARDWARE FEATURES - TI TMS320C6424™ DSP

- High-Performance
  - 400-/500-/600-/700-MHz, C64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 2.5-, 2-, 1.67-, 1.43-ns Instruction Cycle Time
- 16-Bit Host-Port Interface (HPI)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- C64x+ L1/L2 Memory Architecture
- Two Multichannel Buffered Serial Ports
- 10/100 Mb/s Ethernet MAC (EMAC)
- Multichannel Audio Serial Port (McASP0)
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- Up to 111 General-Purpose I/O (GPIO) Pins
- Port count: 64
- 3.3-V and 1.8-V I/O, 1.2-V Internal
- 3.3-V and 1.8-V I/O, 1.05-V Internal



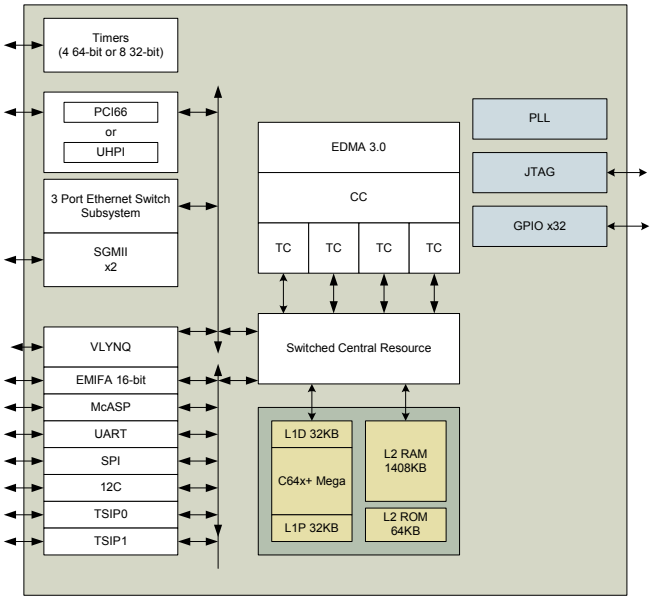
This solution is based upon the TI TMS320C6424 DSP. The C6424 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for digital signal processor applications.

1.1 HARDWARE FEATURES - TI TMS320C6452™ DSP

- High-Performance
  - 720, 900--MHz, C64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 1.39, 1.11-ns Instruction Cycle Time
- 1 32/16-Bit Host-Port Interface (HPI)
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- C64x+ L1/L2 Memory Architecture
- Two Telecom Serial Interface Ports (TSIP0/1)
- Multichannel Audio Serial Port (McASP0)
- Ten Serializers and SPDIF (DIT) Mode
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- 32 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)

Power

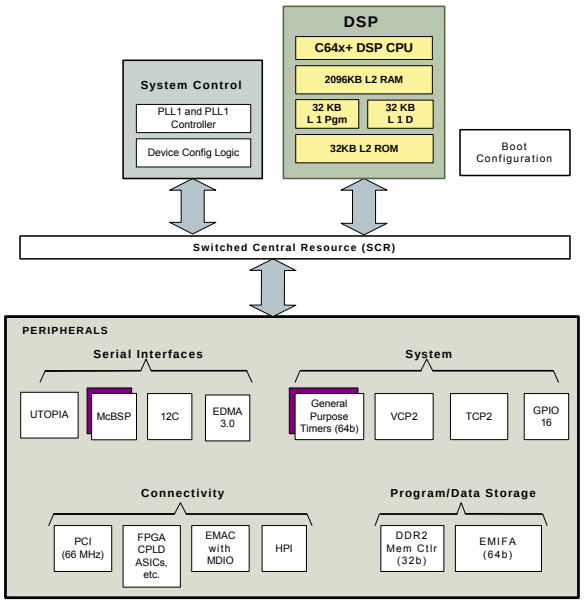
- 3.3-V and 1.8-V I/O, 1.2-V Internal (-720, -900)



The TMS320TCI6452 DSP is a multicore device with large, on-chip shared memory, a DDR interface and Serial RapidIO for inter-DSP communications. Gigabit Ethernet is embedded for native connectivity to IP-based systems. The TCI6486 is ideal for high-density transcoding in mobile video distribution systems.

1.1 HARDWARE FEATURES - TI TMS320C6455™ DSP

- High-Performance
  - 720/850/-MHz, 1/1.2 GHzC64x+™Clock Rate
  - Eight 32-Bit C64x+™ Instructions/Cycle
  - 1.39-, 1.17, 1-, and 0.83-ns Instruction Cycle Time
- Enhanced Turbo Decoder Coprocessor (TCP2)
- DDR2 Memory Controller
- Enhanced Direct-Memory-Access 3 (EDMA3)
- 64 Independent Channels
- 64-Bit External Memory Interface (EMIFA)
- Two Multichannel Buffered Serial Ports
- 10/100/1000 Mb/s Ethernet MAC (EMAC)
- 32-/16-Bit Host-Port Interface (HPI)
- One Inter-Integrated Circuit (I2C) Bus
- IEEE-1149.1 (JTAG™)
- Boundary-Scan-Compatible



TI TMS320C6455 DSP

This solution is based upon TMS320C6455 DSP. The TMS320C6455 DSP has proven itself in demanding applications, including video and telecom infrastructures. Using 90-nm process technology, the C6455 supports as many as 9,600 MIPS at a 1.2-GHz clock rate. The C6455 also features Serial RapidIO™ for high-speed, low latency interprocessor communications, critical in real-time systems such as video processing equipment.

1.2 HARDWARE FEATURES - TI TMS320TCIC6486™ DSP

- **Six On-Chip TMS320C64x+ Megamodules**
- **Endianess: Little Endian, Big Endian**
- High-Performance
  - **500 MHz/625 MHz**
  - Eight 32-Bit Instructions/Cycle
- **Dedicated SPLOOP Instruction**
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- **32-Bit DDR2 Memory Controller**
- **Two 1x Serial RapidIO® Links**
- **UTOPIA Level 2 Slave ATM Controller**
- L1/L2 Memory Architecture
  - **256K-Bit (32K-Byte) L1P Program**
  - **256K-Bit (32K-Byte) L1D RAM/Cache**
- **Three Telecom Serial Interface Ports (TSIPs)**
  - **Each TSIP is 8 Links of 8 Mbps per direction**
- Two 10/100 Mb/s Ethernet MACs (EMACs)
- 16-Bit Host-Port Interface (HPI)
- IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
- On-Chip ROM Bootloader
- 16 General-Purpose I/O (GPIO) Pins

This solution is based upon TMS320TCI6486 DSPThe TMS320TCI6486 device has six 500-MHz-optimized TMS320C64x+™ megamodules, which combinehigh performance with the lowest power dissipation per port. The C64x+ megamodules are thehighest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C64x+megamodule is based on the third-generation high-performance, advanced

2 SOFTWARE FEATURES - ADAPTIVE DIGITAL

- **G.168 EC Certified by AT&T Voice Quality Lab**
- ITU G.168-2002 Compliant
- **Excellent voice quality maintained even in large conferences**
- Supports TDM or packet interface for input and output data
- DTMF Detection
- Tone Generation
- Voice Playout
- Voice Record
- **Available in wideband, narrowband or mixedband versions**

3 CHANNEL DENSITY

Application	Solution	Product Number/Silicon	Channel Count	Description
PCM Conferencing	CONF-T	CONF-T-512 TMS320C6416V	512	C64x+ core 400-, 500-, 600-MHz C64x+™ Clock Rate 1, 16-Bit Host-Port Interface (HPI) 2 McBSPs
	CONF-T	CONF-T-256 TMS320C6424V	4 - 256	C64x+ core 400-, 500-, 600-MHz C64x+™ Clock Rate 1, 16-Bit Host-Port Interface (HPI) 10/100 Mb/s EMAC2 McBSPs
	CONF-T	EC-N-96 TMS320C6452V	256, 512	C64x+ core 720, 900-MHz C64x+™ Clock Rate 32-/16-Bit Host-Port Interface 64 32-bit General-Purpose Registers Five Configurable Video Ports
	CONF-T	Conf-48/64 TMS320C6455V	720	C64x+ core 720-MHz, 850-MHz, 1-GHz, & 1.2-GHz Clock Rate 32-/16-Bit Host-Port Interface (HPI) 10/100/1000 Mb/s EMACs2 McBSPs
	CONF-T	EC-N-256/320 TMS320C6472	1024, 1536	6 C64X+ Megamodules (cores) @ 500 MHz ea. 608 KB L2 RAM3 TSIP (Telecom Serial Ports) 10/100/1000 Mb/s EMAC

Application	Solution	Product Number/Silicon	Channel Count	Description
Packet Conferencing	CONF-P	CONF-T-256 TMS320C6424V	64, 72	C64x+ core 400-, 500-, 600-MHz C64x+™ Clock Rate 1, 16-Bit Host-Port Interface (HPI) 10/100 Mb/s EMAC2 McBSPs
	CONF-P	CONF-P-TMS320C6452V	96, 128	C64x+ core 720, 900-MHz C64x+™ Clock Rate 32-/16-Bit Host-Port Interface 64 32-bit General-Purpose Registers Five Configurable Video Ports
	CONF-P	CONF-P-TMS320C6455V	224	C64x+ core 720-MHz, 850-MHz, 1-GHz, & 1.2-GHz Clock Rate 32-/16-Bit Host-Port Interface (HPI) 10/100/1000 Mb/s EMAC, 2 McBSPs
	CONF-P	CONF-P-416-512 TMS320C6472	416, 512	6 C64X+ Megamodules (cores) @ 500 MHz ea. 32 KB L1P RAM, 32 KB L1D RAM 608 KB L2 RAM3 TSIP (Telecom Serial Ports) 32 bit DDR2 @ 533 MHz 10/100/1000 Mb/s Ethernet MAC (EMAC)

DEVICE OVERVIEW

The Adaptive Digital PCM conference chip (CONF-T-1024/1536) is designed to provide up to 1536 channels of conference call capability to telephone systems. The Packet Conference chip (CONF-P-416/512) provides up to 512channels of conference call capability. The number of conferences and number of members per conference is fully programmable, providing the ultimate flexibility.

The conferencing chip adds the active conference input signals together to form a composite signal. The conference chip makes use of sophisticated voice activity detection, noise reduction, and dominant speaker selection algorithms in order to maximize voice quality, even in very large conferences. Automatic Gain Control (AGC) is used to compensate for channels with different attenuation characteristics. Before sending the composite signal back to each conference member, that member's transmission is removed from the composite signal to avoid the perception of echo. The composite signal is also made available for recording purposes.

The CONF-T-512 | CONF-P 96/148 is based upon the Texas Instruments TMS320C6454 DSP, combined with Adaptive Digital's VoIP firmware and host processor API software.

NOTE

In addition to the conferencing feature, the conferencing chip provides tone detection and tone generation capabilities. Tone detection is typically used in a conference server to allow the user to enter a conference ID and password, or to perform other control functions. Tone generation is used to generate alerting signals.

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4 FUNCTIONAL DESCRIPTION

The TMS320TCI6452 DSP is a multicore device with large, on-chip shared memory, a DDR interface and Serial RapidIO for inter-DSP communications. Gigabit Ethernet is embedded for native connectivity to IP-based systems. The TCI6486 is ideal for high-density transcoding in mobile video distribution systems.

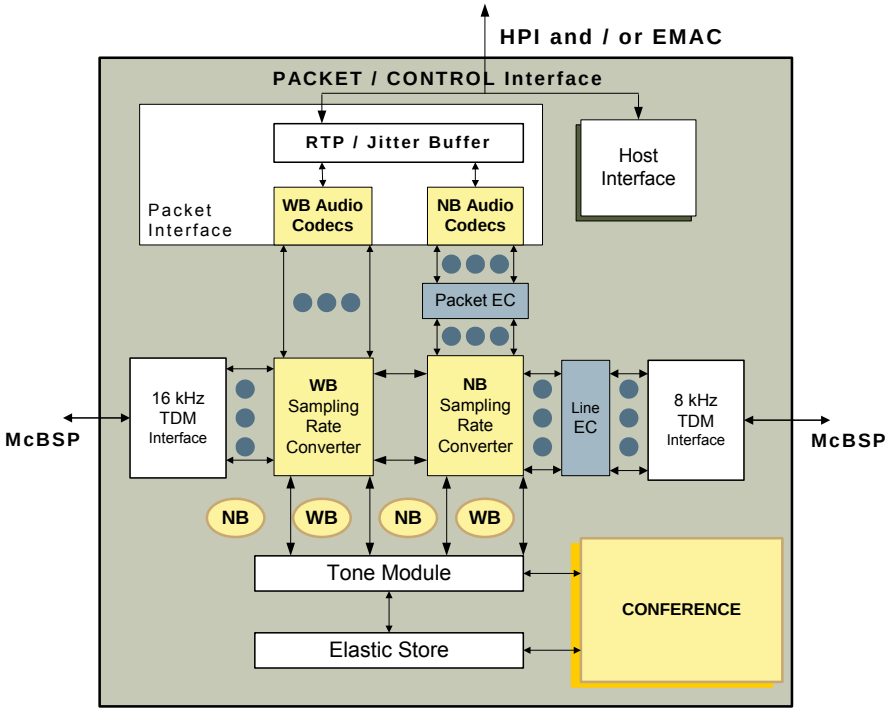

Figure 2: Chip Block Diagram

The conference chip is controlled via the DSP's Host Port Interface (HPI) and or Ethernet Interface. In order to simplify the use of the conferencing chip, the conferencing chip's ANSI "C" API software resides on the host processor. This API provides an abstraction layer that hides the details of the control mechanisms from the host application.

Figure 2 is a block diagram of a mixed narrowband/wideband VoIP conference system on a chip. The packet interface block handles RTP, jitter buffering, and both narrowband and wideband speech encode and decode functions. The packet echo canceller cancels echo that may be present on the opposite side of the packet network for narrowband channels only. It is assumed that wideband channels use four-wire interfaces at the far-end and therefore have no hybrid echo. Using a similar argument, there is a line echo canceller connected to the narrowband (8 kHz) TDM interface, but not to the wideband (16 kHz) TDM interface.

The sampling rate converters perform sampling rate conversion with appropriate filtering on narrowband and wideband signals which include both PCM and packet channels.

The elastic store is a buffering mechanism that compensates for possible varying frame sizes in the packet channels.

The conference module performs the actual conferencing - including voice activity detection, noise suppression, dominant speaker identification, AGC, and conference summation.

4.1 Channel Type

4.1.1 TDM to Conference Channel Type (CONF-T / CONF-P)

TDM to conference channel types are used to allow analog telephones to join a conferencing call. These channels invoke two functions within a single processing thread as shown in **Figure 1**.

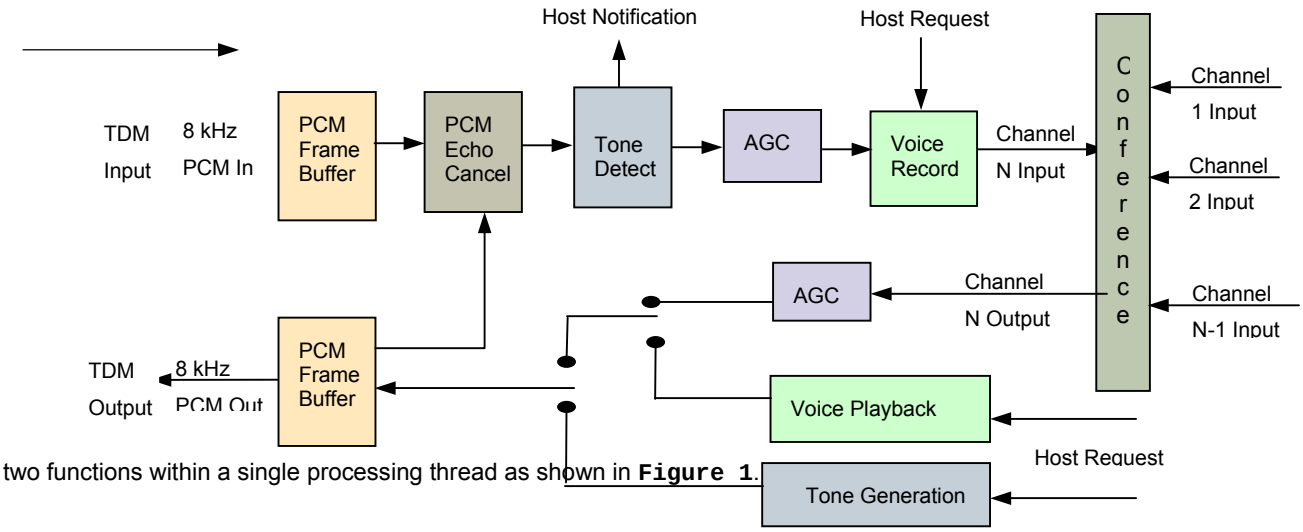

Figure 1 – Conference TDM Channel

Conference input. The conference input function inputs 8 kHz PCM samples from a TDM slot and buffers as many samples as needed for a frame used by the conference. When enough samples are buffered, the PCM data is optionally passed through PCM echo cancellation, tone detection and automatic gain control (AGC) algorithms before being passed to the Conferencing algorithm for use as one of the conference inputs. The PCM data can be recorded at the host's request for future playback.

Conference output. The conference output function buffers the conference's output data for the channel. Each channel has its own conference output data that removes a speaker's voice from his own output. The buffered samples are optionally passed through AGC and then output to a TDM slot. The host may override the TDM output with either a previously recorded message or a generated tone.

The pcm canceller and automatic gain control algorithms are independent options selectable at channel setup.

4.1.2 Packet to Conference Channel Type (CONF-P)

Packet to conference channel types allow digital telephones to join a conferencing call. These channels invoke two functions within a single thread of processing as shown in **Figure 2**.

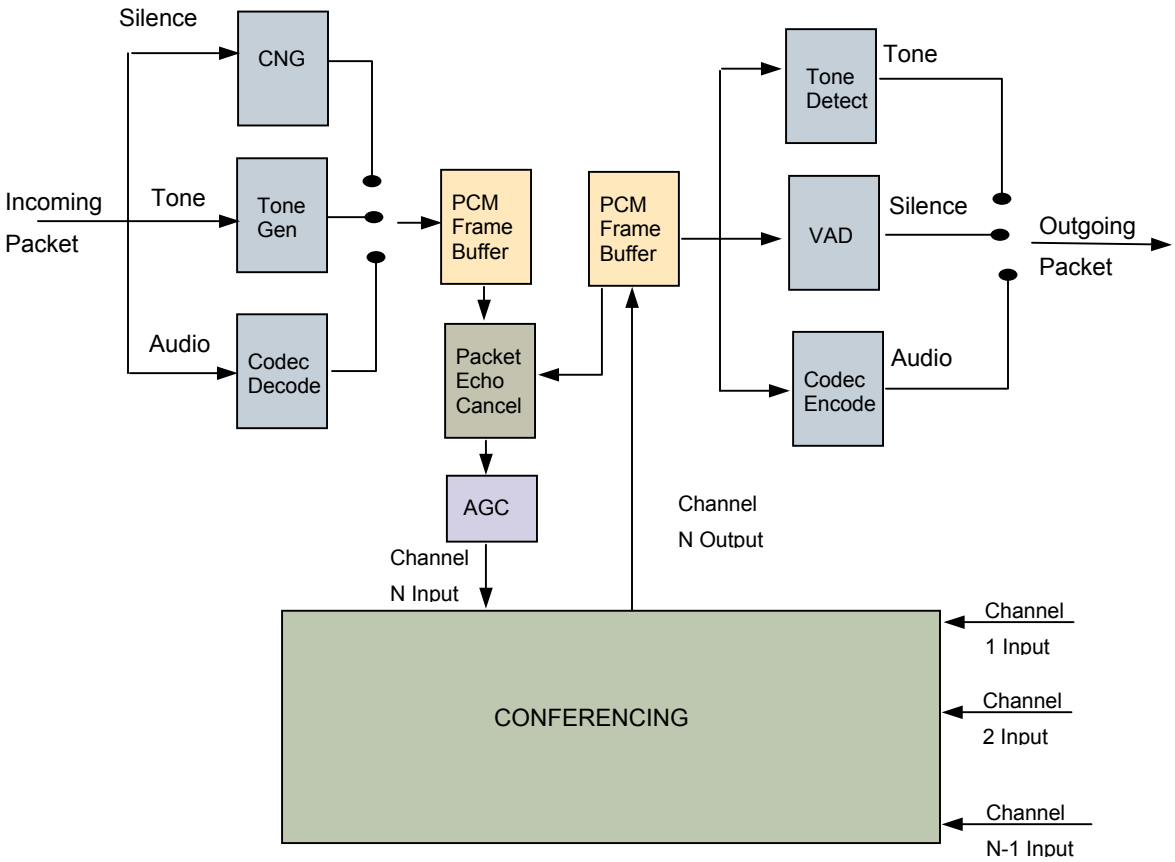

Figure 2 – Conference Packet Channel

Conference input. The conference input function reads a packet from the host control processor and generates PCM samples according to the received packet type. If a silence packet is received, comfort noise is generated. If a tone packet is received, the specified tone is generated. If an audio packet is received, it is decoded according to the input packet codec type.

The generated PCM samples are then optionally passed through the packet echo canceller and automatic gain control algorithms before being passed to the Conferencing algorithm for use as one of the conference inputs.

Conference output. The conference output function buffers the normalized sum of all conference member's input data minus the channel's own input data. The samples are buffered until there are enough samples to build an output frame. When enough samples are buffered, the samples are optionally passed through the tone detector (TD) and the voice activity detector (VAD).

G.PAK notifies the host at the start and end of each tone. If tone relay is enabled, tone packets are generated for each frame until the tone ends; an end of tone packet is generated when the tone stops.

Voice activity detection is optionally performed when no tone is detected. A silence packet is generated when VAD does not detect voice activity,

Voice encoding is performed whenever tone or silence packets are NOT generated. The channel's encoder type identifies which vocoder will be used. The vocoder output is formatted and packed into the vocoder's packet payload and sent to the host for transmission.

The packet echo canceller, tone detection, tone relay, voice activity detection, and automatic gain control algorithms are independent options selectable at channel setup. Input packets are read and output packets are generated with the same frequency as the conference's frame size.

5 CONF-T APIs

The **CONF- T/ P** APIs are the interface between a user's application program and **CONF- T/ P** DSP cores. The APIs execute in a host control processor connected to the DSP via the DSP's Host Port Interface (HPI). The APIs support multiple DSP cores and use a DSP Identifier to select a particular core. The association between a DSP Identifier and a particular DSP core is made by the user modified **CONF-T/ P** support functions.
In order to simplify the use of the conferencing chip, the conferencing chip's ANSI "C" API software resides on the host processor. This API provides an abstraction layer that hides the details of the control mechanisms from the host application.

The APIs are provided as ANSI "C" source code.

6 REFERENCES

1. Adaptive Digital Technologies G.PAK Users Guide
2. Texas Instruments TMS320C6424 Fixed-Point Digital Signal Processor (literature number SPRS347C)
3. Texas Instruments TMS320C6455 Fixed-Point Digital Signal Processor (literature number SPRS276H)
4. Texas Instruments TMS320C648x Digital Signal Processor (literature number SPRU894D)

Adaptive Digital is a strategic member of the Texas Instruments Developer Network.

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