TI C6446 CACHE NOTES

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Adaptive Digital Technologies specifies algorithm MIPS requirements based upon the peak utilization when all code and data are placed in their ideal locations in internal RAM. In some circumstances, for high-density applications it is not possible to fit in all the program and data internally due to internal RAM size limitations. For example, the 'C6446 only has 64 KB of L2 RAM, but it support big external DDR2 memory.

When using external RAM for code or data, each instruction, load, or save requires more cycles than the case where code or data resides in internal RAM. This is caused by the time it takes to access the external RAM and the latency through the DSP's EMIF (External Memory Interface). On the 'C6446, the situation is even worse because these devices have a flaw in their EMIF design that results in even more lost cycles. (This is not the case for other 'C55X devices that have I-Caches).

Fortunately, the 'C6446 has an on-chip two-level cache, a dedicated program(L1P) and a dedicated data memory(L1D) on the first level, and L2 memory. Once instructions or data are loaded from external RAM into cache, they can execute at full speed until bumped out of cache.

Characterizing the performance of an algorithm when portions are running from external RAM is not straightforward. We have run some tests using the Echo Canceller algorithm and DTMF Detectors as examples to show the effect of using external RAM for code and data as well as the effect of the I-Cache. The results are listed in the table below for the 'C6446. Noted here, L1P cache (32KB) is always enabled during the test.

Single channel test and L1P 32KB is enabled

Test #	Code	Per Chan Data	L2 Cache(64KB)	Peak Cycles	Peak MIPS	Average Cycles	Average MIPS
1	Internal	Internal	N/A	35847	3.58	33602	3.36
2	External	Internal	Off	58130	5.8	40731	4.07
3	External	External	Off	1905345	190	1628503	160
4	External	Internal	On	43859	4.38	34704	3.47
5	External	External	On	45469	4.54	35161	3.51

Table 1: Echo Canceller MIPS as a function of memory placement

The results show a number of things.

1. The L1P is very effective. If we compare test 2 with test 1 in Table 1, for example, the L1P Cache will help the MIPS number even when we put all EC program externally. The average MIPS goes up from 3.36 to 4.07, which is not big jump.

2. Placing data sections externally without enabling L2Cache will cause huge MIPS hit. We can see this fact by looking at the test 3, the average MIPS soars up to 160, which is about 50 times more than internal memory MIPS number!
3. Enabling L2 Cache is a simple way to bring the MIPS down, even with data sections being placed out of chip. Test 4 and test 5indicate the average MIPS numbers are close to the internal memory version. But the maximum MIPS number jumps from 3.58 to 4.54, due to the cache in/cache out overhead.

When multiple channels and multiple algorithms come into the picture, the cache performance would not be characterized as easy as single channel case. With more code and data sections bumped in and out of cache, the MIPS number would not be a linear prediction. The next 120-channel Echo Canceller plus DTMF detector test shows more interesting result. We already draw a conclusion that the L2 cache would help to bring down the cycles when we pace data externally, so in the following test, we would enable both L1P and L2 cache.

Test #	Code	Per Chan Data	L2 Cache(64KB)	Peak MIPS	Average MIPS	Per Chan Average MIPS
120-channels EC only	External	External	On	591.6	560.4	4.6
120-channels EC+DTMF	External	Internal	On	637.2	600.7	5.0

From above table, we can see that, with 120 channels running, the average MIPS increased from 3.5 to 4.5. The maximum MIPS number is even bigger, since the multiple echo canceller channels and two sets of the algorithm compete cache memory.

Conclusions

1. A good compromise is placing code in external RAM to use L1P and data in internal RAM.
2. Enable L2 cache if it's not possible to place data internally.
3. If simply enabling L2 cache can't bring the MIPS down to the goal, especially for the very high-density application, we can place per channel data externally, then DMA the data into internal RAM in advance of when the channel data will be needed. Since DMA operations can be done with nearly no overhead, this technique can be used to preserve even more precious internal RAM.

Further Reading

1. TMS320C64+ DSP Megamodule Reference Guide, SPRU871. Texas Instruments, Inc. Oct, 2006.
2. TMS320C64+ DSP Cache User's Guide, SPRU862. Texas Instruments, Inc. Oct, 2006