# TONE RELAY Signaling Tone

## PRODUCT DESCRIPTION

Adaptive Digital's Tone Relay is a carrier class Signaling Tone passer that provides exceptional channel densities. The ADT Signaling Tone Relay detects Signaling tones such as DTMF, MF R1, R2 Forward, R2 Reverse, Call Progress signals, passes coded tone information to the other end of the channel, and regenerates signaling tones. Adaptive Digital's proprietary algorithm is robust enough to meet Bellcore GR-506, and ITU Q455 recommendations while using few CPU cycles and has a low memory requirement.

A DTMF suppressor is included to suppress DTMF tones in Voice-Over-Packet systems that employ tone passing via out-of-band signaling. This is useful when a low rate speech compression algorithm is unable to pass the DTMF tones without significant distortion. Other signaling tone types are muted, as they do not occur along with speech signals.

### *FEATURES*

- Meets Bellcore GR506, ITU Q455 specifications
- Robust detection
- Low per-channel memory requirements
- Low false alarm rate
- C-callable
- Designed for multi-channel operation
- Programmable Frame Size

## AVAILABILITY

ADT AEC is available on the following Platforms: Other configurations are available upon request.

| Product | Platform | Memory Model | Endian | Code Gen Tool Version |
|---|---|---|---|---|
| ADT_TR_c54x | TI TMS320C54x | Far | N/A | N/R |
| ADT_TR_c55x | TI TMS320C55x | Large | Little | N/R |
| ADT_TR_c64x**p** | TI TMS320C64x+ | Mml3 | Little | CC6_1_15 |
| ADT_TR_c64x | TI TMS320C64x | Mml3 | Little | CC6_1_15 |

Endian, byte order: "Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

Acronyms

Mm – Memory Model: Memory Model is specific to Texas Instruments processors.

## SPECIFICATIONS

# TI TMS320

## C54x

### CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of 16-bit word.

| Function | MIPS Per Channel | Program Memory | Data Memory | Per-Channel Data Memory | MIPS Per Channel | Program Memory | Data Memory | Per-Channel Data Memory |
|---|---|---|---|---|---|---|---|---|
| TRDetect | 1.81 | 689 | 16 | 40 | 0.66 | 1609 | 207+ | 48 |
| TRGenerator | 0.41 | 2361 | 384 | 39 | 0.38 | 383 | 227+ | 28 |
| DTMF | --[1] | 607 | 40 | 55 | --[1] | 601 | 1704 | 72 |
| MFR1 | 0.69[1] | 587 | 66 | 55 | 0.3[1] | 598 | 1626 | 72 |
| MFR2_F | 0.92[1] | 551 | 60 | 55 | 0.3[1] | 492 | 828 | 72 |
| MFR2_R | 0.92[1] | 551 | 60 | 55 | 0.3[1] | 492 | 828 | 72 |
| Cprg | 0.55[1] | 610 | 32 | 55 | 0.3[1] | 576 | 1496 | 72 |
| Detector Common | -- | 689 | 16 | -- | -- | 597 | 16 | -- |

[1] the detector MIPS (TRDetect) include the DTMF detector MIPS. When other detectors are enabled, the total TRDetect MIPS increases by the amount indicated.

+ 207 words are shared between detector and generator library

## C55x

### CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of byte.

| Function | *MIPS Per Channel* | Program Memory | Data Memory | Per-Channel Data Memory |
|---|---|---|---|---|
| ToneRelay Detector | 0.57 | 2636 | -- | 120 |
| ToneRelay Generator | 0.28 | 519 | 40 | 56 |
| ToneRelay Common | -- | 671 | 400 | -- |
| DTMF | -- | 1311 | 3412 | 152 |
| MFR1 | -- | 1228 | 3256 | 152 |
| MFR2_F | -- | 1133 | 1660 | 152 |
| MFR2_R | -- | 1133 | 1660 | 152 |
| Cprg | -- | 1290 | 2996 | 152 |
| Tone Detector Common | -- | 1369 | 32 | -- |

Note: The MIPS (Detector + Regenerator) estimation was done when only DTMF signals were looked for. Adding other tone types adds 0.3MIPS approx. to the detector part. However the generator MIPS remain the same.

*Specifications C6000x Cont'd -*

## C64XP - *(C64x+)*

### CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

| Function | MIPS | Program Memory | Data Memory | Scratch | Per Channel Data Memory | Stack | Heap-Persistent | Heap - Scratch |
|---|---|---|---|---|---|---|---|---|
| TR_ADT_relayDetect | 1.2 | 13504 | 1036 | 0 | 356 | 256 | 0 | 0 |
| TR_ADT_relayGenerate | .15 | | | 0 | 75 | 256 | 0 | 0 |

Notes:

1. These specifications do not include requirements for the underlying detectors (DTMF, MF, etc.)
2. These specifications assume that suppression delay is not being used

We specify MIPS (Millions of Instructions Per Second) as MCPS (Millions of Instruction Cycles Per Second). Unless otherwise specified, peak MIPS are indicated.

## C64X

### CPU UTILIZATION & MEMORY REQUIREMENTS

All Memory usage is given in units of bytes.

| Function | MIPS | Program Memory | Data Memory | Scratch | Per Channel Data Memory | Stack | Heap-Persistent | Heap - Scratch |
|---|---|---|---|---|---|---|---|---|
| TR_ADT_relayDetect | 1.2 | 16064 | 1036 | 0 | 356 | 256 | 0 | 0 |
| TR_ADT_relayGenerate | .15 | | | 0 | 75 | 256 | 0 | 0 |

### FUNCTIONS

```
TR_ADT_detectInit (. . .)           Initializes tone relay detector

TR_ADT_generateInit (. . .)         Initializes tone relay generator

TR_ADT_detect (. . .)               erform tone relay detect

TR_ADT_getLastDetectResults (. . .) Retrieve latest tone relay detect result

TR_ADT_sendNewEventToGenerator(. . .) Send a new tone event to the tone relay
                                    generator

TR_ADT_generator(. . .)             Perform tone relay generate
```

*Deliverables*

The deliverable items are platform dependent. In general, there is one library. (Sometimes multiple variants of the library are included in the deliverables.) There are also header files, some of which are specific to the product and others are common across many of Adaptive Digital's products. Also included in the deliverables is product documentation, which includes a users guide and usually includes release notes and a data sheet. Sample/test code may be included as well.

*Adaptive Digital is a member of the Texas Instruments Developer Network, and ARM Connected Community.*

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