AT45DBxxxE DataFlash®: SRAM Buffer Read Feature Description

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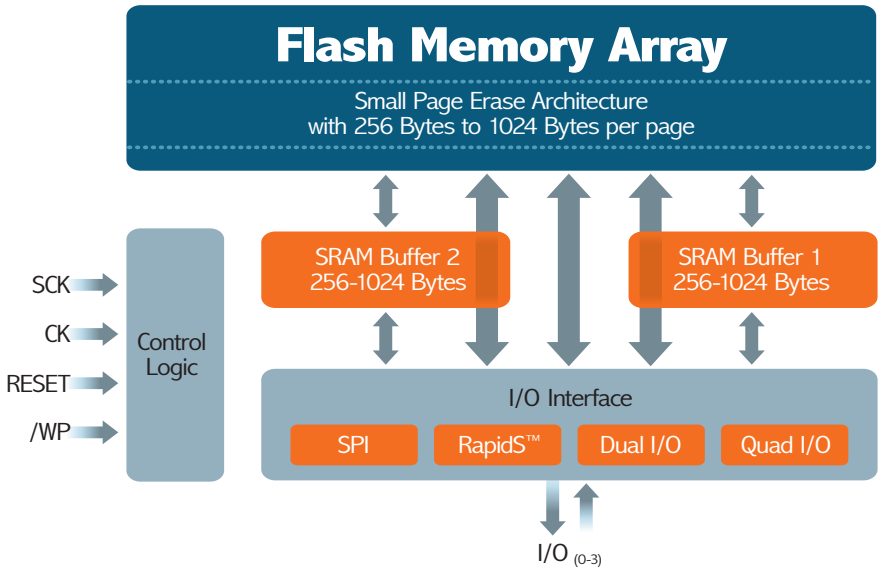
Introduction

The next generation of Adesto AT45DBxxxE series DataFlash devices are a family of enhanced feature rich SPI Serial Flash products that will contribute to improved system performance and lower energy consumption. The design philosophy behind these products has been focused on enhanced system performance and operation whilst contributing to a reduced energy consumption footprint. Figure 1 below shows a top level view of the DataFlash architecture and Dual SRAM buffers.

Figure 1. AT45DBxxxE Structure Block Diagram



Features

All DataFlash memories come with on chip SRAM buffer(s) to provide system design flexibility.The different number of buffers and various buffers sizes are shown in Table 1 below:

Table 1. Buffer Sizes

Root Part Number	Density	Number of Buffers	Standard (Default Page Size)	Binary (Power-of-2) Page Size
AT45DB021E	2Mbit	1	264 Bytes	256 Bytes
AT45DB041E	4Mbit	2	264 Bytes	256 Bytes
AT45DB081E	8Mbit	2	264 Bytes	256 Bytes
AT45DB161E	16Mbit	2	528 Bytes	512 Bytes
AT45DB321E	32Mbit	2	528 Bytes	512 Bytes
AT45DB641E	64Mbit	2	264 Bytes	256 Bytes

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These SRAM buffers can be used in many ways, supporting read, write and data buffering operations. In addition when the SRAM buffers are not required by the DataFlash itself they can be used as additional sequential access system SRAM. These SRAM buffers can be considered additional resources for system designers.

Software and Hardware Designers can:

- Continuously write to the memory. For example, with no interruption of streaming of data.
- Use the SRAM as the additional high speed memory.
- Temporary data storage for frequently changed data. No need to erase before write.
- Can write to or read from SRAM with no endurance cycle limitation.
- Reduce or eliminate expensive external SRAM memory for cost reduction.

Refer to the Appendix 1 and 2 for the available buffer commands. Note that the AT45DB021E, 2Mbit device is a single buffer device where as all other devices have two SRAM buffers. As a result, AT45DB021E does not offer the commands for Buffer 2.

How to read from the buffers

D1h and D4h are the commands to read from buffers. With these two commands, system can read from either of the buffers at any time.

However, **during erase or program operation on the memory array**, all buffer reads should be completed before the erase operation or program operation is completed.

Appendix 1.

Table 2. Read Commands for AT45DB021E

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Buffer Read (Low Frequency)	D1h
Buffer Read (High Frequency)	D4h

Table 3. Read Commands for AT45DB041E, AT45DB081E, AT45DB161E, AT45DB321E, AT45DB641E

Command	Opcode
Main Memory Page Read	D2h
Continuous Array Read (Low Power Mode)	01h
Continuous Array Read (Low Frequency)	03h
Continuous Array Read (High Frequency)	0Bh
Continuous Array Read (High Frequency)	1Bh
Continuous Array Read (Legacy Command – Not Recommended for New Designs)	E8h
Buffer 1 Read (Low Frequency)	D1h
Buffer 2 Read (Low Frequency)	D3h
Buffer 1 Read (High Frequency)	D4h
Buffer 2 Read (High Frequency)	D6h

Appendix 2.

Table 4. Program and Erase Commands for AT45DB021E

Command	Opcode
Buffer Write	84h
Buffer to Main Memory Page Program with Built-In Erase	83h
Buffer to Main Memory Page Program without Built-In Erase	88h
Main Memory Page Program through Buffer with Built-In Erase	82h
Main Memory Byte/Page Program through Buffer without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah

Table 5. Program and Erase Commands for AT45DB041E, AT45DB081E, AT45DB161E, AT45DB321E, AT45DB641E

Command	Opcode
Buffer 1 Write	84h
Buffer 2 Write	87h
Buffer 1 to Main Memory Page Program with Built-In Erase	83h
Buffer 2 to Main Memory Page Program with Built-In Erase	86h
Buffer 1 to Main Memory Page Program without Built-In Erase	88h
Buffer 2 to Main Memory Page Program without Built-In Erase	89h
Main Memory Page Program through Buffer 1 with Built-In Erase	82h
Main Memory Page Program through Buffer 2 with Built-In Erase	85h
Main Memory Byte/Page Program through Buffer 1 without Built-In Erase	02h
Page Erase	81h
Block Erase	50h
Sector Erase	7Ch
Chip Erase	C7h + 94h + 80h + 9Ah
Program/Erase Suspend	B0h
Program/Erase Resume	D0h

Adesto Technologies
Headquarters

1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: (+1) 408.400.0578
Email:contact@adestotech.com
Web: http://www.adestotech.com

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