# AT45DB041D and AT45DB041E Comparison

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# AT45DB041D and AT45DB041E Comparison

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# AT45DB041E Differences Highlight – Items require Software Change

Conversion from AT45DB041D to AT45DB041E

- ✓ Command set: No change
- ✓ Product ID: Now with 5 bytes. No change on the first 3 bytes
- ✓ Chip Erase Time: Change from 12sec to 17sec
- ✓ Status Register: Now with two bytes. No change on the first byte

# AT45DB041D and AT45DB041E Comparison

AT45DB041E is designed to replace the AT45DB041D in the 8 pin packages. While it maintains the fine granular structure, it also introduces a few new features.

- ✓ Improved Deep Power Down mode – 4.5µA (typical)
- ✓ Ultra-Deep Power Down mode – 400nA
- ✓ Low Power Read mode
- ✓ User configurable and re-configurable page size (256bytes or 264bytes)
- ✓ Program / Erase Suspend and Resume
- ✓ New max operating clock frequency at 104MHz (command 1Bh)
- ✓ Wider operating voltage range: 1.65V – 3.6V
- ✓ Allows Software Reset
- ✓ Now with 5 Bytes Device ID

# AT45DB041D and AT45DB041E Comparison

## AT45DB041D

- Single 2.5V or 2.7V to 3.6V Supply
- RapidS™ Serial Interface: 66MHz Maximum Clock Frequency
  - SPI Compatible Modes 0 and 3
- User Configurable Page Size
  - 256-Bytes per Page
  - 264-Bytes per Page
  - Page Size Can Be Factory Pre-configured for 256-Bytes
- Page Program Operation
  - Intelligent Programming Operation
  - 2,048 Pages (256-/264-Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (256-Bytes)
  - Block Erase (2-Kbytes)
  - Sector Erase (64-Kbytes)
  - Chip Erase (4Mbits)
- Two SRAM Data Buffers (256-, 264-Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 7mA Active Read Current Typical
  - 25µA Standby Current Typical
  - 15µA Deep Power-down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier

## AT45DB041E

- Single 1.65V - 3.6V supply — New
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports RapidS™ operation
- Continuous read capability through entire array — New
  - Up to 85MHz
  - Low-power read option up to 20MHz
  - Clock-to-output time ($t_V$) of 6ns maximum
- User configurable page size
  - 256 bytes per page
  - 264 bytes per page (default)
  - Page size can be factory pre-configured for 256 bytes
- Two fully independent SRAM data buffers (256/264 bytes)
  - Allows receiving data while reprogramming the main memory array
- Flexible programming options — New
  - Byte/Page Program (1 to 256/264 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase (256/264 bytes)
  - Block Erase (2KB)
  - Sector Erase (64KB)
  - Chip Erase (4-Mbits)
- Program and Erase Suspend/Resume — New
- Advanced hardware and software data protection features
  - Individual sector protection
  - Individual sector lockdown to make any sector permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low-power dissipation
  - 500nA Ultra-Deep Power-Down current (typical) — New
  - 3µA Deep Power-Down current (typical)
  - 25µA Standby current (typical at 20MHz) — New
  - 11mA Active Read current (typical)

# AT45DB041E Features not recommended for new design

**These commands are supported, but recommended not to use in new design**

| Commands | AT45DB041D | AT45DB041E |
|---|---|---|
| Buffer 1 Read | 54H | 54H |
| Buffer 2 Read | 56H | 56H |
| Main Memory Page Read | 52H | 52H |
| Continuous Array Read | 68H | 68H |
| Status Register Read | 57H | 57H |
| Continuous Array Read (Legacy Command – Not Recommended for New Designs) | E8H | E8h |

# AT45DB041E Command Set Comparison

| Commands | AT45DB041D | AT45DB041E |
|---|---|---|
| Buffer 1 Read (High Frequency) | D4H | D4h |
| Buffer 1 Read (Low Frequency) | D1H | D1h |
| Buffer 2 Read (High Frequency) | D6H | D6h |
| Buffer 2 Read (Low Frequency) | D3H | D3h |
| Continuous Array Read (High Frequency) | 0BH | 0Bh |
| Continuous Array Read (High Frequency) | | 1Bh |
| Continuous Array Read (Low Frequency) | 03H | 03h |
| Continuous Array Read (Low Power Mode) | | 01h |
| Main Memory Page Read | D2H | D2h |
| | | |
| Block Erase | 50H | 50h |
| Buffer 1 to Main Memory Page Program with Built-In Erase | 83H | 83h |
| Buffer 1 to Main Memory Page Program without Built-In Erase | 88H | 88h |
| Buffer 1 Write | 84H | 84h |
| Buffer 2 to Main Memory Page Program with Built-In Erase | 86H | 86h |
| Buffer 2 to Main Memory Page Program without Built-In Erase | 89H | 89h |
| Buffer 2 Write | 87H | 87h |
| Chip Erase | C7H, 94H, 80H, 9AH | C7h + 94h + 80h + 9Ah |
| Main Memory Byte/Page Program through Buffer 1 without Built-In Erase | | 02h |
| Main Memory Page Program through Buffer 1 with Built-In Erase | 82H | 82h |
| Main Memory Page Program through Buffer 2 with Built-In Erase | 85H | 85h |
| Page Erase | 81H | 81h |
| Program/Erase Resume | | D0h |
| Program/Erase Suspend | | B0h |
| Sector Erase | 7CH | 7Ch |

New

New

New

New

# AT45DB041E Command Set Comparison

| Commands | AT45DB041D | AT45DB041E | |
|---|---|---|---|
| Enable Sector Protection | 3DH + 2AH + 7FH + A9H | 3Dh + 2Ah + 7Fh + A9h | |
| Disable Sector Protection | 3DH + 2AH + 7FH + 9AH | 3Dh + 2Ah + 7Fh + 9Ah | |
| Erase Sector Protection Register | 3DH + 2AH + 7FH + CFH | 3Dh + 2Ah + 7Fh + CFh | |
| Program Sector Protection Register | 3DH + 2AH + 7FH + FCH | 3Dh + 2Ah + 7Fh + FCh | |
| Read Sector Protection Register | 32H | 32h | |
| Sector Lockdown | 3DH + 2AH + 7FH + 30H | 3Dh + 2Ah + 7Fh + 30h | |
| Read Sector Lockdown Register | 35H | 35h | |
| Freeze Sector Lockdown | | 34h + 55h + AAh + 40h | New |
| Program Security Register | 9BH + 00H + 00H + 00H | 9Bh + 00h + 00h + 00h | |
| Read Security Register | 77H | 77h | |
| Main Memory Page to Buffer 1 Transfer | 53H | 53h | |
| Main Memory Page to Buffer 2 Transfer | 55H | 55h | |
| Main Memory Page to Buffer 1 Compare | 60H | 60h | |
| Main Memory Page to Buffer 2 Compare | 61H | 61h | |
| Auto Page Rewrite through Buffer 1 | 58H | 58h | |
| Auto Page Rewrite through Buffer 2 | 59H | 59h | |
| Deep Power-Down | B9H | B9h | |
| Resume from Deep Power-Down | ABH | ABh | |
| Ultra-Deep Power-Down | | 79h | New |
| Status Register Read | D7H | D7h | |
| Configure “Power of 2” (Binary) Page Size | 3Dh + 2Ah + 80h + A6h | 3Dh + 2Ah + 80h + A6h | |
| Configure Standard DataFlash Page Size | | 3Dh + 2Ah + 80h + A7h | New |
| Software Reset | | F0h + 00h + 00h + 00h | |

# AT45DB041E Command Set Comparison

## AT45DB041E New 5-byte Manufacturer ID

| Commands | AT45DB041D | AT45DB041E |
|---|---|---|
| Manufacturer and Device ID Read | 9FH | 9Fh |
| Manufacturer ID | 1Fh | 1Fh |
| Device ID (Byte 1) | 24h | 24h |
| Device ID (Byte 2) | 00h | 00h |
| [Optional to Read] Extended Device Information (EDI) String Length | 00h | 01h |
| [Optional to Read] EDI Byte 1 | | 00h |

New

# AT45DB041D and AT45DB041E – Program / Erase Time

AT45DB041D

| Symbol | Parameter | AT45DB041D (2.5V Version) Min | Typ | Max | AT45DB041D Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{EP}$ | Page Erase and Programming Time (256/264 bytes) | | 14 | 35 | | 14 | 35 | ms |
| $t_P$ | Page Programming Time (256-/264-bytes) | | 2 | 4 | | 2 | 4 | ms |
| $t_{PE}$ | Page Erase Time (256-/264-bytes) | | 13 | 32 | | 13 | 32 | ms |
| $t_{BE}$ | Block Erase Time (2,048-/2,112-bytes) | | 30 | 75 | | 30 | 75 | ms |
| $t_{SE}$ | Sector Erase Time (65,536-/67,584-bytes) | | 0.7 | 1.3 | | 0.7 | 1.3 | s |
| $t_{CE}$ | Chip Erase Time | | 5 | 12 | | 5 | 12 | s |

AT45DB041E

| Symbol | Parameter | 1.65V to 3.6V Typ | Max | 2.3V to 3.6V Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{EP}$ | Page Erase and Programming Time (256/264 bytes) | 10 | 25 | 15 | 25 | ms |
| $t_P$ | Page Programming Time | 1.5 | 3 | 1.5 | 3 | ms |
| $t_{BP}$ | Byte Programming Time | 8 | | 8 | | µs |
| $t_{PE}$ | Page Erase Time | 12 | 25 | 12 | 25 | ms |
| $t_{BE}$ | Block Erase Time | 30 | 35 | 30 | 35 | ms |
| $t_{SE}$ | Sector Erase Time | .7 | 1.1 | .7 | 1.1 | s |
| $t_{CE}$ | Chip Erase Time | 6 | 17 | 5 | 17 | s |

# AT45DB041D and AT45DB041E – Program / Erase Current

## AT45DB041D

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DP}$ | Deep Power-down Current | $\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = $V_{IH}$, all inputs at CMOS levels | | 15 | 25 | µA |
| $I_{SB}$ | Standby Current | $\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = $V_{IH}$, all inputs at CMOS levels | | 25 | 50 | µA |
| $I_{CC1}$ | Active Current, Read Operation | f = 20MHz; $I_{OUT}$ = 0mA; $V_{CC}$ = 3.6V | | 7 | 10 | mA |
| | | f = 33MHz; $I_{OUT}$ = 0mA; $V_{CC}$ = 3.6V | | 8 | 12 | mA |
| $I_{CC2}$ | Active Current, Program/Erase Operation | $V_{CC}$ = 3.6V | | 12 | 17 | mA |

## AT45DB041E

| | | | 1.65V to 3.6V | | | 2.3V to 3.6V | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Condition | Min | Typ | Max | Min | Typ | Max | Units |
| $I_{UDPD}$ | Ultra-Deep Power-Down Current | All inputs at 0V or $V_{CC}$ | | 0.4 | 1 | | 0.4 | 1 | µA |
| $I_{SB}$ | Standby Current | $\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = $V_{IH}$ All inputs at CMOS levels | | 25 | 40 | | 25 | 40 | µA |
| $I_{CC1}$ | Active Current, Low Power Read (01h) Operation | f = 1MHz; $I_{OUT}$ = 0mA; $V_{CC}$ = 3.6V | | 6 | 9 | | 6 | 9 | mA |
| | | f = 15MHz; $I_{OUT}$ = 0mA; $V_{CC}$ = 3.6V | | 7 | 10 | | 7 | 10 | mA |
| $I_{CC3}$ | Active Current, Program Operation | $\overline{CS}$=$V_{CC}$ | | 14 | 16 | | 14 | 16 | mA |
| $I_{CC4}$ | Active Current, Erase Operation | $\overline{CS}$=$V_{CC}$ | | 8 | 12 | | 8 | 12 | mA |

# AT45DB041E – New 2-byte Status Register

## Status Register Read

The 2-byte Status Register can be used to determine the device's ready/busy status, page size, a Main Memory Page to Buffer Compare operation result, the sector protection status, Freeze Sector Lockdown status, erase/program error status, Program/Erase Suspend status, and the device density. The Status Register can be read at any time, including during an internally self-timed program or erase operation.

To read the Status Register, the $\overline{CS}$ pin must first be asserted and then the opcode D7h must be clocked into the device. After the opcode has been clocked in, the device will begin outputting Status Register data on the SO pin during every subsequent clock cycle. After the second byte of the Status Register has been clocked out, the sequence will repeat itself, starting again with the first byte of the Status Register, as long as the $\overline{CS}$ pin remains asserted and the clock pin is being pulsed. The data in the Status Register is constantly being updated, so each repeating sequence may output new data. The RDY/$\overline{BUSY}$ status is available for both bytes of the Status Register and is updated for each byte.

Deasserting the $\overline{CS}$ pin will terminate the Status Register Read operation and put the SO pin into a high-impedance state. The $\overline{CS}$ pin can be deasserted at any time and does not require that a full byte of data be read.

**Table 9-1. Status Register Format – Byte 1**

| Bit | Name | | Type[1] | Description | |
|---|---|---|---|---|---|
| 7 | RDY/$\overline{BUSY}$ | Ready/Busy Status | R | 0 | Device is busy with an internal operation. |
| | | | | 1 | Device is ready. |
| 6 | COMP | Compare Result | R | 0 | Main memory page data matches buffer data. |
| | | | | 1 | Main memory page data does not match buffer data. |
| 5:2 | DENSITY | Density Code | R | 0111 | 4-Mbit |
| 1 | PROTECT | Sector Protection Status | R | 0 | Sector protection is disabled. |
| | | | | 1 | Sector protection is enabled. |
| 0 | PAGE SIZE | Page Size Configuration | R | 0 | Device is configured for standard DataFlash page size (264 bytes). |
| | | | | 1 | Device is configured for "power of 2" binary page size (256 bytes). |

Note: 1. R = Readable only

No change on the first byte

**Table 9-2. Status Register Format – Byte 2**

| Bit | Name | | Type[1] | Description | |
|---|---|---|---|---|---|
| 7 | RDY/$\overline{BUSY}$ | Ready/Busy Status | R | 0 | Device is busy with an internal operation. |
| | | | | 1 | Device is ready. |
| 6 | RES | Reserved for Future Use | R | 0 | Reserved for future use. |
| 5 | EPE | Erase/Program Error | R | 0 | Erase or program operation was successful. |
| | | | | 1 | Erase or program error detected. |
| 4 | RES | Reserved for Future Use | R | 0 | Reserved for future use. |
| 3 | SLE | Sector Lockdown Enabled | R | 0 | Sector Lockdown command is disabled. |
| | | | | 1 | Sector Lockdown command is enabled. |
| 2 | PS2 | Program Suspend Status (Buffer 2) | R | 0 | No program operation has been suspended while using Buffer 2. |
| | | | | 1 | A sector is program suspended while using Buffer 2. |
| 1 | PS1 | Program Suspend Status (Buffer 1) | R | 0 | No program operation has been suspended while using Buffer 1. |
| | | | | 1 | A sector is program suspended while using Buffer 1. |
| 0 | ES | Erase Suspend | R | 0 | No sectors are erase suspended. |
| | | | | 1 | A sector is erase suspended. |

New

Note: 1. R = Readable only

# AT45DB041E - Ultra-Deep Power Down

New

## Ultra-Deep Power-Down

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry. Since almost all active circuitry is shutdown in this mode to conserve power, the contents of the SRAM buffers cannot be maintained. Therefore, any data stored in the SRAM buffers will be lost once the device enters the Ultra-Deep Power-Down mode.

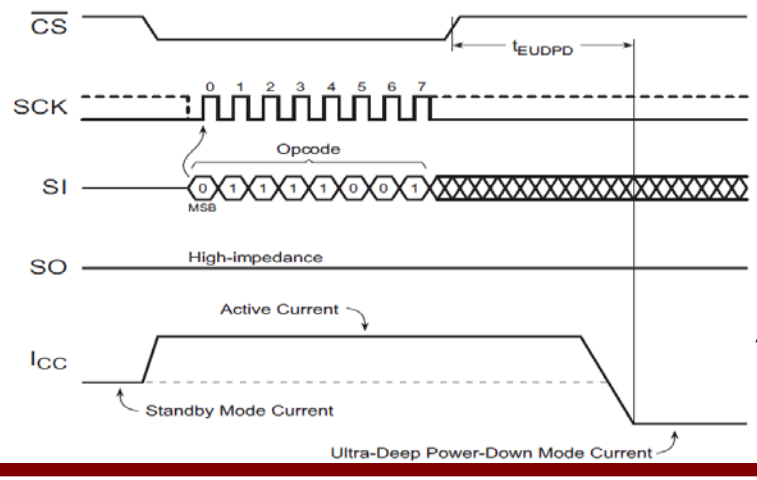
When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Ultra-Deep Power-Down mode within the maximum time of $t_{EUDPD}$.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle.

The Ultra-Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

**Figure 10-3. Ultra-Deep Power-Down**




Market Leading
Ultra-Deep Power Down

- 400nA (typ)
- 1µA (max)

# AT45DB041E - Exit Ultra-Deep Power Down

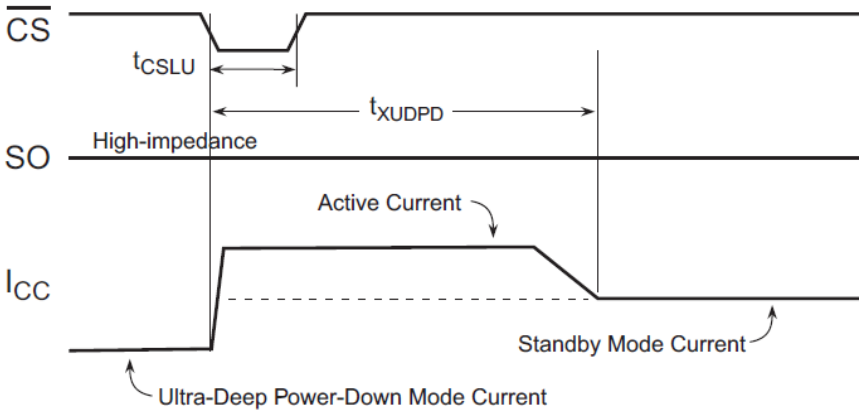
New

## Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the $\overline{CS}$ pin must simply be pulsed by asserting the $\overline{CS}$ pin, waiting the minimum necessary $t_{CSLU}$ time, and then deasserting the $\overline{CS}$ pin again. To facilitate simple software development, a dummy byte opcode can also be entered while the $\overline{CS}$ pin is being pulsed just as in a normal operation like the Program Suspend operation; the dummy byte opcode is simply ignored by the device in this case. After the $\overline{CS}$ pin has been deasserted, the device will exit from the Ultra-Deep Power-Down mode and return to the standby mode within a maximum time of $t_{XUDPD}$. If the $\overline{CS}$ pin is reasserted before the $t_{XUDPD}$ time has elapsed in an attempt to start a new operation, then that operation will be ignored and nothing will be performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

Since the contents of the SRAM buffers cannot be maintained while in the Ultra-Deep Power-Down mode, the SRAM buffers will contain undefined data when the device returns to the standby mode.

**Figure 10-4. Exit Ultra-Deep Power-Down**



# AT45DB041E – Freeze Sector Lockdown

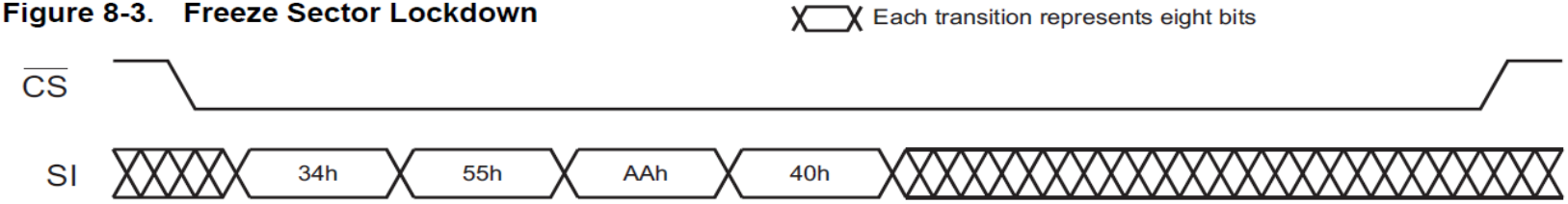
New

### Freeze Sector Lockdown

The Sector Lockdown command can be permanently disabled, and the current sector lockdown state can be permanently frozen so that no additional sectors can be locked down aside from those already locked down. Any attempts to issue the Sector Lockdown command after the Sector Lockdown State has been frozen will be ignored.

To issue the Freeze Sector Lockdown command, the $\overline{CS}$ pin must be asserted and the opcode sequence of 34h, 55h, AAh, and 40h must be clocked into the device. Any additional data clocked into the device will be ignored. When the $\overline{CS}$ pin is deasserted, the current sector lockdown state will be permanently frozen within a time of $t_{LOCK}$. In addition, the SLE bit in the Status Register will be permanently reset to a Logic 0 to indicate that the Sector Lockdown command is permanently disabled.

**Figure 8-3. Freeze Sector Lockdown**



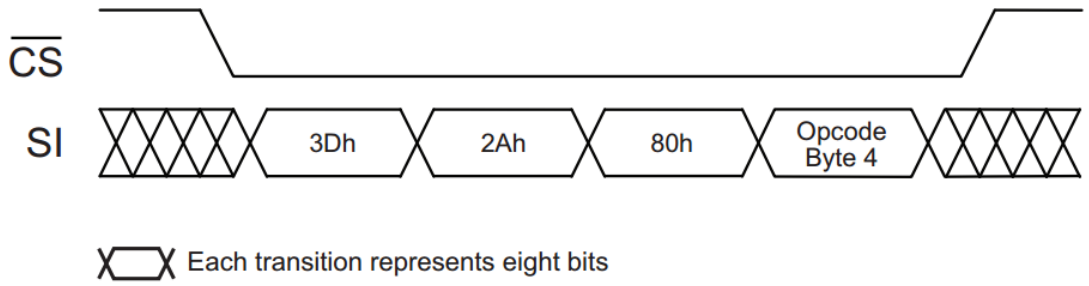
# AT45DB041E – page size re-configuration

New

**Table 11-1. Buffer and Page Size Configuration Commands**

| Command | Byte 1 | Byte 2 | Byte 3 | Byte 4 |
|---|---|---|---|---|
| “Power of 2” binary page size (256 bytes) | 3Dh | 2Ah | 80h | A6h |
| DataFlash page size (264 bytes) | 3Dh | 2Ah | 80h | A7h |

**Figure 11-1. Buffer and Page Size Configuration**




User can reconfigure as needed

# AT45DB041E – Software Reset

New

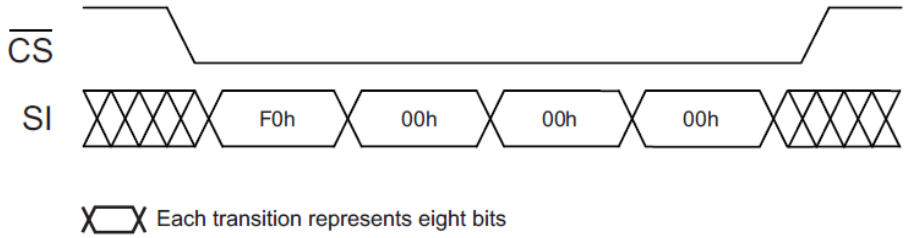
## Software Reset

In some applications, it may be necessary to prematurely terminate a program or erase cycle early rather than wait the hundreds of microseconds or milliseconds necessary for the program or erase operation to complete normally. The Software Reset command allows a program or erase operation in progress to be ended abruptly and returns the device to an idle state.

To perform a Software Reset, the $\overline{CS}$ pin must be asserted and a 4-byte command sequence of F0h, 00h, 00h, and 00h must be clocked into the device. Any additional data clocked into the device after the last byte will be ignored. When the $\overline{CS}$ pin is deasserted, the program or erase operation currently in progress will be terminated within a time $t_{SWRST}$. Since the program or erase operation may not complete before the device is reset, the contents of the page being programmed or erased cannot be guaranteed to be valid.

The Software Reset command has no effect on the states of the Sector Protection Register, the Sector Lockdown Register, or the buffer and page size configuration. The PS2, PS1, and ES bits of the Status Register, however, will be reset back to their default states. If a Software Reset operation is performed while a sector is erase suspended, the suspend operation will abort and the contents of the page or block being erased in the suspended sector will be left in an undefined state. If a Software Reset is performed while a sector is program suspended, the suspend operation will abort and the contents of the page that was being programmed and subsequently suspended will be undefined. The remaining pages in the sector will retain their previous contents.

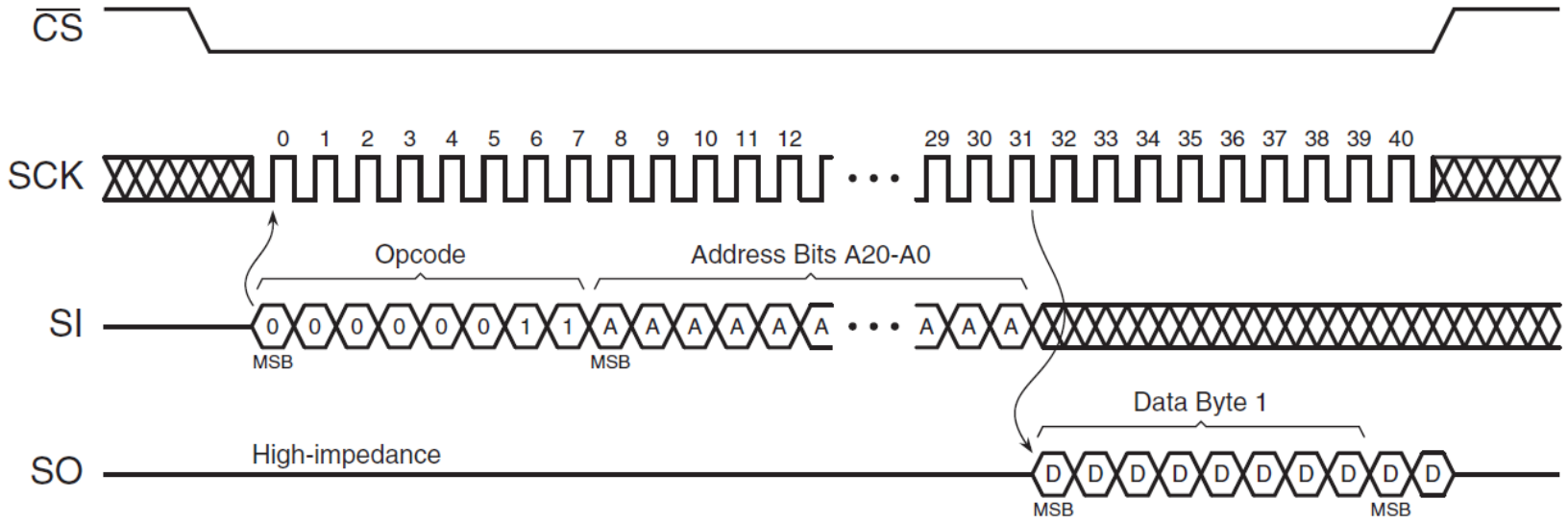
The complete 4-byte opcode must be clocked into the device before the $\overline{CS}$ pin is deasserted, and the $\overline{CS}$ pin must be deasserted on a byte boundary (multiples of eight bits); otherwise, no reset operation will be performed.



# AT45DB041E – Low Power Read Mode

New

**Continuous Array Read (Opcode 01h or 03h)**




**Lower Read Current:**

Command 01h:

6mA typ at 1MHz

7mA typ at 15MHz

# AT45DB041E – Program / Erase Suspend - Resume

New

## Program/Erase Suspend

In some code and data storage applications, it may not be possible for the system to wait the milliseconds required for the Flash memory to complete a program or erase cycle. The Program/Erase Suspend command allows a program or erase operation in progress to a particular 128KB sector of the main memory array to be suspended so that other device operations can be performed.

**Example:** By suspending an erase operation to a particular sector, the system can perform functions such as a program or read operation within a different 128KB sector. Other device operations, such as Read Status Register, can also be performed while a program or erase operation is suspended.

## Program/Erase Resume

The Program/Erase Resume command allows a suspended program or erase operation to be resumed and continue where it left off.

Note: Please refer to datasheet for the detail

# DataFlash DataSheets and Samples

DataFlash® Datasheet:

http://www.adestotech.com/products/serial-flash/dataflash

DataFlash® Sample Request:

http://www.adestotech.com/sample-ordering-information