Adesto Serial Flash Power Saving Features and Concepts

Introduction

This note describes and discusses unique features of Adesto Serial Flash Devices and illustrates how to implement these features to lower system-level energy consumption and increase performance. Many of these features work in conjunction with the host MCU, and through efficient software implementation, increase overall system efficiency. Some of the features reduce the MCU software overheads, improving performance and reducing MCU time when accessing or managing the memory device itself, therefore directly reducing the energy footprint of the Host MCU. Other features reduce the energy consumption of the memory device itself. Lastly some of the options allow the system designer to improve efficiency by reducing the number of external components required, further reducing the system energy consumption and improving energy efficiency. The net result of this is a system that requires fewer components, fewer batteries, has a longer operating life for a given energy source, and operates faster with a smaller software footprint.

While this note does not provide software solutions or code examples, it will discuss the individual modes of operation for each feature, the concepts behind them, and the benefits derived from their use.

Feature	Applicable Devices		
	DataFlash® (AT45)	Fusion (AT25DF)	Standard Serial Flash
Small Page Erase/Write	✓	✓	--
Active Interrupt	✓	✓	--
Byte Write	✓	--	--
Ultra Deep Power Down Mode	✓	✓	--
Wide Operating Voltage Range	✓	✓	--
Dual SRAM Buffers	✓	--	--

Small Page Erase			
	DataFlash® (AT45)	**Fusion (AT25DF)**	**Standard Serial Flash**
Command Code	**0x81h**	**0x81h**	Not Available
Small Page Write			
	DataFlash® (AT45)	**Fusion (AT25DF)**	**Standard Serial Flash**
Command Code	**0x83h** (buffer1, w/ Erase) **0x88h** (buffer1, w/o Erase) **0x86h** (buffer2, w/ Erase) **0x89h** (buffer2, w/o Erase)	**0x02h**	Not Available

In the case where the application requires small packets of data to be frequently stored in non-volatile memory, or requires single bytes of data to be updated, small page Erase and Write commands improve performance and lower power usage. Examples single byte updates include: a PIN code, or last button press, or a simple time and date stamp. These activities require just a few bytes to be written. Many industry standard serial flash devices available today allow individual byte write operations, but force the designer to erase a 4KByte block first. This creates inefficiency in the system that small page size solves.

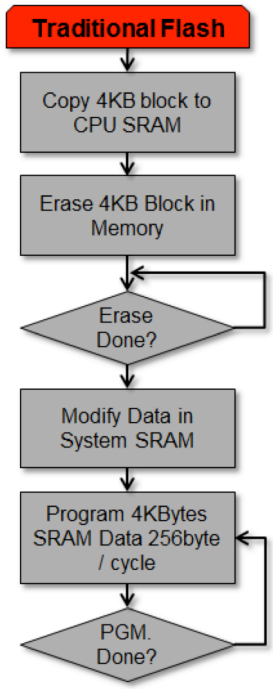

Figure 1

If the block of memory where the single-byte update will be located has data that must be preserved, the MCU is required to Read the entire block into system SRAM, then erase the entire 4KByte block before updating the single-byte. This requires 4Kbytes of temporary SRAM buffer space to hold the entire 4KByte block of data while it is erased. The MCU is then required to update the single-byte in SRAM and then copy the entire 4KBytes back to the Flash. Figure 1 shows a typical software flow for this single-byte update operation when Industry Standard Flash with 4Kbyte Blocks is used.

Not only is this inefficient but it also requires a massive amount of MCU time, often running into 10ms to 20ms to wait for the erase cycle to complete and then the MCU has to manage multiple page program cycles to re-program the data to the specific 4KByte block. Taking this into account the MCU is active for a much

longer time, consuming more energy, and the memory device itself is active in its programming and erase mode which is also consuming the maximum energy. Adesto Fusion Serial Flash solves this problem.

Adesto Fusion (AT25DF) Serial Flash Memory supports 256Byte Page erase and 256Byte Page write capabilities. These are features added to Adesto Serial flash devices to allow designers to utilise a smaller erase granularity, which directly reduces the active time of the MCU (Host) AND the memory device itself.

Self-contained Read-Write Data Buffering in Adesto DataFlash®

Adesto DataFlash® (AT45DB) devices support the page erase capability as described above but also provide additional features that increase performance and lower system energy use. DataFlash® integrates two (2) bi-directional SRAM buffers, in contrast to Industry Standard Serial Flash's single, unidirectional buffer, which can only be used for programming. The twin DataFlash® buffers can be individually written-to, and read-from. These SRAM buffers can be used as temporary SRAM buffer space. Frequently updated data can be written directly to the internal SRAM buffers and, read back from these buffers, without initiating a power hungry programming or erase cycle. There is more detail on this topic later in this note

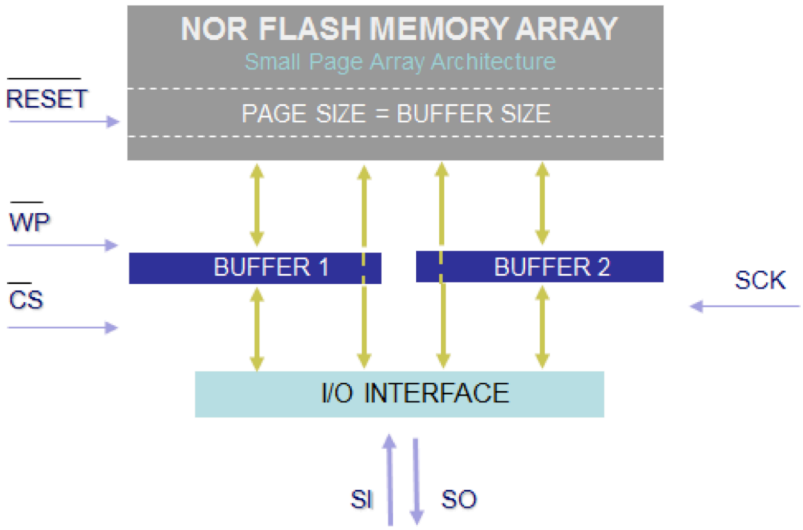

Figure 2

The dual-bidirectional buffer architectural advantage of DataFlash® can also be employed to increase the effective endurance of the device; for example the MCU can write 1,000 times to the buffer, and write once from the buffer to the flash memory array. This approach will enhance the endurance by a factor of 1,000:1 while reducing the programming and erase energy used by a factor of 1,000:1.

The dual buffers can be used in alternating fashion to provide continuous data logging. The MCU writes to Buffer 2 while Buffer 1 is being programmed into the flash array. Similarly, Buffer 2 can be read during this time that the contents of Buffer 1 are being programmed into the flash array.

One use of the dual buffers is to use one for typical read/write functions, and the other buffer as the holder of run-time parameters, which may change during operation, but need to be saved at each power-down. The

buffer is used as SRAM until the power down sequence gives the command to write the buffer to the flash array for safe keeping until the next POR.

Active Interrupt			
	DataFlash® (AT45)	**Fusion (AT25DF)**	**Standard Serial Flash**
Command Code	**0x25h**	**0x25h**	Not Available

For systems that use industry standard serial flash today, when a programming or erase operation is underway, the only way the MCU (host) can determine the status of the device is to poll the memory device status register, extract the Ready/Busy bit from the status register sequence and make a judgement based on values of the pertinent bits. This process is time consuming and MCU-resource heavy. An alternative is to let the MCU sleep for some predetermined length of time, before waking up and polling the memory device. This process is a little hit or miss and also results in system efficiency short falls.

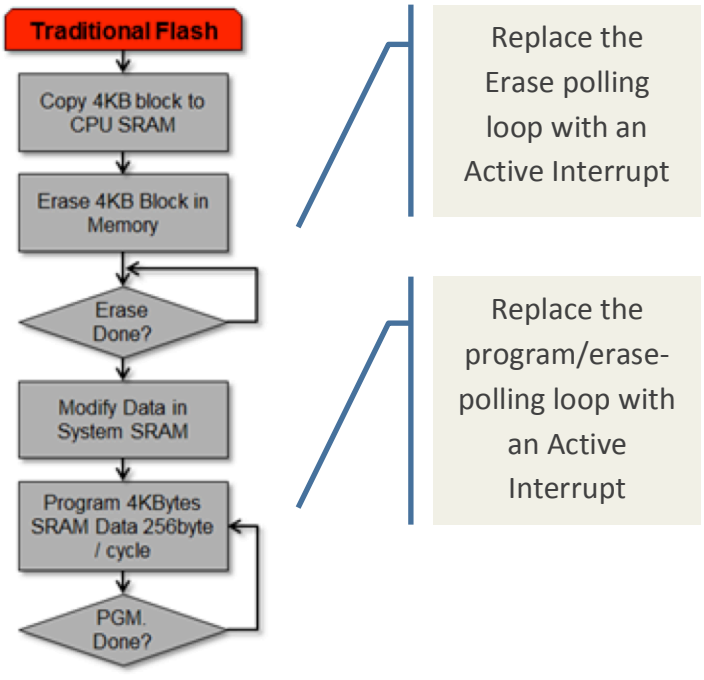

Figure 3

Adesto's patented Active Interrupt capability is implemented the Fusion (AT25DF) Serial Flash memory devices, in the 2Mbit and 4Mbit densities. Active Interrupt is a command-enabled option that is used when the host initiates a program or erase operation to the serial flash. By issuing the Active Interrupt command, the MCU (the SPI bus master) can then enter a sleep state during the program/erase time. The Adesto memory device with Active Interrupt will toggle the flash memory's SO line (which is the MCU SI line) at the completion of the program/erase cycle. The MCU SI line can be configured as an interrupt input to wake up the MCU from the sleep state and continue normal operation. The Active Interrupt feature brings the memory device into the realm of an intelligent peripheral device,

interactively communicating with the MCU as required to signal the end of a program/erase cycle.

The Active Interrupt capability works for all internal programming operations and all internal erase operations on the Adesto serial flash memory device. The MCU needs to support edge triggered interrupts on its SI line from the memory device, or the same signal can be tied to an alternative MCU pin that does support interrupt capability.

This one feature will significantly reduce system energy consumption when performing programming and erase operations by allowing the MCU (host) to sleep during these periods. It will reduce inefficiencies in time-out based solutions and reduce software complexity and size.

Byte Write			
	DataFlash® (AT45)	**Fusion (AT25DF)**	**Standard Serial Flash**
Command Code	**0x58h (buffer 1)** **0x59h (buffer2)**	Not Available	Not Available

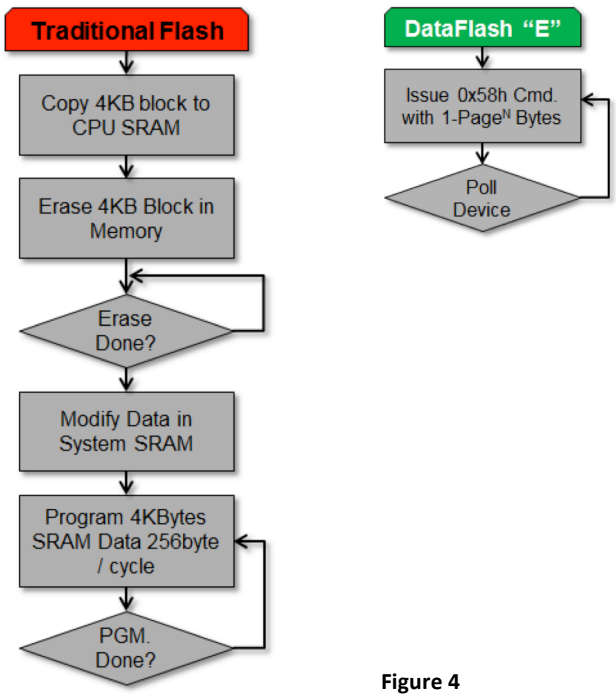

Figure 4

DataFlash® (AT45DB) Serial Flash devices offer many features that support superior system performance and reduced software overhead. One significant feature is the inclusion of an internally managed byte write capability. Earlier in this note the page erase, and page write features were discussed. These features allow the erase and reprogramming of smaller, more granular, blocks of data. For applications looking for single byte write and the ability to replace serial E²PROM, the DataFlash® BYTE WRITE command is available. This command is available in the DataFlash® E-Series (5th Generation) and later products. The Byte write command allows the designer to write anywhere from 1byte to a full Page of bytes, without any pre-erase or other page programming command. The device will internally manage the read-modify-write operation, providing the serial flash with the byte-write capability usually found in serial E²PROM devices. DataFlash® supports two bi-directional SRAM buffers, and the byte write command can be implemented through either SRAM

buffer independently. The Command 0x58h addresses buffer 1 and the Command 0x59h addresses buffer 2. If data is written to the buffer, and the byte write command is initiated, then only those modified bytes will be written to the memory array, at the defined page address. Data in un-modified locations in that same page address will remain un-modified. This command will reduce the MCU software overhead when writing very small blocks of data.

Ultra Deep Power Down Mode			
	DataFlash® (AT45)	Fusion (AT25DF)	Standard Serial Flash
Command Code	**0x79h**	**0x79h**	Not Available

In many applications powered from batteries, coin cells, or energy harvesters, minimizing system energy usage is critical. These systems also tend to spend a significant amount of their time in standby or sleep mode. Adesto memory supports this concept and Adesto serial flash memory devices implement an Ultra-Deep Power-Down mode (UDPD) to achieve the lowest power consumption possible.

UDPD is an additional level of power-down capability, over and above the general standby, low power or power-down mode and deep power-down mode, supported by most serial flash architectures today. UDPD is command driven and turns off all internal memory logic, charge pumps, sense amplifiers, SRAM buffers, internal clocks and control logic, except for a simple edge triggered, or level-detect, circuit on the Chip Select input pin. This circuitry design allows the memory to enter the lowest possible sleep state of any serial flash device. Power levels below 150nA are possible, as compared to the best-case levels of 1uA or 2uA typical of the alternatives available in the industry from other supplies today.

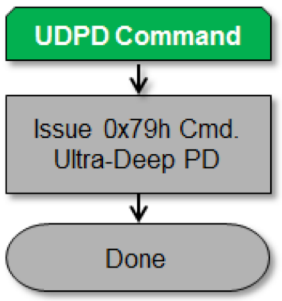

Figure 5

Entering the UDPD mode is accomplished by issuing the command 0x79h. If no internal programming or erase operation is underway, the device will enter the Ultra-Deep Power-Down mode. To wake the flash memory up, the host system simply needs to activate the chip select signal to the memory device, and within a short period of time, the memory device will be ready to accept new command cycles. In practice, many uses will simply send a dummy command, or no op command (a command that has no valid function) to the flash and by the time all 8 bits of the dummy command have been clocked in, the flash device will be awake. The longer a system spends in Ultra-Deep Power-Down mode, the greater the benefit this feature will deliver.

Wide Operating Voltage Range	Applicable Devices		
	DataFlash® (AT45)	Fusion (AT25DF)	Standard Serial Flash
Command Code	**No commands required**	**No commands required**	Not Available

Adesto DataFlash® (AT45) and Fusion (AT25DF) serial flash devices all support a wide VCC operating range of 1.65V to 3.6V. The wide VCC range allows the memory device to operate and function directly from the battery. Many ASSP chipsets and MCU's today can operate over a wide VCC range, and are connected to various power sources including lithium chemistry based cells. In systems where serial flash memory is required to provide additional system storage for data, or OTA capability the designer is often forced to utilize a serial flash with limited VCC range (2.3V to 3.6V) and then has to add additional components such as Low Drop Out regulators, buck-boost convertors (with the additional inductors and capacitors) and associated levels shifters. This severely impacts the system battery life, system performance, AND often increases the Bill of Material costs and PCB size. Wide VCC range Serial EEPROMs are available, but they are prohibitively expensive in the densities often required. Adesto DataFlash® (AT45) and Fusion (AT25DF) serial flash devices solve this problem by supporting a wide VCC operating range of 1.65V to 3.6V. Some Fusion (AT25DF) serial flash devices support 1.65V to 4.4V VCC operating range to allow direct connection to LiPoly batteries and their associated chargers.

Buffer Write			
	DataFlash® (AT45)	Fusion (AT25DF)	Phoenix (AT25SF)
Command Code	**0x84h (buffer 1)** **0x87h (buffer 2)**	Not Available	Not Available

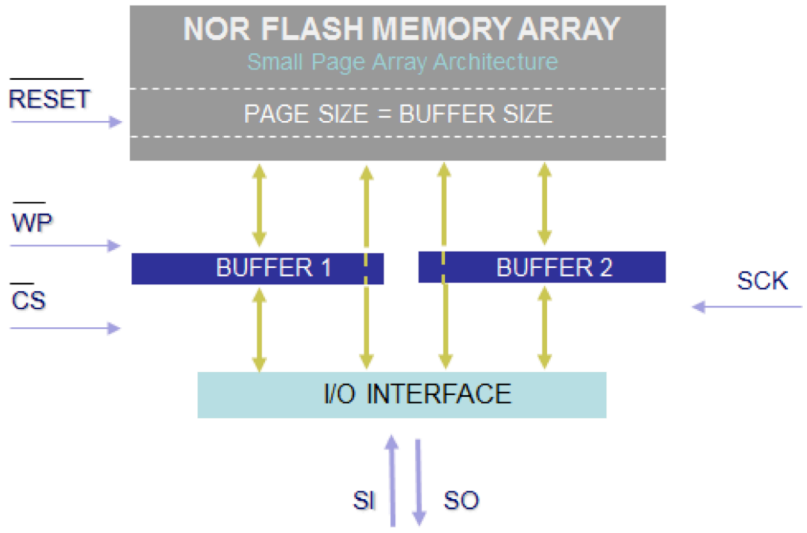

Figure 6

Adesto DataFlash® architecture integrates two (2) bi-directional SRAM data buffers, which are independent of each other, allowing the system to initiate programming via one buffer and to continue using the device via the 2nd buffer. An example of a benefit of this feature is during Over-The-Air Updates (OTA), which often require programming of large areas of the array. Using both buffers, the designer can stream to buffer 2 while buffer 1 is programming, and vice versa. This will save significant amounts of time and energy in the system.

Another benefit of the SRAM buffers on the DataFlash® devices is the ability to stream data directly to the buffer and hold it there until writing to the flash array is required. This technique saves significant amounts of precious MCU stack space and internal SRAM resources.

Finally DataFlash® supports another feature that can save time and energy. If the application knows that a page is pre-erased, then the system can initiate a page program without erase. This will shorten the programming time to less than 50% of standard flash. In systems that require power failsafe, or other critical system data backup, this shortened page programming time can be a powerful benefit.