Introduction to Alliance Memory SRAMs

SRAM is a device that is a key part of the core of a lot of hard ware systems. SRAM stands for Static Random Access Memory. This application note is intend to provide a first time reader an introduction to SRAM basics and structure in SRAMs

SRAM and DRAM are Random Access Memories that can store data as long as power is applied to the device. If the power is removed, all the data that was stored in the memory will be lost; DRAM data could be lost if it is not periodically refreshed, while in SRAMs data can be stored without refreshing, and SRAMs data will remain in the SRAM once it has been written there, and as long as the power supply to the device is maintained ; Figure 1 below shows SRAM Basic Architecture.

SRAMs are differentiated from its memory counterparts by the type of the memory cell. Most SRAMs either use a 4- Transistor or a 6- Transistor Memory cell. These cell structures allow data to be stored for an indefinite amount of time in the device as long as powered. Figure 2 below shows the Memory Cell History the 4 transistor and the 6 transistor cell, 1 transistor cell for DRAM. The SRAM cell is formed by cross-coupled inverters; Hard- ware system evolution overtime has led to the creation of different types of SRAMs (these referred to as the 4- T and 6- T cells, respectively.)

Types of SRAM

SRAMs basically come in two different flavors: synchronous and asynchronous.

Synchronous SRAMs are devices that are synchronized with an external signal clock.

Asynchronous SRAMs are devices that are not synchronized with an external signal clock, but they will begin to read or write data into memory as soon as it receives the instruction to do; Because asynchronous devices are slightly easier to understand, and these devices are typically subdivided into two different categories, based on their access time, which is the total time it takes for the device to
output data after receiving a read instruction. It based on their access time, which is the total time it takes for the device to output data after receiving a read instruction.

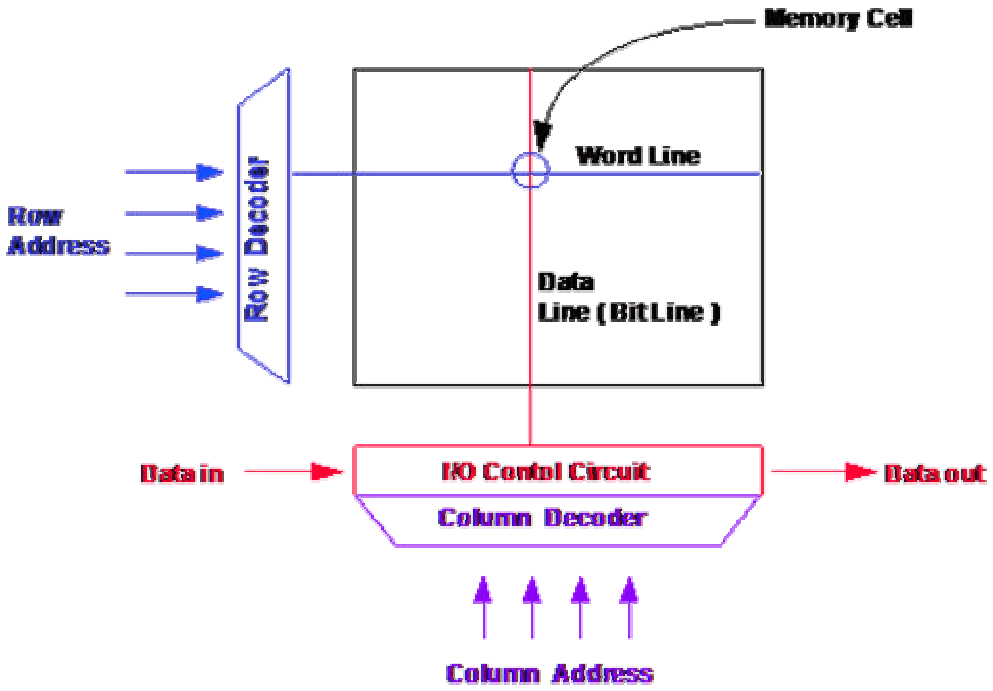
Fast Asynchronous SRAMs

These are devices that typically operate in the sub 10 ~ 20 ns region. They are often used in buffer memory applications, consumer products, etc. Fast asynchronous SRAMs have been used for a long time and the market for these devices has matured to a stable level. The density range for these types of SRAMs is from the sub 64K to 4 Mb and have data words that are mostly configured as x8, x16 . (This is the size in bits that each memory location can store.)

Low Power SRAMs

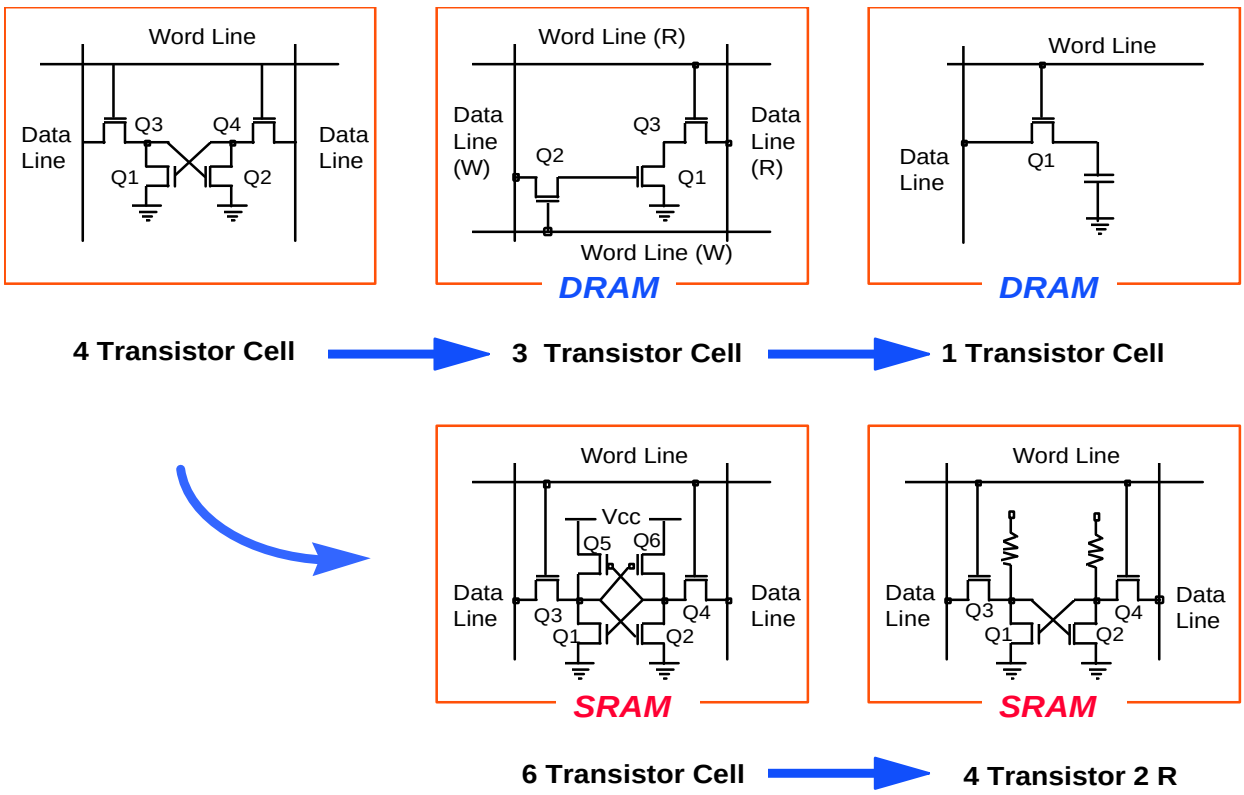
These are devices that typically operate in the 45-ns and slower speed range. These SRAMs are typically designed to consume very low power and are used in applications where power is a major concern. Applications for these SRAMs include digital signal processors (DSPs), PDAs, radios, pagers, consumer electronic products, etc. In these applications, these devices are used for temporary data storage, as well as scratch pad applications. Although Low Power SRAMs have also been around for many years, the recent surge in consumer electronic products have expanded the market for these devices. The density range for these SRAMs is usually from 64K to 8 Mb and are mostly configured with word widths of 8, 16 bits

Figure 1. SRAM Basic Architecture



Column Addresses, Row Addresses have different pins.
Usually Common I/O

Figure 2. Memory Cell History



Summary

Alliance Memory, Inc. is one of the leading to the legacy SRAM products; In addition, Alliance memory offers Synchronous DRAMs in the both 16Mb and 64Mb densities, we have committed to support the legacy SRAM products and to provide the excellent customer service, delivery and reliability.