Cleaning Challenges and Approaches of Advanced Strip Technologies for the 32nm Node and Beyond

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Abstract

The critical challenges for cleaning technology to meet the requirements of semiconductor manufacturing fabrication for the 32nm node and beyond are described. The effects on cleanliness and various types of material loss, dopant loss, and surface modification during HDIS (High Dose Implant Strip) are discussed. The adoption of plasma dry strip technology to emerging material removal applications such as Si-containing ARC (Anti-Reflective Coating) layer removal, strip over exposed TiN or TaN layers, and strip over ultra low-k material have been also explored. Each specific emerging advanced material and complex stack layer requires the readiness of the hardware to apply novel chemistries and customized technical approaches.

Introduction

Dry strip has evolved over time to address technical and economic drivers, and will continue to meet new challenges. The materials to be removed have broadened from photoresists to Oxide and Nitride hardmasks, Carbon-rich spin on materials and Si-containing ARC layers. In order to generate high photoresist ash rates and high removal rates of the aforementioned materials, various plasma chemistries such as O_2, N_2, FG (Forming Gas), CF_4, H_2O and NH_3 have been developed and commercialized. An even greater challenge is given by increasingly more stringent substrate loss requirements, that are originated from the complexity of stack layers and the introduction of new materials, such as high-k materials, low-k materials, and novel metal layers. Optimum process integration has become a major focus in dry strip. The dry strip cleaning equipment has also become more complex to accommodate new plasma chemistries and technologies with advanced technology being adopted in order to deliver stable plasma and prevent any adverse effects on the substrate from interaction with plasma.~~a..~~

In this paper, we will list the most challenging areas for dry strip and present current analyses of the issues as well as technical approaches to resolve them.

HDIS (High Dose Implant Strip)

The HDIS (High Dose Implant Strip) application continues to require a high degree of cleanliness, while advanced device complexities add additional requirements such as controlling substrate loss, substrate oxidation and dopant loss. In addition to the previously studied results[1], many different approaches have been explored including all-wet, partial ashing of the crust layer combined with wet cleaning, and dry strip with DI (Deionized) water rinse. Optimizing a process by varying process chemistry and process temperature to prevent adverse effects such as resist popping, blistering and residue is necessary in order to maintain acceptable levels of process defects, manufacturability, and reliability[2].

In the early stages of dry strip technology, most substrate loss testing was carried out on thermal oxide, which is relatively immune to etching by downstream plasma chemistry. Substrate loss has been controlled primarily by varying the gas ratio and process temperature during dry strip processing[3]. However, the use of implants with increasing doses at lower energies and multiple implant species have reduced substrate loss specifications dramatically. The effects of ash chemistry on silicon consumption have been shown in previous studies[4]. It has been indicated that processes using fluorine-containing etching chemistries have shown linear relationships to substrate loss, as a function of the number of sequential process steps, while non-etching chemistries, wet cleaning (SPM+APM) and a combination of dry strip and wet cleaning have shown self-limiting behavior. This material loss has been well known to result in critical issues such as dramatic increase in source/drain resistance and shifted transistor threshold voltages, especially during USJ formation [5].

Ash-related substrate oxidation has been extensively studied in order to understand the nature of Si loss and provide the direction to avoid it. Oxidizing chemistries have shown self-limiting growth during ash and higher oxidation rates are observed for hydrogen-containing plasma due to H* enhanced oxidation. Oxidation rates peak at around ~10% O_2 for hydrogen-containing plasma which may be due to OH* reactivity as shown in Fig.1.

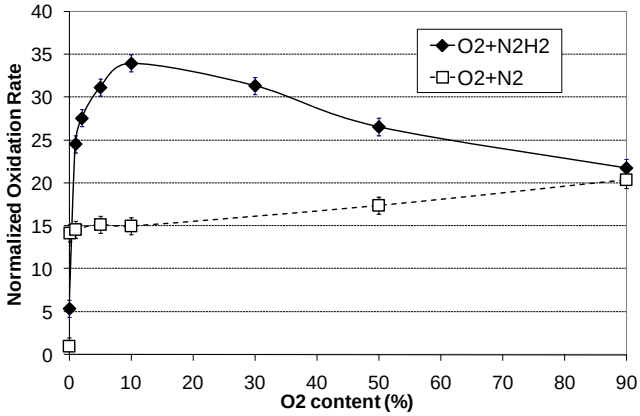

Fig. 1. Normalized oxidation rate as a function of O_2%. 240 ^oC process temperature with O_2+FG or O_2+N_2 chemistry

Oxidizing ash chemistries generally also result in thicker oxide growth compared to reducing chemistries. As evidenced by SIMS analysis, the nitrogen signature peaks at about half

the maximum of the oxygen profile, which indicates that a nitrided (SiN) layer is formed at the Si/SiO_2 interface. Based on the results described above, advanced chemistry approaches have been introduced in order to control substrate loss and substrate oxidation while maintaining the cleanliness of the HDIS process and demonstrating acceptable ash rate and ash rate non-uniformity.

According to previous studies[4-6] on ash process effects on junction resistivity during USJ (Ultra Shallow Junction) formation, there appear to be several mechanisms, such as substrate loss, dopant loss, dopant diffusion (TED), dopant out-diffusion and dopant activation. For As implanted samples, the surface oxidation trend is shown, indicating that dopant loss for As is mainly ash induced. For the BF_2 implanted case, an oxide capping effect is shown indicating that dopant loss for this case is mainly dictated by the anneal, as shown in Fig. 2. This result clearly indicates that junction design and optimization requires inclusion and optimization of post-implant clean effects.

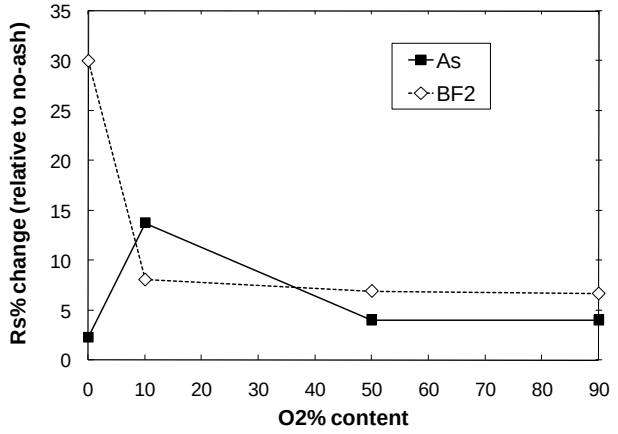

Fig. 2. Normalized sheet resistance change as a function of Oxygen content in ash chemistry on As and BF_2 implanted Si, respectively.

Strip over Advanced materials

Si-containing material has been widely adapted in order to produce high etch selectivity at sub-micron nodes, and the Si content of these materials has been increased to more than 40% in some cases. Traditional O_2-based chemistries have shown adverse effects due to Si oxidation, and the inability to remove the Si-ARC layer and the organic residues causing issues during wet cleaning. Loss of the oxide layer beneath the planarizing layer must be controlled and Si-ARC related residue formation on top of the underlying oxide layer must be minimized. The all-wet cleaning approach or an O_2+CF_4 process in either an etcher or asher have been used to attempt to meet the requirements described above. We have introduced a fluorine-free chemistry to remove the planarization layer by penetrating through the Si-ARC, and incorporated diluted HF cleaning for the remaining Si-ARC residues.

In order to remove 193nm resist over High-k/Metal Gate without adversely affecting device electrical characteristics, most notably V_t and T_{inv}, an oxygen-free ash process has been characterized and implemented in a 32nm manufacturing environment. Oxygen-based chemistry was ruled out, in that oxygen diffusion through the high-k would oxidize the silicon and lower k-value. Fluorine chemistry has been reported to damage the gate area and shift device performance. A more extensive study of hydrogen- and nitrogen-containing chemistries has been requested in order to further understand the exact mechanism of deterioration of device performance when using various stack layers including encapsulated high-k and exposed metal gate schemes.

Removal of resist or carbon spin-on-hardmask without oxidation of underlying metal layers such as TiN, TaN, W or residue from etch damaged resist have also been investigated. We demonstrated different H_2 -containing chemistries for metal oxidation free ashing for exposed tungsten metal bit lines and high aspect ratio tube capacitors with exposed TiN / TaN. In order to determine accurate surface thickness change, various methodologies such sheet resistance measurement, XPS (X-ray Photoelectron Spectroscopy) and TEM (Transmission Electron Microscopy) were utilized. We observed a strong increase in TaN metal oxidation with added ppm-levels of O_2 without substantial increase in ash rate. Inert wafer cooling resulted in a ~50% decrease in oxidation for the same recipe, as shown in Fig. 3. This may result in potential yield improvements and higher productivity by enabling use of chemistries with higher oxygen content, along with higher temperatures.

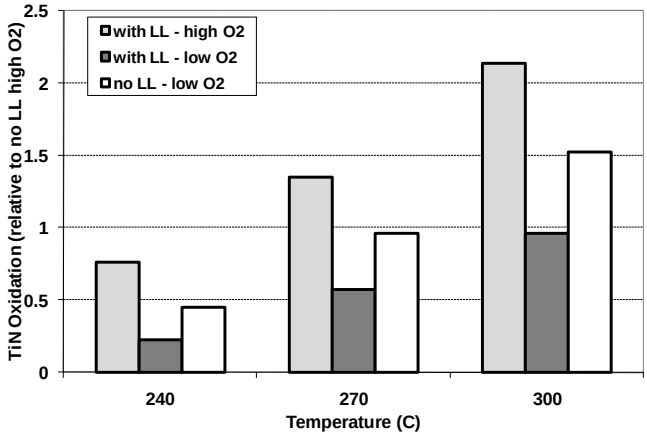

Fig. 3. The amount of TiN oxidation as a function of process temperature in various cooling environments.

Lastly, a study on strip over low-k was done, comparing the HeH_2 down stream plasma chemistry approach to RIE (Reactive Ion Etch) type processes using oxidizing and reducing chemistries. The low-k material damage mechanism has been extensively studied[7-9] and it has been concluded that $He:H_2$ ash preserves carbon in the Low-k film whereas oxygen and nitrogen consume carbon. It has also been concluded that the difference in RC-delay between a device treated with $He:H_2$ ash compared to that treated with CCP (capacitively coupled plasma) ash becomes more pronounced with smaller feature dimensions since the contribution of the modified dielectric region to the total capacitance becomes more significant.

Summary

Dry strip has evolved over time to address technical and economic drivers, and will continue to evolve to meet new challenges. Residue-free, substrate loss-free HDIS requires optimized process integration between dry and wet cleaning. Junction design and optimization requires inclusion and optimization of post-implant clean effects. Emerging advanced materials and complicated stacks require the readiness of hardware to apply novel chemistries and technology approaches.

Acknowledgments

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