BarcoSilex

# PCI Express (PCIe) Endpoint DMA

BA611
Product sheet

## General Description

**The PCI Express (PCIe) Endpoint DMA is a highly configurable solution for any FPGA design requiring PCIe interfacing. It supports PCIe Gen 1, Gen 2 and Gen 3 interfaces, with up to 8 lanes. The DMA makes it easy to quickly transfer massive data between CPU and FPGA.**

The flexibility of the IP core enables many different use cases. The configuration of the Endpoint DMA can easily be adapted to the requirements of each project.

The PCIe Endpoint DMA is already used in many applications such as Ethernet cards, high resolution image processing and others.

## Technical Description

The PCIe Endpoint DMA is an assembly of multiple modules: the bridge, the translation layer, registers, DMA and interrupts.

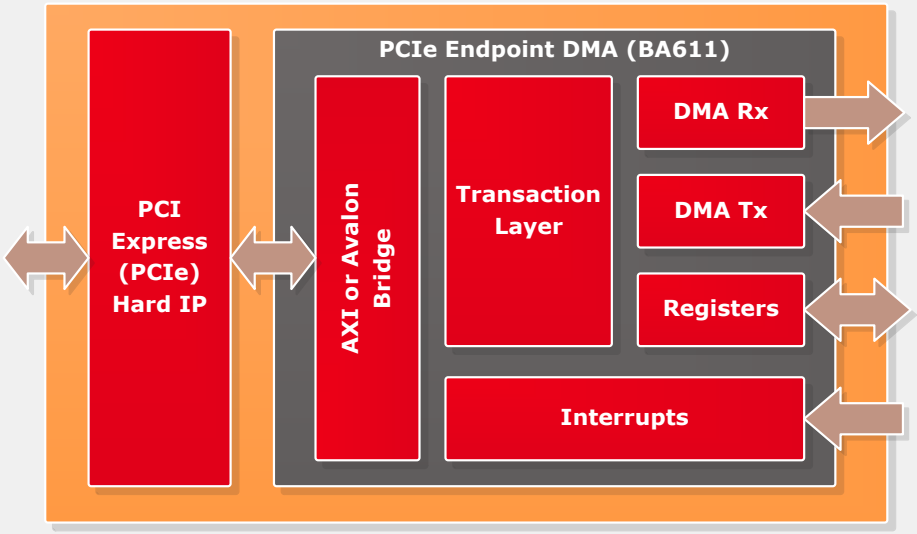
The Rx and Tx DMA modules can support both 32-bit and 64-bit address access. Each DMA is individually configurable on the fly.

The Endpoint DMA IP core can be used to implement multiple functions. The multiple functions make it possible to have multiple PCIe endpoints with a single physical interface.

The Interrupts module efficiently handles and transmits MSI-type interrupts.

## Features

- PCIe endpoint
- Gen 1, Gen 2 and Gen 3
- 1x, 2x, 4x and 8x
- Up to 16 DMA controllers
- Highly configurable
- Altera FPGA
  - Cyclone V
  - Arria II & V
  - Stratix IV & V
- Xilinx FPGA
  - Spartan-6
  - Artix-7
  - Kintex-7
  - Virtex-7
- Standard interfaces
  - AXI-4
  - Avalon
  - Simple streaming
- Drivers
  - Windows
  - Linux



## Configuration parameters

The following configuration parameters can be defined according to the requirements of the project.

| Parameters | Description |
|---|---|
| PCIe Type | Gen 1, Gen 2, Gen 3 |
| Number of lanes | Number of lanes on PCIe physical bus |
| Number of functions | Number of PCIe functions (up to 8) |
| Number of Rx DMA | Number of DMA for Rx transfers |
| Number of Rx Direct Write | Number of Direct Write for Rx transfers |
| Number of Tx DMA | Number of DMA for Tx transfers |
| Number of registers modules | Number of modules to be connected to different BARs |
| BAR info | Number and size of BARs |
| Timing info | User clock frequency used for register access and Tx transfers |
| Number of external IRQ | Number of interrupt signals coming from the user application |
| Type of data interface | AXI4, Avalon or Streaming |
| Type of register interface | AXI4 Lite, Avalon, or SRAM |

## Drivers

The PCIe Endpoint DMA is provided with the necessary drivers for Windows and Linux. An example application is included to accelerate your own development.

# Deliverables

- Encrypted VHDL files for simulation with/without BFM (Altera or Xilinx BFM).
- Testbenches (VHDL and C files) and scripts for simulation with Modelsim and NCSim.
- Synthesized netlist or source code of the PCIe Endpoint DMA.
- Constraints file for implementation tool.
- Driver and example application software (source code in C language).

# About Barco Silex

Barco Silex is an electronic design house (ASICs, FPGAs, DSP, boards, embedded SW) specialized in video compression, security and memory controllers. Barco Silex offers the best guarantee for continuous support throughout the complete lifecycle of products.

## For more information, please contact us.

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