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Discussion on non functional pad removal / backdrilling and PCB reliability. - Bill Birch

The pads Vs no pads question has been going around for many years. There have traditionally been two trains of thought that are usually based on the products end use environments. The first opinion - originally - (and still is to some extent) driven by the military and the second philosophy by the higher end users. The military believe (based on studies in the 60's, 70's & 80's) that the addition of non functional lands on all internal layers would increase the reliability of the plated through hole structure. The second opinion driven by the majority of PWB manufacturers and the commercial world believe removing non functional lands would increase yields (lower costs), by potentially avoiding other issues like internal shorts between pads and traces.

Secondly, " lower end " users believe that the life expectancy of their products would never reach the point where the subtle differences of pads Vs no pads would ever become a factor for interconnect reliability. The realities of today's products is that most products are considered commodities, life expectancy is decreasing, cost savings are being sought at every level and electrical performance needs supercede any possible concerns related to via integrity.

The interesting thing about the question of pads Vs no pads is that both sides are both right, although we need to be a little more specific in order to understand the causes and effects on the potential failure mechanisms. We have completed several large pads Vs no pad studies for various companies. The continuing trend (which as always is product design specific) is as follows:

With smaller vias/higher aspect ratio (.008" / 0.2mm to .020" 0.5mm) the inclusion of internal lands is negative (10-30% reduction in long term performance). Conversely, with larger holes/lower aspect ratio (via size - .020"+ / 0.5mm+) the inclusion of internal lands is positive (10-15% increase in long term performance).

Ongoing failure analysis at PWB shows that when .008"-.020" PTV's contain pads on all or most layers, the barrel crack locations are nearly always positioned between, or adjacent to the two central pads (propagating from glass bundles in resin rich areas). With PTV's where pads are removed, the cracks occur randomly throughout the central region of the barrel, but not necessarily in the central zone. We believe this situation is primarily related to the distribution and re-distribution of stain.

One hypothesis at PWB is that when strain is applied to the sidewall of the .008"-.020"(higher aspect ratio) PTH barrel, the pads in the central zone create a "focal point" or stress riser for the strain. The pads "channel" the strain to the point of least resistance, which tends to be the thinner plated copper in the center of the PTH vias. The small improvements in performance for products with pads removed (smaller hole size only) is related to the fact that cracks occur in areas away from the center, where the PTH copper is slightly thicker.

The situation is different for larger diameter vias, the increased surface area of the PTH barrel is more able to absorb and re-distribute the stain (barrel receives less local strain). When the strain is redistributed the non functional pads absorb a proportion of the stain (usually seen as land rotation), the redistributed strain reduces the relative stress/fatigue applied to the barrel.

We must put the question of pads Vs no pads into the perspective of the product attributes and the quality of the interconnect. A simple way to look at the situation is to consider some of the major factors that influence interconnect performance, this is important because the influence of pads Vs no pads is very subtle and only becomes a factor under certain conditions. We must consider the hierarchical influence of each set of conditions and determine if the inclusion of pads will increase or decrease interconnect reliability.

PWB's experience has identified major considerations that affect PTH barrel and internal interconnect reliability (in hierarchical order) are as follows:

1st Level: Copper plating – Thickness and quality, (uniformity, ductility, elongation, tensile strength).

2nd Level: Material (Tg, CTE, Modulus) - board thickness, hole diameter, number of layers (glass to resin ratio).

3rd Level: Surface finish, PTH metallization, foil thickness, construction, grid size).

4th Level: Design (pads Vs no pads, annular ring, anti-pad clearance).

Based on the above information 2 additional major factors must also be considered, these are NOT normally included in studies to determine interconnect performance.

1) Who builds the product is one of the biggest variables in the industry, virtually all studies that we have completed (with multiple vendors) identified that the supplier was the most dominant factor (on products designed and produced using the same attributes, materials, plating thickness' etc.). The range of potential performance is very wide (making the decision of pads Vs no pads disappear far into the noise!!), if you refer back to the hierarchical order it helps to identify where the major differences are between numerous PWB suppliers.

2) The impact of the assembly environment is becoming an important issue for certain products, especially as we move toward lead free profiles. We have completed several studies which compared the impact of multiple cycles through the IR ovens, in some cases the interconnect performance was virtually unaffected, other products measured reductions of 80%. The majority of studies were completed by testing the as received products, followed by testing after 3 or 6 passes through an IR oven (again, the impact was vendor related!!!)

Most mid to high end products are using double sided BGA's on the substrates, this requires the board to see 3 IR reflows as a standard, some companies want to know if they have the ability to rework the BGA's, thus 5 or 6 cycles was selected to ensure a safety margin.

The environment of your products is an important factor, most companies that are concerned about this issue have products that are required to perform in very severe temperature/humidity environments, or require long term performance (15-25 years). For the majority (98+%) of products the working life is shrinking, as technology accelerates, products are becoming redundant within 5-10 years.

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With all that said, I can not see why removing the non functional lands (on smaller via diameters) would influence the products performance. All of our data shows that the effects are subtle, pads Vs no pads is down in the lower hierarchical influence category, there are clearly much more dominant factors that are affecting interconnect performance.

To some extent the aspect ratio determines the "rules"; Once you get above 4 to 1 the influence of non-functional pads starts to play a role, especially when layer counts and/or higher resin contents constructions are used. In an ideal situation there would be "no pads" in the barrel structure, this would permit maximum compliance/compression during the thermal excursion. In reality we have random "locking" locations that focus the stress toward the bending moment, creating a stress riser.

Basically, the higher the aspect ratio (or volume of resin) the more compliance is required. In order to maximize the strength of the barrel we need to "re-distribute" the stress somewhere away from the focal point (usually the centre of the construction) by removing non-functional pads from the central zone. Our experience has shown us that distributing the stresses equally across the central zone of the barrel achieves the highest reliability, specifically when good quality plating, materials and processing conditions are involved.

The majority of premature failures that we investigate include individual connections between the internal pad located in the central zone of the PTH via, the barrel cracks are predominantly on the B stage (pre-preg) side of the foil. The pad creates the anchor point, which becomes more influential as the foil thickness increases.

A standard design rule that we recommend would locate non-functional pads at the signal or plane layer locations closest to 1/3rd of the distance from the top and bottom of the structure (total two non-functional pads, this is in additional to the functional pads. This approach divides the barrel into 3 "stress" sections; The upper and lower sections receive virtually no tensile or compressive stress (most of the stress' are heading to the surface, between the vias), the location of two constraining connections permits a more even distribution of stress around the central area of the barrel.

For a worse case condition a secondary rule could apply as follows: If you have a 16 layer board and the signal layer is connected only on layer 9, locate a non-functional pad on layer 8 (to balance the centre stress distribution), plus apply the 1/3rd rule.

I hope this has helped to explain the logic. Obviously, the rules are relative to the product complexity and construction, I would be very interested to hear the results of any other testing that has been completed.

2) Back Drilling or “Counter boring”

From a reliability perspective the back drilling process greatly increases the performance of the PTH vias. The primary reason is due to the “relieving” influence of disconnecting the via from one side of the substrate, the barrel is virtually “floating” achieving literally unrestrained movement). If the via is back-drilled beyond the central plane most of the mechanical constraints are removed, in basic/simple terms the more you remove, the more reliability is achieved

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The issues with back drilling are all associated to manufacturing, the primary problems that we have experienced are as follows:

1) Controlling the overall dielectric thickness and/or back drill depth

Traditionally we have created a test circuit within the IST coupon that is used to determine if the back drilling has reached the specified/required depth. Most PWB shops (to date) have not demonstrated the capability consistently to hold better than +/- .004" (0.1mm). The most common problem is "under-drilling" (not drilling deep enough), this is due to placing most of the tolerances on the "better to under-drill rather than over-drill" philosophy. Microsections have confirmed that even when an electrical clearance (open) is achieved the spacing between internal feature (usually plane) and the bottom of the back drilled via can be less than .001", potentially leading to CAF or dendrite shorts.

PWB manufacturers generally blame a combination of the following 1) differences in substrate thickness, 2) bend/bow/twist of the substrate, 3) planarity of height control across the entire panel. Please keep in mind that for most PWB shops back-drilling is one of the final operations, the panel is often etched before the drilling process.

2) Tolerances of dielectric spacing

We usually receive panels of coupons (36, 48, 60 up), we find that there are "areas" that are under-drilled. The drilling department will commonly set a single Z-axis coordinate; this is usually in the centre of the panel, coupons toward the edge or corners experience "shorts", likely due to slightly thicker dielectrics.

3) Under-sized back-drill diameters

To avoid the risk of leaving a slivers of copper on one side of the hole wall it is necessary to select a drill size between .006" and .010" larger than the original hole size. The combination of registration, hole wall preparation and shrinkage issues must be considered when specifying the secondary drilling process. Secondly, the power/ground clearance diameter and distance to feature edge must anticipate the larger geometry of the back-drilling, this creates an increased no-go area around these features.

Bill Birch