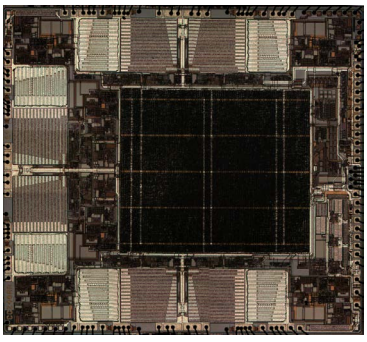
Automotive Electronics

Product Information

CG240

Integrated Low Side Current Regulator

BOSCH
Invented for life



Customer benefits:

- Fast six-channel current regulator for transmission control systems
- Integrated shunts and low side drivers
- Hardware solution, no µC necessary for regulation
- Available as bare die for high temperature integrated TCU applications
- Each channel can be configured for current control or switch mode
- Monitoring and diagnostic functions
- Minimum PCB area
- Higher channel count can be realized in combination with CG208 (two channels) or additional CG240
- 50% less space compared to discrete solution

Products

- Bare die solution - available
- Packaged solution - planned

Features

- Continuous current regulation 0.6mA to 1.2A
- 11 bit target current with 0.6mA/LSB resolution
- Integrated 300mΩ shunt resistance
- Current regulation capability can be doubled by parallel operation of two channels
- Current regulation can be configured with dither function and cycle frequencies
- Regulation parameters are programmable
- Dither shape sinusoidal or triangular
- -40°C ≤ TJ ≤ 175°C operating range for bare die
- Compensation of temperature effects
- Design-in full scale accuracy target: <1% (after TCU calibration)
- ±4kV HBM ESD handling robustness on TCU pins

Communication features

- 32 bit SPI interface, 4 MHz
- Optional synchronization of the power stage cycle frequency with external clock

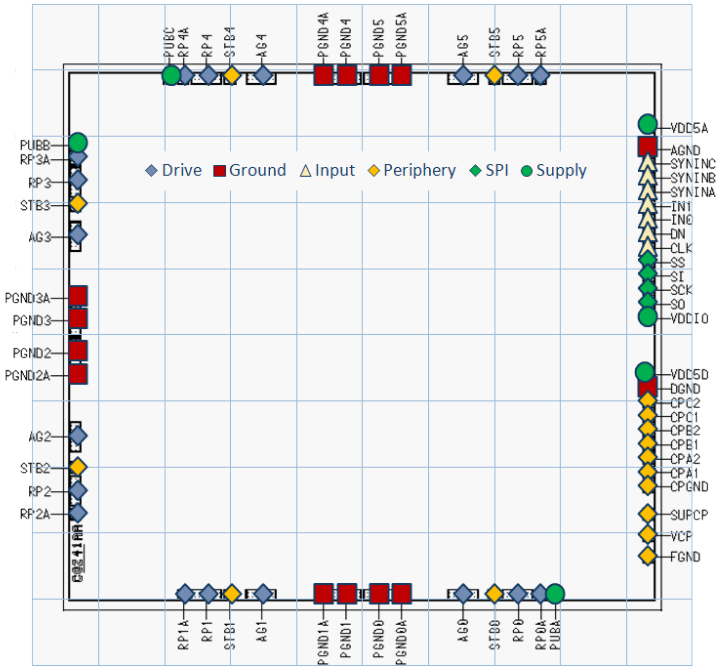
Target Package

- TQFP ePAD100

Key Parameters

Parameter	Value
V_{DD} supply	4.4 V .. 5.5 V
V_{PUB} driver supply	6.0 V .. 20 V
Operating supply incl. pulses	5.4 V .. 45 V
External CP capacitors / diodes	3 x ~33 nF
External CP freewheeling diodes	6
Max. temperature 100x30min / lifetime	175 °C
Storage temperature bare die	-55 °C .. 125 °C
Current control offset	< ±20 mA
Current control gain failure	0 .. 5 %
Current control INL	±5 mA
Current control temperature error	< ±1.75 %
Current control aging > 0.5A	< ±0.2 %
Current control aging < 0.5A	< ±1 mA
On-resistance power stages	typ. 100 mΩ
External clock input f_{CLK}	2 MHz
External synchronization (opt.)	max. 4 kHz
Dither amplitude (7bit)	Max. 591 mA
Dither frequency programming	Fraction of f_{CLK}

Pad layout overview



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