GTM-RM

GTM-IP Reference Model

Errata sheet

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Revision History

Issue	Date	Remark
0.1	10.04.2014	GTM-RM v1.5.5 differences to GTM-IP Spec. v1.5.5

Conventions

The following conventions are used within this document.

ARIAL BOLD CAPITALS	Names of signals
Arial bold	Names of files and directories
`Courier bold`	Command line entries
`Courier`	Extracts of files

References

This document refers to the following documents.

Ref	Authors(s)	Title
1	AE/EIN2	GTM-IP Specification
2	AE/EIN2	GTM-RM Users guide

Terms and Abbreviations

This document uses the following terms and abbreviations.

Term	Meaning
GTM	Generic Timer Module

Table of Contents

1 Errata

If an erratum listed in table below has the 'Fixed' attribute 'false', it is not yet fixed with current GTM-RM version 1.5.5-01. If it was fixed, it is no longer listed.
The value 'all' in column 'refer to' means that it is currently not intended to implement the feature.

Errata-ID	Errata	refer to	Fixed
GTM-RM-3	Title: AEI Bridge: The register fields TO_MODE, TO_VAL in GTM_CTRL are not implemented yet. Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: The AEI bridge is not relevant on GM-RM level. Thus, this feature is currently not intended to be implemented on GTM-RM. Scope: AEI Bridge (only available on GTM-IP) Effects: Workaround: None Severity: Low Classification: Non-critical	all	False
GTM-RM-4	Title: AEI Bridge: The GTM_AEI_ADDR_XPT, GTM_BRIDGE_MODE, GTM_BRIDGE_PTR1, and GTM_BRIDGE_PTR2 registers are not implemented yet.	all	False

	Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: The AEI bridge is not relevant on GM-RM level. Thus, this feature is currently not intended to be implemented on GTM-RM. Scope: AEI Bridge (only available on GTM-IP) Effects: Workaround: None Severity: Low Classification: Non-critical		
GTM-RM-8	Title: DMA support: Hysteresis functionality for IRQ signaling not implemented. Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: This feature is currently not intended to be implemented on GTM-RM. Scope: FIFO DMA support. Effects:	all	False

	Workaround: None Severity: Low Classification: Non-critical		
GTM-RM-10	Title: CMU: CMU_ECLKx clocks are not implemented. Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: The external clocks are currently not intended to be implemented on GTM-RM. Scope: CMU ECLKs Effects: Workaround: None Severity: Low Classification: Non-critical	all	False
GTM-RM-16	Title: MCS: Only the accelerated scheduling mode is implemented for the MCS-channels. Date of Notation: 20.12.2010 Date of Update:	all	False

	16.07.2012 Description: The SCHED bit in MCS[i]_CTRL register is not functional. Scope: MCS scheduling mechanism Effects: Only accelerated scheduling mode can be used for MCS operation. Workaround: None Severity: Low Classification: Non-critical		
GTM-RM-17	Title: MCS: Exact instruction timing not modeled. Date of Notation: 20.12.2010 Date of Update: 16.07.2012 Description: MCS Instruction timing not cycle accurate modeled compared to implementation in GTM-IP Scope: MCS Instruction timing Effects: MCS Instruction timing not cycle accurate. Workaround: None Severity:	all	False

	Low Classification: Non-critical		
GTM-RM-23	Title: MCFG: sub module MCFG not implemented. Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: This feature is currently not intended to be implemented on GTM-RM. Scope: MCFG Effects: No configurable memory areas for several MCS sub modules possible. Workaround: None Severity: Low Classification: Non-critical	all	False
GTM-RM-26	Title: DPLL: RAM access priorities not implemented. Date of Notation: 20.12.2010 Date of Update: 28.01.2011 Description: See title.	all	False

	Scope: DPLL Effects: Workaround: None Severity: Low Classification: Non-critical		
GTM-RM-59	Title: SPE: SPE does not support sensor signals with multiple input signal change on same point in time Date of Notation: 22.09.2011 Date of Update: 23.05.2012 Description: If more than one TIM input signals changes at the same point in time, the SPE sub module is not able to detect new valid or invalid input pattern correctly even if they are defined (in register SPE[i]_PAT) to change at the same point in time. Note: The problem is limited to SPE module, the TIM module can handle multiple input signal changes at same point in time. Scope: SPE Effects: In the described case the SPE[i]_PAT_PTR is not updated correctly and the SPI[i]_NIPD signal is not raised. Instead the SPE[i]_PERR flag is	v1.5.5-01	False

	raised. On the other hand, an invalid input pattern with multiple signal changes at the same point in time, may be detected as a valid input pattern. Workaround: Don't apply valid or invalid sensor signal patterns in which multiple edges occur at same point in time Severity: Low Classification: Non-critical		
GTM-RM-66	Title: MAP: Simultaneous changing of input signal TIM0_CH6 not supported Date of Notation: 22.09.2011 Date of Update: 08.11.2011 Description: If TIM0_CH6 is selected as direction signal T_DIR for the trigger input, TIM0_CH6 must not change at the same point in time as the actual trigger input signal changes (TVALID). Scope: MAP Effects: Wrong direction information will be forwarded to the module DPLL. Workaround: Only apply input signals, where the direction information of TIM0_CH6 is already stable during the time of the trigger event.	v1.5.5-01	False

	Severity: Low Classification: Non-critical		
GTM-RM-73	Title: TIM: External Capture Feature Date of Notation: 12.01.2012 Date of Update: 09.11.2012 Description: If two consecutive events occur with a delay of one clock cycle only one external capture event is forwarded to the destination instance. Scope: TIM Effects: Missing external capture events during runtime. Workaround: None. Severity: Medium Classification: Critical	v1.5.5-01	False
GTM-RM-77	Title: TOM: missing CCU1 interrupt request Date of Notation: 08.03.2012 Date of Update: 09.11.2012 Description:	v1.5.5-01	False

	Under following conditions bit CCU1TC of register TOM[i]_CH[x]_IRQ_NOTIFY is not set and thus no CCU1 interrupt may be raised. 1) On channel enable if CN0 >= CM1 and CM1 > 0 no CCU1 interrupt is generated. 2) In one shot mode if CN0 is written and new CN0 < CM1 and new CN0 < CM0 the CCU1 interrupt that should occur if CN0 reaches CM1 first time is not generated. Scope: TOM Effects: In the described case the bit CCU1TC of register TOM[i]_CH[x]_IRQ_NOTIFY is not set and no interrupt is raised. Workaround: None. Severity: Low Classification: Non-critical		
GTM-RM-368	Title: MCS: ECC RAM Error not implemented Date of Notation: 29.01.2013 Date of Update: 29.01.2013 Description: The MCS implementation of the GTM-RM does not simulate ECC RAM Errors. Scope: MCS Effects: ECC Errors cannot be simulated.	all	False

	Workaround: None. Severity: Low Classification: Non-critical		
GTM-RM-373	Title: ATOM/TOM: wrong output signal in case of centre aligned PWM with CM1=0 on triggered channel Date of Notation: 27.03.2013 Date of Update: 27.03.2013 Description: In case of RST_CCU0=1 (CN0 reset is triggered by preceding channel) and CM1=0, on CN0 reset to 0 an edge to !SL is generated (triggered by CCU1 after trigger of CCU0) The correct behavior would be that at point in time of reset CN0 to 0 trigger of CCU0 has higher priority than trigger of CCU1 (because of CM1=0) and thus at same point in time only trigger of CCU0 is executed (edge to SL). Scope: ATOM SOMP mode, TOM Effects: In the described case an additional edge to !SL is generated. This leads to incorrect PWM output signal. Workaround: None. Severity: Low	v1.5.5-01	False

	Classification: Non-critical		
GTM-RM-382	Title: MCS: Evaluation of CAT bit after blocking ARU instruction Date of Notation: 11.02.2014 Date of Update: 12.02.2014 Description: The specification for the instructions ARD, AWR, ARDI, and AWRI claims that the CAT bit can be evaluated by the MCS program in order to check if the last ARU transfer was successful (CAT=0) or cancelled by Software (CAT=1). However, since the CAT bit can be set directly by Software to cancel an ARU transfer at any time the bit does not reflect the status information reliably. Bad case: If the software is setting CAT between the time of ARU data arrival and evaluation of CAT bit. Scope: MCS Effects: If the mechanism for cancelling blocking ARU transfers by CPU is used the MCS may signalize an aborted ARU transfer by a set CAT bit although the transfer has finished successfully. Workaround: If the mechanism for cancelling blocking ARU transfers by CPU is used and data consistency by ARU transfers is important, a possible workaround may check the consistency by inspection of the transferred data (e.g. checking for linear increment of ECNT for data transfers from TIM to MCS).	v1.5.5-01	False

	Severity: Medium Classification: Non-critical		