Automotive Electronics C_CAN FD8 IP Module





C_CAN FD8 IP Module

Customer benefits:

- Based on the most widely used CAN IP module the C_CAN
- Driver Support of the C_CAN can be re-used for C_CAN FD8

Features

- Support of Classical CAN and CAN FD up to 8 byte according ISO 11898-1: 2015
- 32 Message Objects
- Each Message Object has its own Identifier Mask
- Programmable FIFO mode
- Maskable interrupt
- Programmable loop-back mode for self-test

General description

The C_CAN FD8 is a CAN IP module that can be realized as a stand-alone device, as part of an ASIC or as a FPGA (Altera or Xilinx).

The C_CAN FD8 performs communication according to ISO 11898-1:2015 up to 8 byte payload. For the connection to the physical layer additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the CAN_Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN FD8 can be accessed directly by an external CPU via the module interface. These registers are used to control/configure the CAN_Core and the Message Handler and to access the Message RAM.

The C_CAN FD8 module is delivered with an example of the AMBA APB bus interface from ARM. For Altera FPGAs the Altera Avalon bus interface is provided.

They can easily be replaced by a user-defined module interface.

Block Diagram



Block functions and size

CAN Core

The CAN_Core performs communication according to ISO 11898-1:2015. CAN FD with up to 8 byte payload is supported.

Message RAM

Stores 32 Message Objects and Identifier Masks.

Registers

All registers used to control and to configure the module.

Message Handler

State Machine that controls the data transfer between the Rx/Tx Shift Register of the CAN Core and the Message RAM as well as the generation of interrupts as programmed in the Control and Configuration Registers.

Module Interface

The Module Interface holds two interface control registers. The interface control registers are used to access the Message Objects in the message RAM. The Module Interface supports connection of the C_CAN FD8 to a wide range of customer CPUs.

Regional sales contacts

Europe/Japan	bosch.semiconductors@de.bosch.com
USA/Canada	bosch.semiconductors@us.bosch.com
China	bosch.semiconductors@cn.bosch.com
Korea	bosch.semiconductors@kr.bosch.com

www.bosch-semiconductors.com www.bosch-sensors.com Approximate size of C_CAN FD8 for ASIC designC_CAN FD813,7k gatesMessage RAM4,448 bits

Approximate size of C_CAN FD8 for Altera FPGAs 4000 Logic Elements (Cyclone III) + 4 M9Ks RAM

Approximate size of C_CAN FD8 for Xilinx FPGAs

32 Message Objects 2850 LUTs (Spartan 6) + Memory (32 x 139 bit)

Deliverables for ASIC design

- Well documented VHDL source code
- Complete test bench
- C_CAN FD8 User's Manual (programmer's view)
- C_CAN FD8 Module Integration Guide (designer's view)
- C_CAN FD8 Classical CAN Conformance Test Report

Deliverables for FPGA design

- Encrypted VHDL source code
- C_CAN FD8 User's Manual (programmer's view)
- C_CAN FD8 FPGA Integration Guide (designer's view)
- C_CAN FD8 Classical CAN Conformance Test Report
- Programming examples for fast start up

Supported FPGA vendors

- Altera
- Xilinx (on request)

Robert Bosch GmbH AE/MKC Postfach 13 42 72703 Reutlingen Germany

www.bosch.de

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