

Automotive Electronics

Product Information

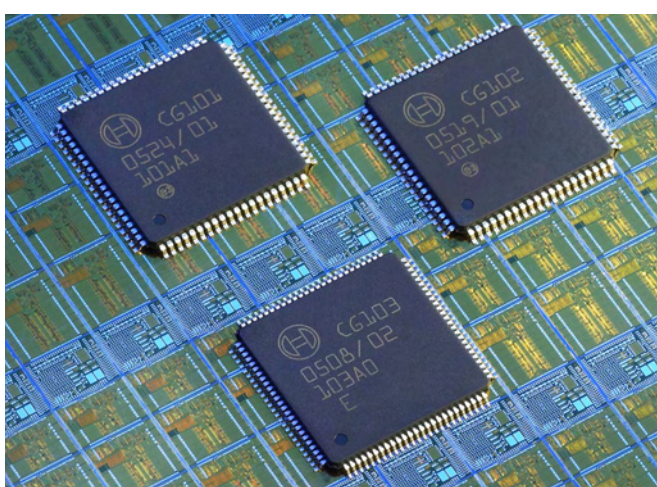
Airbag Chip Set 4th Generation

CG101, CG102, CG103



BOSCH

Invented for life



Single chip integrated airbag scalable system ASICs

Customer benefits:

- ▶ Excellent system know-how
- ▶ Smart concepts for system safety
- ▶ Secured supply
- ▶ Long- term availability of manufacturing processes and products
- ▶ QS9000 and ISO/TS16949 certified

Maximum ratings

All global pins are voltage robust for full battery range:

Description	Pin	Voltage range
Central protected supply	VZP	-0.3V...36V
Ignition high side driver	IGH	-0.3V...36V
Ignition low side driver	IGL	-0.3V...36V
External sensor interface	PSI	-0.3V...36V
Analog inputs	AIN	-0.3V...36V
Analog outputs	AIO	-0.3V...36V
Diagnosis line	DIA	-0.3V...36V
	DIA_SENSE	-18V....36V

Features

Features general

- ▶ airbag system on one chip
- ▶ highly scalable through modular design
- ▶ smart packaging using LQFP100 / 64 (on request)
- ▶ using advanced 0.35μ BCD process technology

Features power module

- ▶ Inrush current limitation
- ▶ energy reserve dc/dc up-converter 25V/33V
- ▶ supply voltage dc/dc down-converter 6.7V
- ▶ 5.0V linear voltage regulator
- ▶ 3.3V linear voltage regulator
- ▶ temperature control
- ▶ voltage monitoring and reset circuitry
- ▶ internal oscillator 1.6MHz
- ▶ sleep mode

Features firing loop module

- ▶ up to 12 firing loops
- ▶ power stages short circuit protected
- ▶ special disable channels

Features safety module

- ▶ safety controller for plausibility of crash datas
- ▶ Safety IDs for safety datas
- ▶ up to 6 general purpose analog inputs
- ▶ 2 general purpose analog I/Os
- ▶ internal ADC including sample & hold
- ▶ 8 channel analog multiplexer for ADC
- ▶ 3 watchdogs for clock and software control

Features interface module

- ▶ up to 4 sensor interfaces
- ▶ LIN 2.0 interface
- ▶ SPI 8MHz, 16 bit
- ▶ 48 channel low offset analog output amplifier AOUT
- ▶ 3.3V CMOS I/O interface

General description power module

- ▶ High Current Capability
 - ▶ 550mA @ VAS = 6.7V
 - ▶ 250mA @ VST50 = 5.0V
 - ▶ 200mA @ VST33 = 3.3V
- ▶ Power Supply Features
 - ▶ Precharging of energy reserve with different current levels of 350mA and 700mA
 - ▶ High efficiency energy reserve dc/dc up-converter with selectable ER voltage 25V / 33V
 - ▶ High efficiency dc/dc down-converter VAS 6.7V
 - ▶ 5.0V linear voltage regulator VST50
 - ▶ 3.3V linear voltage regulator VST33
 - ▶ Separated ground and supply pins for power, analog and digital supply
- ▶ Power Control
 - ▶ Over- and under voltage control of supply voltages VSTx
 - ▶ Power-on reset and delay
 - ▶ Integrated test functionality for energy reserve capacity
 - ▶ Current limitation of all supply voltages
 - ▶ Temperature control with automatic up-converter switch-off and temperature hysteresis
 - ▶ Sleep mode with quiescent current < 100uA
 - ▶ High precision band gap voltage reference
 - ▶ Redundant band gap for reference voltage monitoring
 - ▶ Internal oscillator 1.6MHz

General description safety module

- ▶ 1 watchdog for system clock control
- ▶ 2 watchdogs with answer-response mechanism for software control of foreground and background tasks
- ▶ Disable path for all high side power stages
- ▶ Disable path for all low side power stages
- ▶ Special disable path for dedicated power stage group
- ▶ Warning lamp control
- ▶ Timing control of enable times
- ▶ Configurable reset circuitry with optional control by all watchdogs in case of failure conditions
- ▶ 2 - 6 analog input AIN channels with current and voltage supply modes for hall sensors and buckle switches, programmable current capability and short circuit protection
- ▶ 2 analog output AIO low side drivers with programmable current capability and short circuit protection
- ▶ Internal 8bit ADC for current and voltage measurement
- ▶ Separate supply voltage for AIN channels possible
- ▶ Monitor SPI for read back of bus data
- ▶ Safety identifier mechanism for crash relevant data
- ▶ Different enable thresholds for crash relevant data in combination with safety ID mechanism
- ▶ Definition of enable and disable levels for buckle switch data evaluation
- ▶ Programmable register with lock control

General description firing loop module

- ▶ Different firing modes programmable by SPI
 - ▶ 1.75A @ 0.5ms
 - ▶ 1.75A @ 1ms
 - ▶ 1.2A @ 2ms
 - ▶ 1.2A @ 3ms
- ▶ Energy reserve maximum rating of 36V
- ▶ Firing voltage up to 25V
- ▶ High side and low side power stage short circuit protected
- ▶ Separated power supply of power stages
- ▶ Hardware or software controlled firing duration
- ▶ High resolution firing current counter (40kHz)
- ▶ High precision loop diagnostics for shorts, leakage currents and squib resistances
- ▶ Monitoring of squib pins and supply voltages via analog output AOUT
- ▶ Special disable of dedicated power stage groups
- ▶ Cross coupling on chip
 - ▶ Independent and separated control of high side and low side power stages
 - ▶ Max distance between high side and low side power stages
 - ▶ Free combination of high side and low side power stage
- ▶ Direct disable path for microcontroller control of power stages

General description interface module

- ▶ PSI 5.0 peripheral sensor interface
 - ▶ Supporting 8bit and 10bit peripheral acceleration sensors (PAS3, PAS4, PAS5)
 - ▶ Integrated reference resistance for all PSI channels
 - ▶ Data interpolation mode for synchronisation of sensor data
 - ▶ Adjustable receiver threshold level independent for all PSI channels
- ▶ Analog output amplifier with low offset, high bandwidth, tri-state output and selectable amplification range
- ▶ ISO interface compliance LIN 2.0
- ▶ 16bit SPI, 8MHz
- ▶ 2MHz external system clock input
- ▶ 3.3V CMOS I/O interface

The airbag chip set is designed to cover all needs of today's system designer requests by a modular ASIC design approach with:

- Scalable system architecture
- Extendable functionality
- High flexibility
- Pin compatibility
- Modular design

PIN configuration

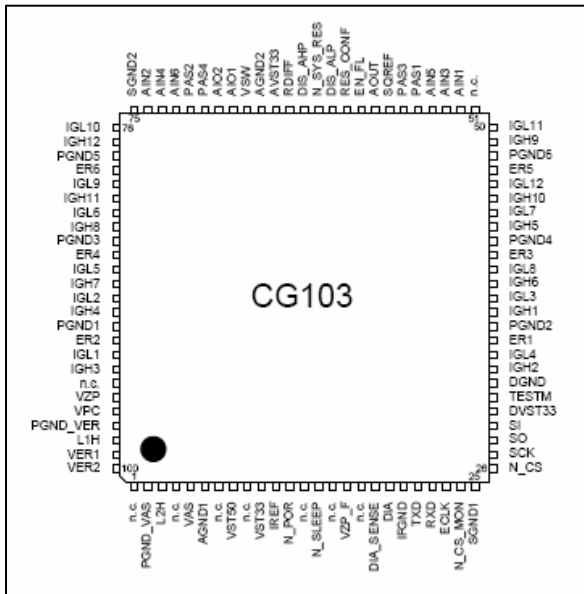


Figure: CG103 LQFP package

PIN description

Pin	Name	Direction	Description	Module
1	n.c.	-	not connected	-
2	PGND_VAS	ground	VAS power ground	POM
3	L2H	in/out	inductor 2 highside dc/dc down Converter	POM
4	n.c.	-	not connected	-
5	VAS	in/out	analog supply, dc/dc down converter output 6.7V, inductor 2 lowside	POM
6	AGND1	ground	analog ground	POM
7	n.c.	-	not connected	-
8	VST50	in/out	linear regulator output 5.0V	POM
9	n.c.	-	not connected	-
10	VST33	in/out	linear regulator output 3.3V	POM
11	IREF	out	current reference	POM
12	N_POR	out	power-on reset, low active	POM
13	n.c.	-	not connected	-
14	N_SLEEP	in	sleep mode control, low active	POM
15	n.c.	-	not connected	-
16	VZP_F	in	protected battery supply, filtered	POM
17	n.c.	-	not connected	-
18	DIA_SENSE	in	diagnosis sense input	IM: LIN
19	DIA	out	diagnosis output driver	IM: LIN
20	IFGND	ground	diagnosis interface ground	IM: LIN

Pin	Name	Direction	Description	Module
21	TXD	in	transmit data	IM: LIN
22	RXD	out	receive data	IM: LIN
23	ECLK	in	external clock input, 2MHz	IM: SPI
24	N_CS_MON	in	monitor chip select, low active	IM: SPI
25	SGND1	ground	substrate ground	POM
26	N_CS	in	chip select, low active	IM: SPI
27	SCK	in	serial clock	IM: SPI
28	SO	out	serial data out	IM: SPI
29	SI	in	serial data in	IM: SPI
30	DVST33	in	digital supply voltage input 3.3V	POM
31	TESTM	in	test mode activation	IM: SPI
32	DGND	ground	digital ground	POM
33	IGH2 *)	out	ignition high side	FLM
34	IGL4 *)	in	ignition low side	FLM
35	ER1 *)	in	energy reserve input	FLM
36	PGND2 *)	) ground	power ground	FLM
37	IGH1 *)	out	ignition high side	FLM
38	IGL3 *)	in	ignition low side	FLM
39	IGH6 *)	out	ignition high side	FLM
40	IGL8 *)	in	ignition low side	FLM
41	ER3 *)	in	energy reserve input	FLM
42	PGND4 *)	ground	power ground	FLM
43	IGH5 *)	out	ignition high side	FLM
44	IGL7 *)	in	ignition low side	FLM
45	IGH10 *)	out	ignition high side	FLM
46	IGL12 *)	in	ignition low side	FLM
47	ER5 *)	in	energy reserve input	FLM
48	PGND6 *)	ground	power ground	FLM
49	IGH9 *)	out	ignition high side	FLM
50	IGL11 *)	in	ignition low side	FLM
51	n.c.	-	not connected	-
52	AIN1	in/out	analog input	IM: AIN
53	AIN3	in/out	analog input	IM: AIN
54	AIN5	in/out	analog input	IM: AIN
55	PAS1 in/out		PAS interface supply voltage out, Data in	IM: PSI
56	PAS3 in/out		PAS interface supply voltage out, data in	IM: PSI
57	SQREF	out	squib reference	FLM
58	AOUT	out	analog output, multiplexed	IM: AOUT
59	EN_FL	in	enable firing loop	FLM
60	RES_CONF	in	reset configuration	SAM
61	DIS_ALP	out	disable all low side power stages	SAM
62	N_SYS_RES	in	system reset, low active	SAM
63	DIS_AHP	out	disable all high side power stages	SAM
64	RDIFF	out	ADC current measurement reference	IM: ADC
65	AVST33	in	analog supply voltage input 3.3V	POM
66	AGND2	ground	analog ground	POM
67	VSW	in	switch supply voltage input	IM: AIN
68	AIO1	in	analog I/O	IM: AIO
69	AIO2	in	analog I/O	IM: AIO
70	PAS4	in/out	PAS interface supply voltage out, data in	IM: PSI

Pin	Name	Direction	Description	Module
71	PAS2	in/out	PAS interface supply voltage out, data in	IM: PSI
72	AIN6	in/out	analog input	IM: AIN
73	AIN4	in/out	analog input	IM: AIN
74	AIN2	in/out	analog input	IM: AIN
75	SGND2	ground	substrate ground	POM
76	IGL10 *)	in	ignition low side	FLM
77	IGH12 *)	out	ignition high side	FLM
78	PGND5 *)	ground	power ground	FLM
79	ER6 *)	in	energy reserve input	FLM
80	IGL9 *)	in	ignition low side	FLM
81	IGH11 *)	out	ignition high side	FLM
82	IGL6 *)	in	ignition low side	FLM
83	IGH8 *)	out	ignition high side	FLM
84	PGND3 *)	ground	power ground	FLM
85	ER4 *)	in	energy reserve input	FLM
86	IGL5 *)	in	ignition low side	FLM
87	IGH7 *)	out	ignition high side	FLM
80	IGL2 *)	in	ignition low side	FLM
81	IGH11 *)	out	ignition high side	FLM
82	IGL6 *)	in	ignition low side	FLM
83	IGH8 *)	out	ignition high side	FLM
84	PGND3 *)	ground	power ground	FLM
85	ER4 *)	in	energy reserve input	FLM
86	IGL5 *)	in	ignition low side	FLM
87	IGH7 *)	out	ignition high side	FLM
80	IGL2 *)	in	ignition low side	FLM
89	IGH4 *)	out	ignition high side	FLM
90	PGND1 *)	ground	power ground	FLM
91	ER2 *)	in	energy reserve input	FLM
92	IGL1 *)	in	ignition low side	FLM
93	IGH3 *)	out	ignition high side	FLM
94	n.c	. -	not connected	-
95	VZP	in	protected battery supply	POM
96	VPC	in/out	precharged voltage, inductor 1 Lowside dc/dc up converter	POM
97	PGND_VER	ground	VER power ground	POM
98	L1H	in/out	inductor 1 highside dc/dc up converter	POM
99	VER1	in/out	energy reserve voltage, dc/dc up converter output 24.4V/33V	POM
100	VER2	in/out	energy reserve voltage, dc/dc up converter output 24.4V/33V	POM

*) differences for CG101/CG102, please see table FLM channel mapping

Table: Pin description LQFP100 package left side

PIN Compatibility

The ASICs CG101, CG102 and CG103 are functionally pin compatible. The CG103 defines the superset for all ASICs. Pins not available for the ASICs CG102 and CG101 are left unconnected (n.c.). AINx und PASx pins are pin compatible including their channel number, FLMx pins are functionally pin compatible but have different channel numbers.

Each module consists of 4 firing loop channels, 2 analog inputs (AINx) and 2 external sensor interfaces (PASx). For the first module instead of the two PASx pins there are two analog outputs (AIOx) available.

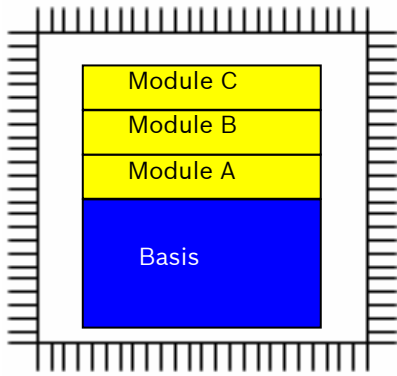


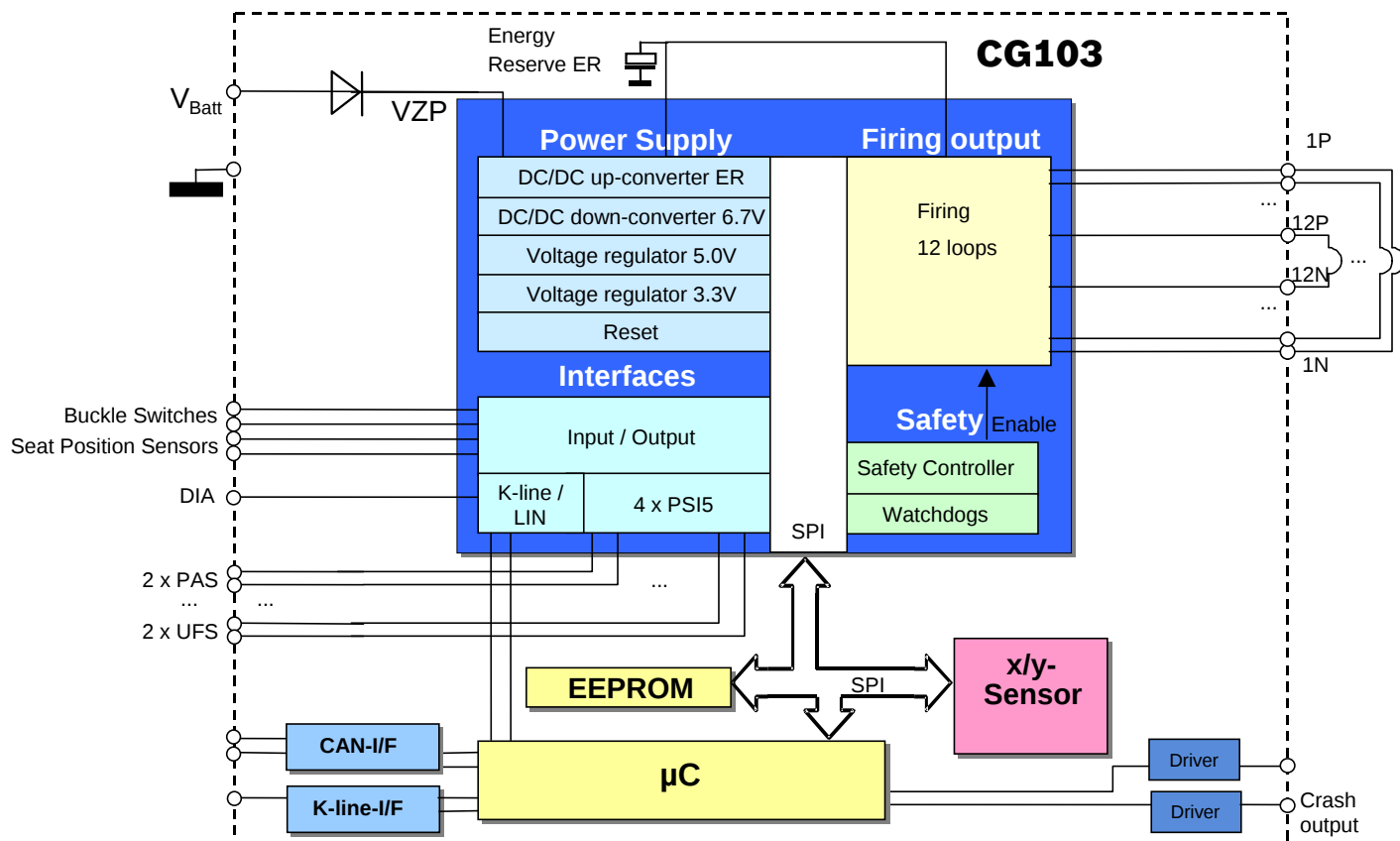
Figure: CG101, 102, 103 modules

The channels of the firing loop module (FLM) are mapped in the following manner:

Module	Pin name CG103	Channel map CG102	Channel map CG101
A	A ER5...6 IGH9...12 IGL9...12 PGND5...6	ER3...4 IGH5...8 IGL5...8 PGND3...4	- - - -
B	ER3...4 IGH5...8 IGL5...8 PGND3...4	ER1...2 IGH1...4 IGL1...4 PGND1...2	ER1...2 IGH1...4 IGL1...4 PGND1...2
C	ER1...2 IGH1...4 IGL1...4 PGND1...2	- - - -	- - - -

Table: FLM channel mapping

CG101 4 loops 2x AIN 0x PSI	CG102 8 loops 4x AIN 2x PSI	CG103 12 loops 6x AIN 4x PSI	
			LQFP100 body 14x14 pitch 0.5
			LQFP64 body 10x10 pitch 0.8 (on request)



ESD

All pins are guaranteed to resist electric static discharge voltages up to 2kV referring to human body model (HBM). Furthermore, all global pins are qualified for machine model (MM) 200V.

EMC

The chip set is designed under consideration of the latest guidelines for electronic magnetic immunity (EMI) and electronic magnetic emission (EME) and fulfills the recent EMC requirements. Complete EMC tests are performed on device level.

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